An Ultra-small 3 mm^2, 7.8 mΩ, 4 A, Load Switch with Discharge

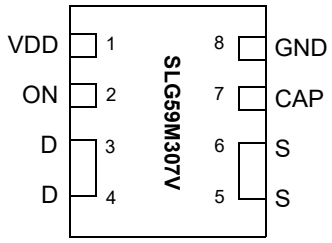
General Description

The SLG59M307V is a 7.8 mΩ, 4 A single-channel load switch that is able to switch 0.85 V to 5.5 V power rails. The product is packaged in an ultra-small 1.5 x 2.0 mm package.

Features

- 1.5 x 2.0 mm FC-TDFN package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- User selectable ramp rate with external capacitor
- 7.8 mΩ RDS_{ON} while supporting 4 A
- Discharges load when off
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -20 °C to 70°C
- Operating Voltage: 1.5 V to 5.5 V

Pin Configuration

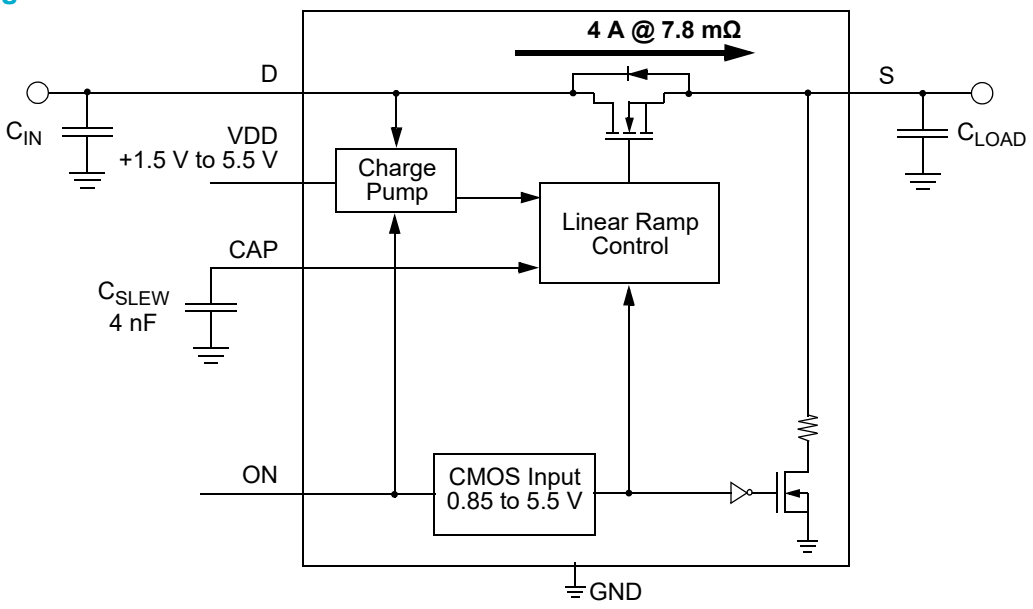


8-pin FC-TDFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	VDD supplies the power for the operation of the power switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor.
2	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M307V's state machine. ON is a CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH} > 0.85 V thresholds. While there is an internal pull-down circuit to GND (~4 MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller.
3, 4	D	MOSFET	Drain terminal connection of the n-channel MOSFET (2 pins fused for D). Connect at least a low-ESR 0.1 µF capacitor from this pin to ground. Capacitors used at D should be rated at 10 V or higher.
5, 6	S	MOSFET	Source terminal connection of the n-channel MOSFET (2 pins fused for S). Connect a low-ESR capacitor from this pin to ground and consult the Electrical Characteristics table for recommended C_{LOAD} range. Capacitors used at S should be rated at 10 V or higher.
7	CAP	Input	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V_S slew rate and overall turn-on time of the SLG59M307V. For best performance C_{SLEW} value should be ≥ 1.5 nF and voltage level should be rated at 10 V or higher.
8	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M307V	FC-TDFN	Commercial, -20 °C to 70 °C
SLG59M307VTR	FC-TDFN (Tape and Reel)	Commercial, -20 °C to 70 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		--	--	7	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	1.5 mm x 2 mm 8L FC-TDFN; Determined using 1 in^2, 1 oz. copper pads under each D and S terminals and FR4 pcb material	--	85	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	1	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	6	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -20 °C to 70 °C unless otherwise noted. Typical values are at T_A = 25 °C.

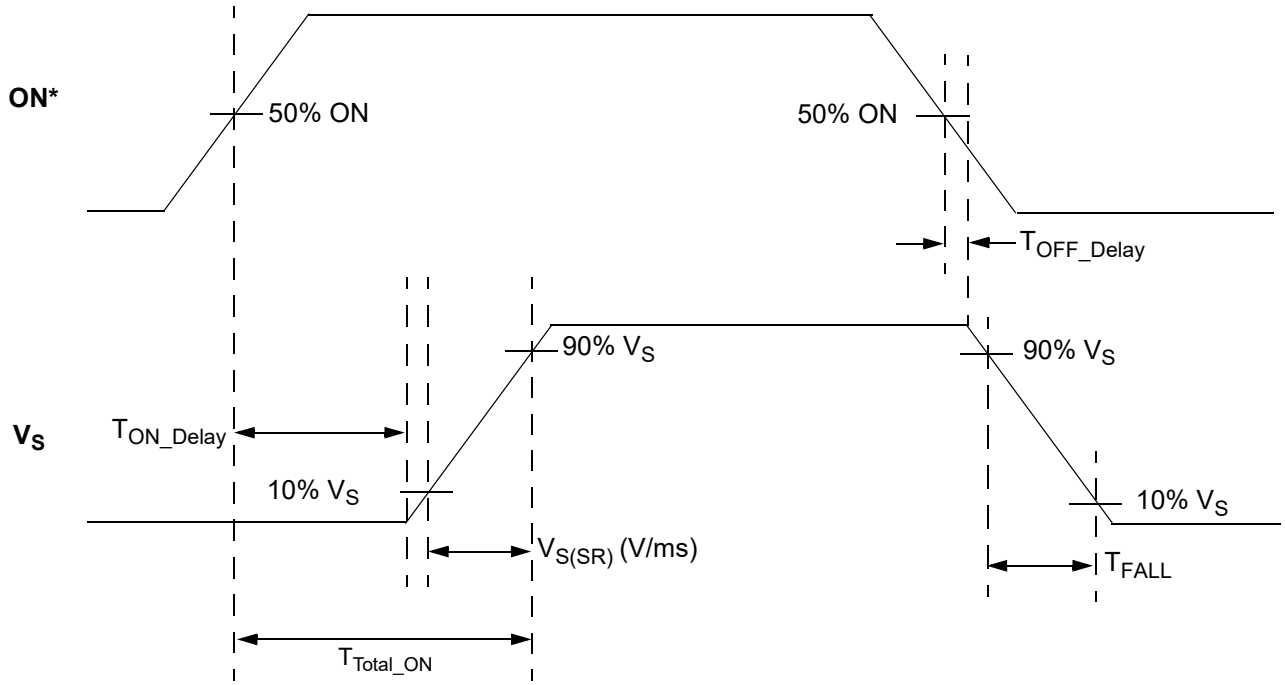
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	-20 °C to 70 °C	1.5	--	5.5	V
I_{DD}	Power Supply Current (PIN 1)	when OFF, ON = 0 V	--	--	1	µA
		when ON, No load	--	70	100	µA
RDS_{ON}	ON Resistance	T_A = 25 °C, I_{DS} = 100 mA	--	7.8	8.5	mΩ
		T_A = 70 °C, I_{DS} = 100 mA	--	8.5	9.6	mΩ
MOSFET IDS	Current from D to S	Continuous	--	--	4	A
V_D	Drain Voltage		0.85	--	V_{DD}	V
T_{ON_Delay}	ON Delay Time	50% ON to V_S Ramp Start; V_{DD} = V_D = 5 V; C_{SLEW} = 4 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω	--	300	500	µs
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_S	Set by External C_{SLEW}[1]			ms
		Example: C_{SLEW} = 4 nF, V_{DD} = V_D = 5 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω	--	1.96	--	ms
$V_{S(SR)}$	Slew Rate	10% V_S to 90% V_S	Set by External C_{SLEW}[1]			V/ms
		Example: C_{SLEW} = 4 nF, V_{DD} = V_D = 5 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω	--	3.0	--	V/ms
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from S to GND	--	--	500	µF
$R_{DISCHRG}$	Discharge Resistance		100	150	300	Ω
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S Fall Start, V_{DD} = V_D = 5 V, R_{LOAD} = 20 Ω, no C_{LOAD}	--	--	15	µs

Electrical Characteristics (continued)

T_A = -20 °C to 70 °C unless otherwise noted. Typical values are at T_A = 25 °C.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Notes: 1. Refer to typical timing parameter vs. C_{SLEW} performance charts for additional information when available.						

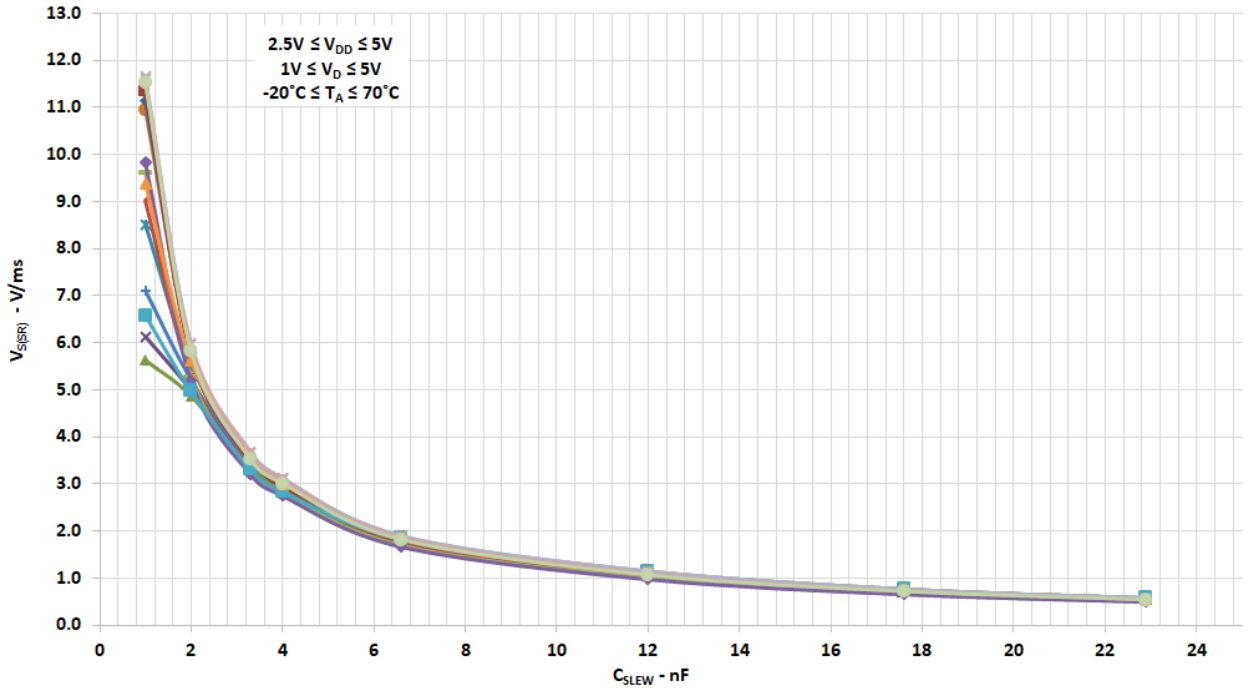
T_{ON_Delay}, $V_{S(SR)}$, and T_{Total_ON} Timing Details



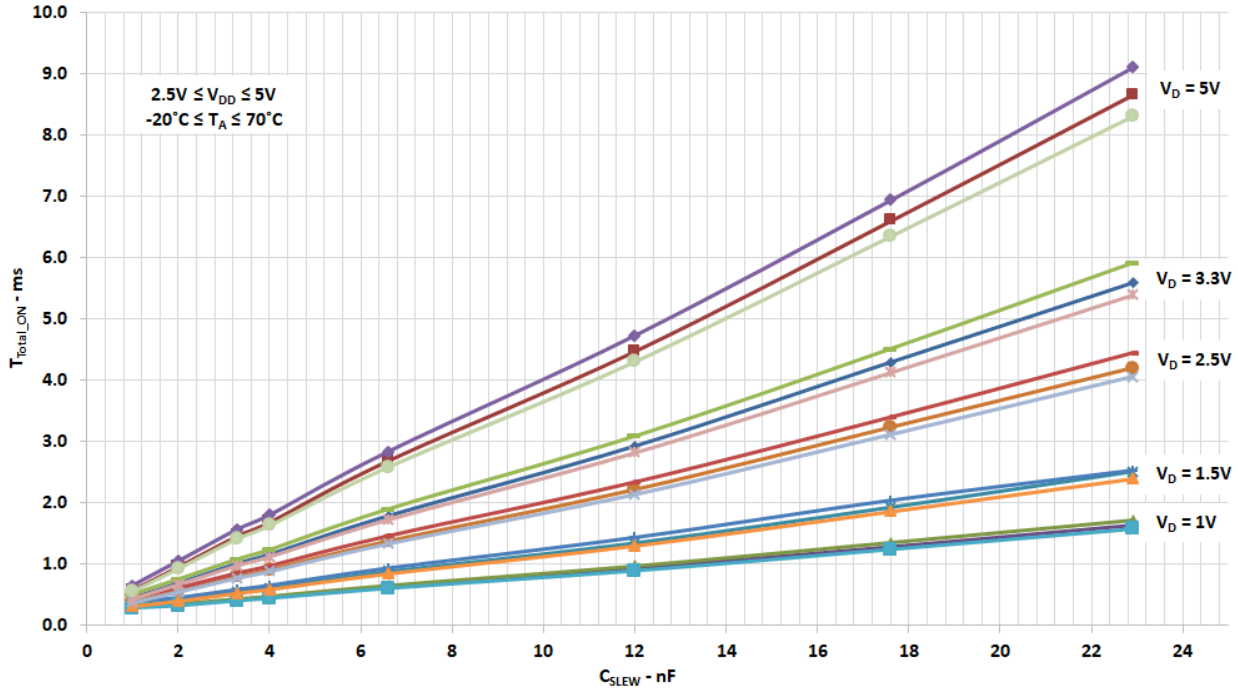
Note: * Rise and Fall times of the ON signal are 100 ns

Typical Performance Characteristics

V_S Slew Rate vs. C_{SLEW}, V_{DD}, and Temperature



T_{Total_ON} vs. C_{SLEW}, V_D, and V_{DD}



SLG59M307V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_D after V_{DD} exceeds 1 V. Then allow V_D to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_D need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 µF C_{LOAD} will prevent glitches for rise times of V_{DD} and V_D higher than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_D have reached their steady-state values, the load switch timing parameters may differ from datasheet specifications.

The slew rate of output V_S follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

Power Dissipation

The junction temperature of the SLG59M307V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59M307V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:
PD = Power dissipation, in Watts (W)
RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
I_{DS} = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

T_J = Junction temperature, in Celsius degrees (°C)
θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)
T_A = Ambient temperature, in Celsius degrees (°C)

For more information on Dialog GreenFET3 integrated power switch features, please visit our Documents search page at our website and see App Note “AN-1068 GreenFET3 Integrated Power Switch Basics”.

Layout Guidelines:

1.The VDD pin needs a 0.1 µF and 10 µF external capacitors to smooth pulses from the power supply. Locate these capacitors as close as possible to the SLG59M307V's PIN1.

2.Since the D and S pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 1, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

3.To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M307V's D and S pins;

4. The GND pin should be connected to system analog or power ground plane.

SLG59M307V Evaluation Board:

A GFET3 Evaluation Board for SLG59M307V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

Please solder your SLG59M307V here

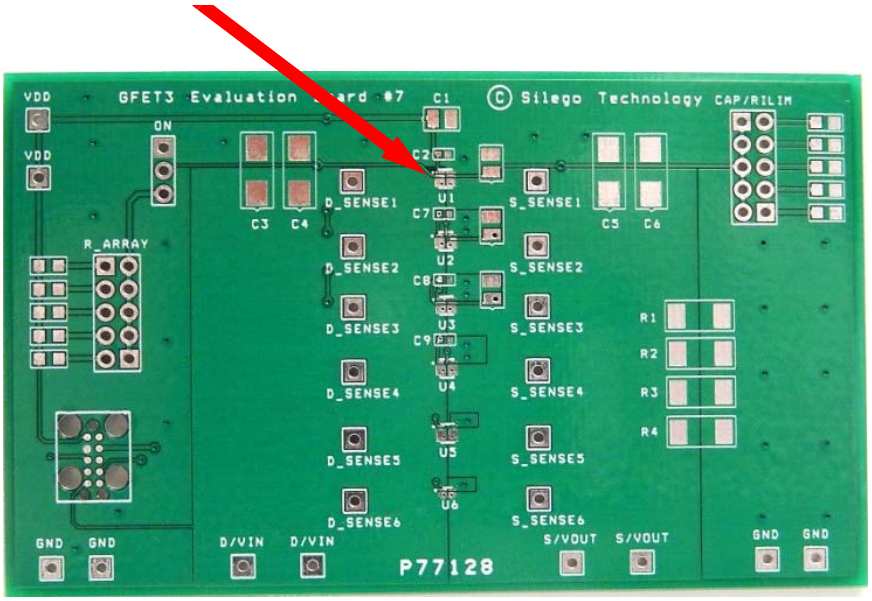


Figure 1. SLG59M307V Evaluation Board.

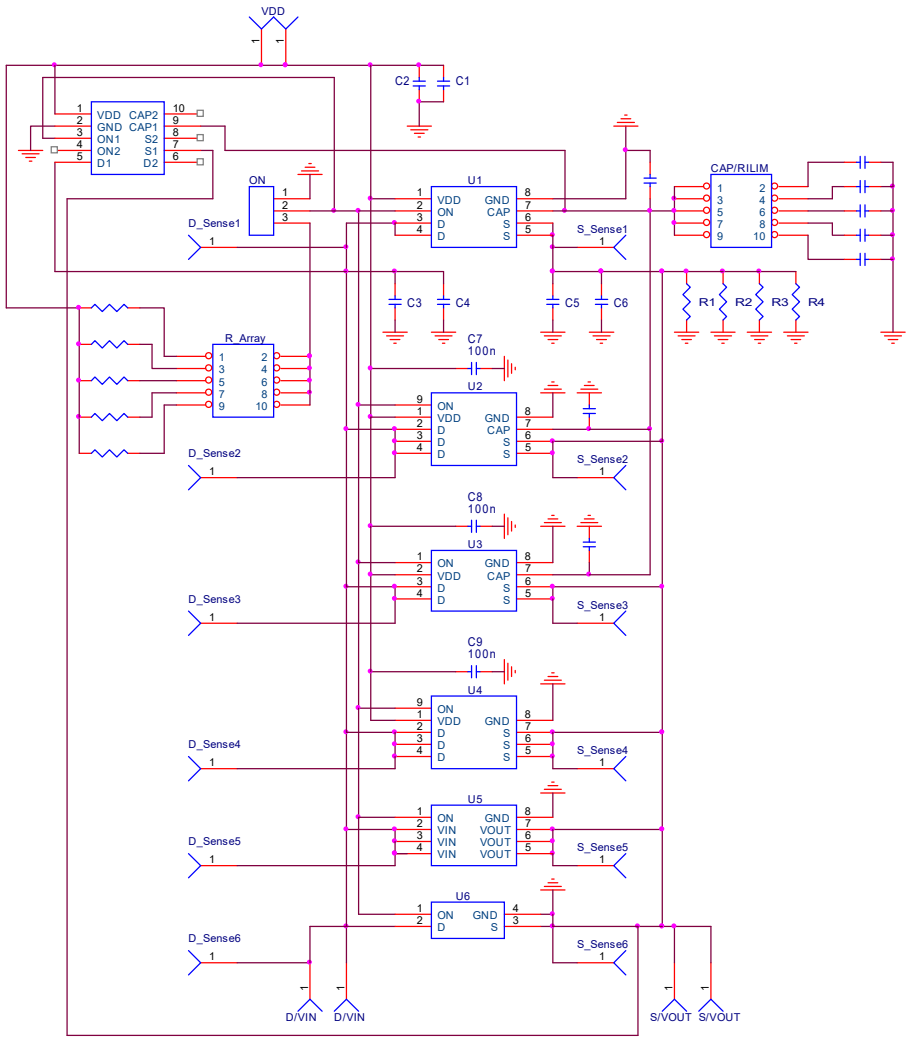


Figure 2. SLG59M307V Evaluation Board Connection Circuit.

Basic Test Setup and Connections

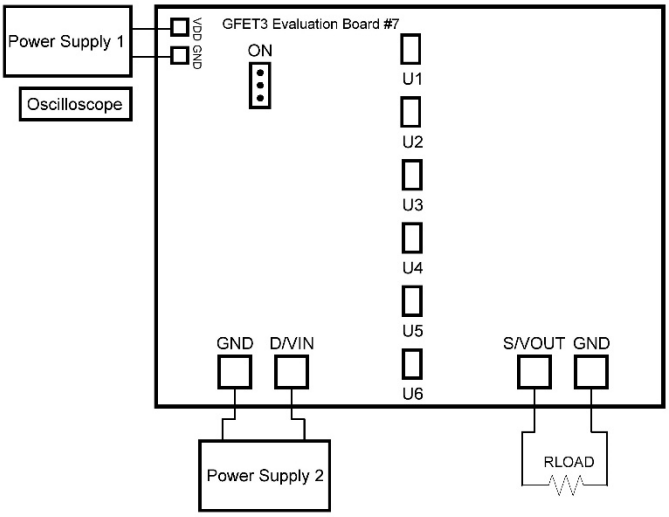


Figure 3. Typical connections for GFET3 Evaluation.

EVB Configuration

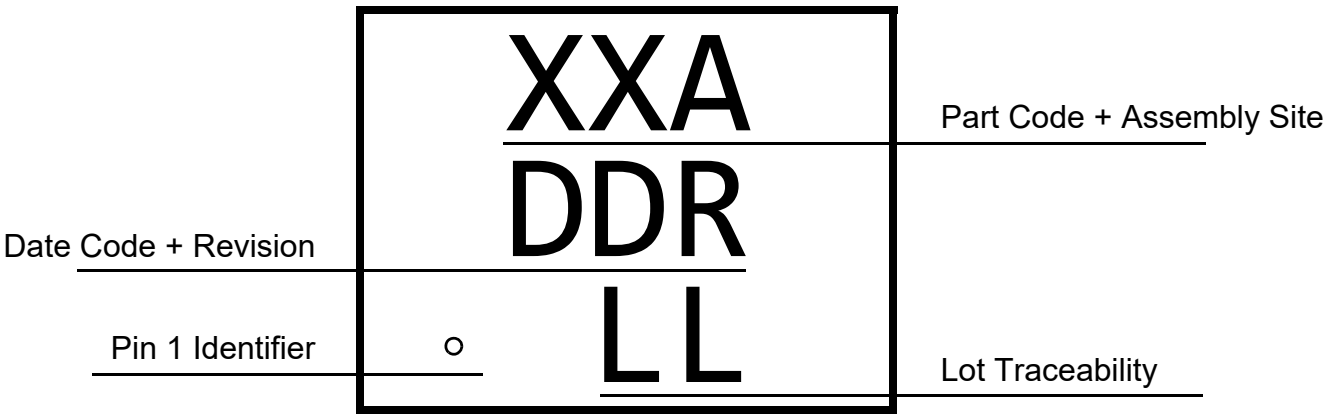
1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;

2.Turn on Power Supply 1 and set desired V_{DD} from 2.5 V…5.5 V range;

3.Turn on Power Supply 2 and set desired V_D from 0.85 V…5.5 V range;

4.Toggle the ON signal High or Low to observe SLG59M307V operation.

Package Top Marking System Definition

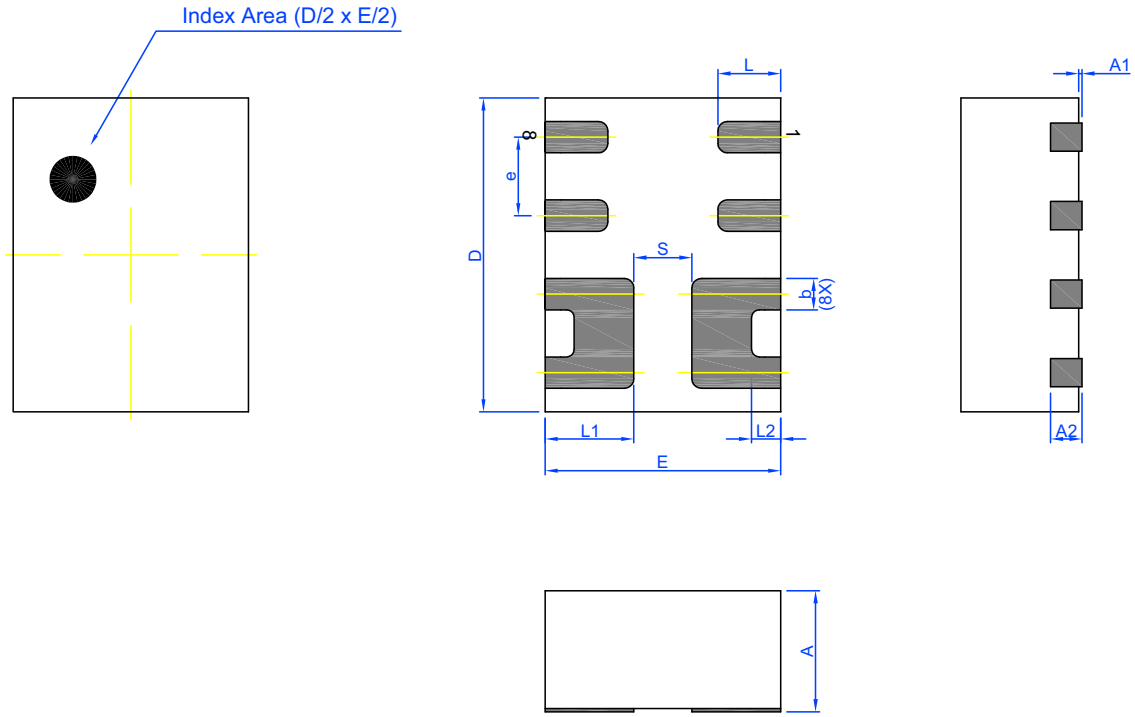


XX - Part Code Field[1]
A - Assembly Site Code Field[2]
DD - Date Code Field[1]
R - Part Revision Code Field[2]
LL - Lot Traceability Field[1]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

Package Drawing and Dimensions

8 Lead TDFN Package 1.5 x 2.0 mm (Fused Lead)
JEDEC MO-252



Unit: mm

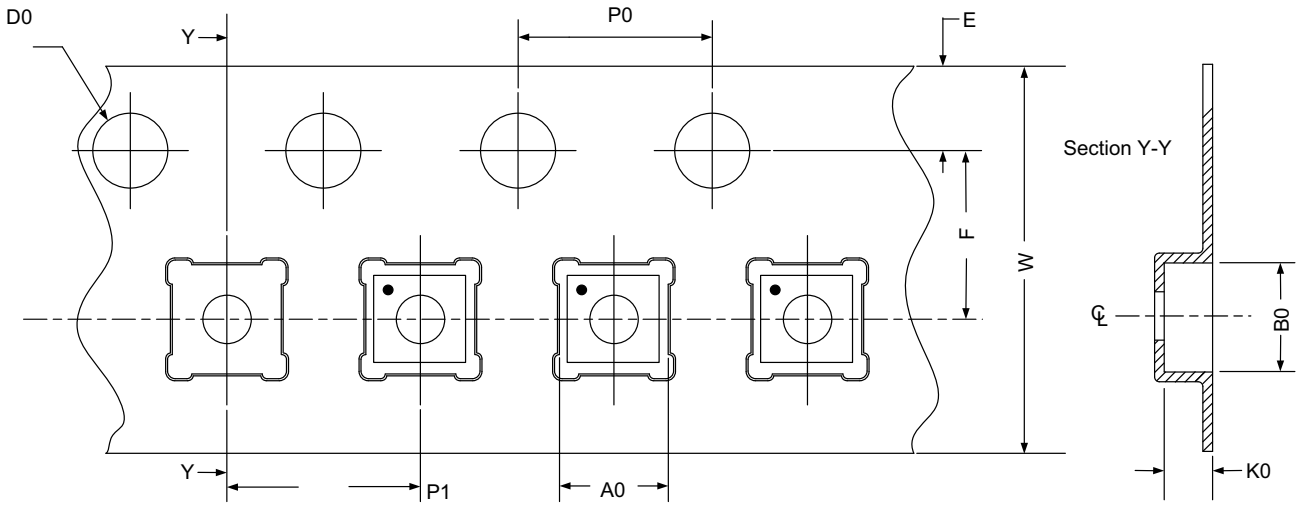
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.70	0.75	0.80	L	0.35	0.40	0.45
A1	0.005	-	0.060	L1	0.515	0.565	0.615
A2	0.15	0.20	0.25	L2	0.135	0.185	0.235
b	0.15	0.20	0.25	e	0.50 BSC		
D	1.95	2.00	2.05	S	0.37 REF		
E	1.45	1.50	1.55				

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L FC Green	8	1.5 x 2.0 x 0.75	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L FC Green	1.68	2.18	0.9	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.25 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
9/1/2020	1.02	Updated Style and Formatting Updated Charts Added Layout Guidelines
12/6/2013	1.01	Fixed typos
7/16/2013	1.00	Production Release