User Manual

DA16200 H/W Design Guide

UM-WI-006

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Terms and Definitions

PCB	Printed Circuit Board
QFN	Quad Flat No-Leads
RF	Radio Frequency
GPIO	General Purpose In/Out
DCDC	Direct Current Direct Current
LDO	Low Drop Out
RTC	Real-Time Clock
SFDP	Serial Flash Discoverable Parameters
QSPI	Quad Serial Peripheral Interface
SPI	Serial Peripheral Interface
AMBA	Advanced Microcontroller Bus Architecture

References

[1] <DA16200>, Datasheet, Dialog Semiconductor.

1 Introduction

This document provides a set of guidelines that help users prepare schematics and PCB layouts for products with the DA16200. Recommended schematic, chip interfaces and surrounding components as well as PCB layout guidelines of both devices are provided.

2 Schematic Guidelines

The DA16200 application schematic includes the following five parts:

- Power supply: Digital Power Supply, Analog Power Supply
- RF: Contains antenna part
- Clock: Main Clock, RTC Clock
- Flash interface
- Digital I/O: GPIO pin assignment, can be changed based on application requirement

The following chapter explains how to design.

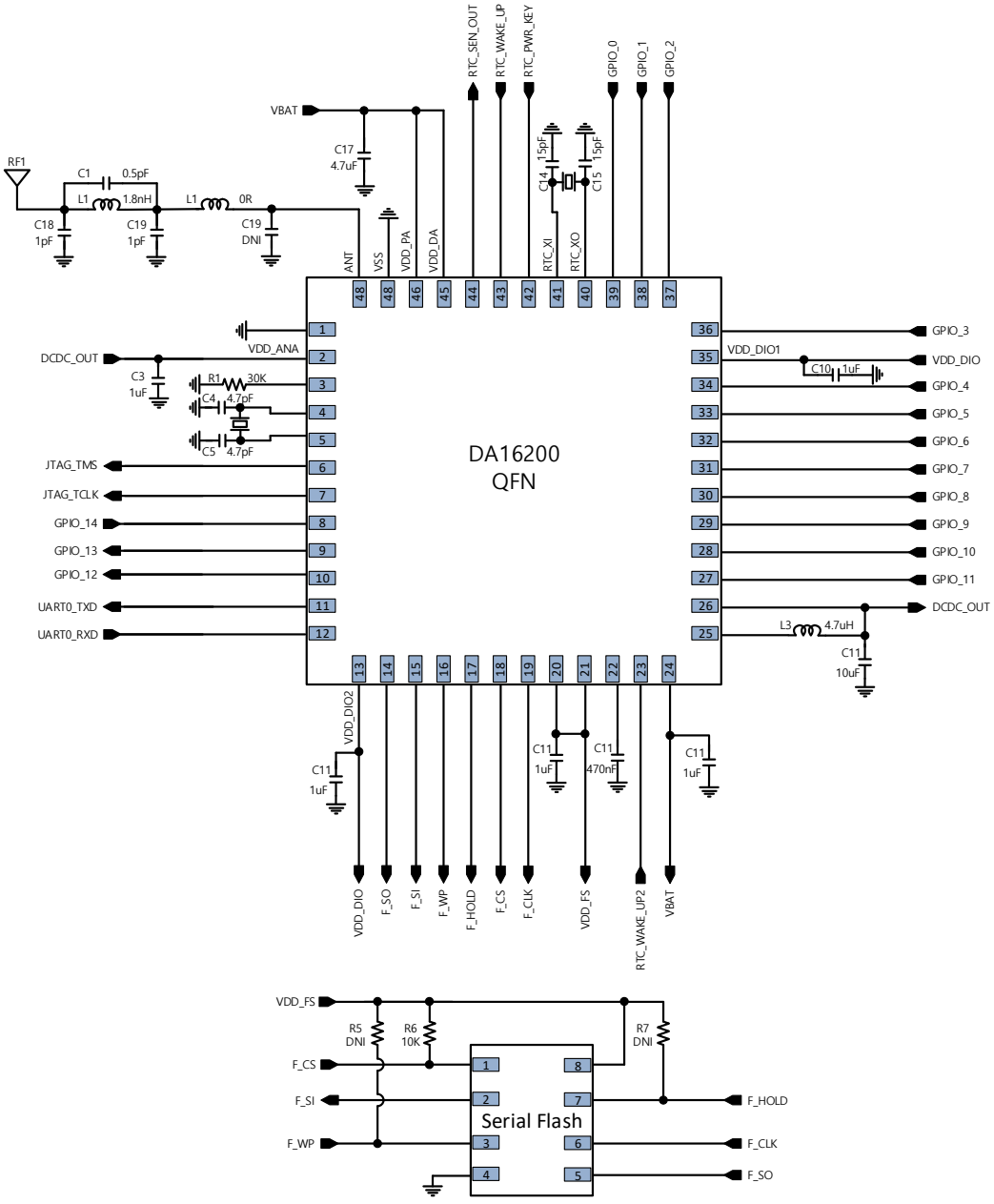


Figure 1: DA16200 Application Schematic

2.1 DA16200 Power Supply

2.1.1 Power Management

The DA16200 has one internal DC-DC converter and several LDOs to supply power to all internal sub-blocks. Power management does the on-off control of these regulators and is implemented through the register setting inside the RTC block.

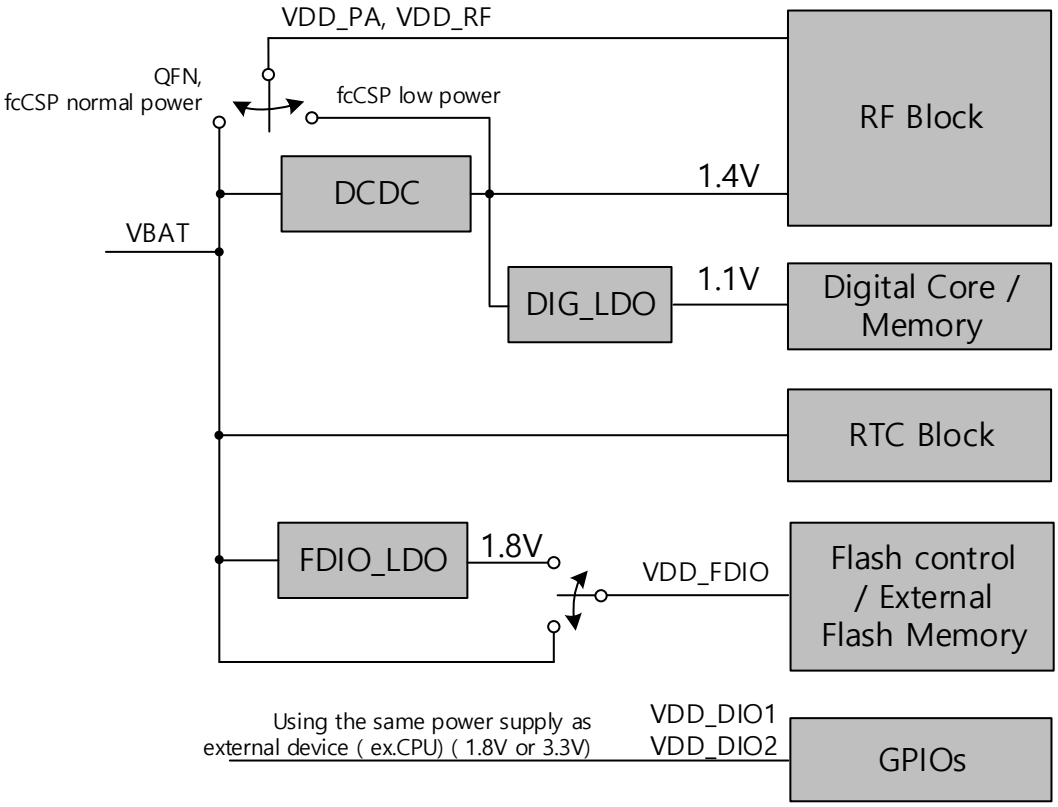


Figure 2: Power Management Block Diagram

Details of the internal DC-DC converters and LDOs are explained below:

- DC-DC converter: from the power supply of external VBAT input, it generates 1.4 V power for the digital LDO and RF block
- LDO for digital Blocks: from the DC-DC output, it generates 1.1 V power which is used for digital blocks
- LDO for I/O and external flash memory:
  - This LDO output is used only for 1.8 V digital I/O applications
  - From external VBAT power input, it generates 1.8 V output voltage which is used for digital I/O power domain in 1.8 V digital I/O applications
  - It is also used for external flash memory
  - For 3.3 V digital I/O applications, external power (3.3 V) is directly supplied for digital I/O power
- FDIO_LDO_OUT supports only 1.8 V

With the internal DC-DC converters and LDOs, all the power necessary for DA16200's internal sub-blocks are sufficiently generated.

Table 1 Power Pin Descriptions

QFN #Pin	fcCSP #Pin	Pin Name	Type	Description
1		GND	GND	Ground
2	D12	VDD_ANA	VDD	RF VDD
13	M8	VDD_DIO2	VDD	Supply power for digital I/O GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD
20	M4	VDD_FDIO	VDD	Flash IO Power
21		FDIO_LDO_OUT	AIO	Flash and IO ldo output and connect to external capacitor for flash LDO
22	L3	VDD_DIG	VDD	Digital power and connect to external cap. for DIG LDO
24	M2	VBAT	VDD	Supply power for internal DC-DC, DIO_LDO, and analog IP
25	L1	DCDC_LX	AIO	Internal DC-DC feedback input for digital block supply
26	J1	DCDC_FB	AIO	Internal DC-DC feedback output for digital block supply
35	C1	VDD_DIO1	VDD	Supply power for digital I/O GPIOA0~GPIOA11
45	A7 B8	VDD_DA	VDD	Tx DA power and RTC block power
46		VDD_PA	VDD	Supply power for integrated power amplifier
47		GND	GND	Ground
fcCSP GND Pin: A1, A9, B6, B10, B12, C7, C9, C11, D8, D10, F6, F8, F10, F12, G5, G7, G9, H4, H8, H10, J3, K2, L5, M6, M12, E5				

2.1.2 VBAT

DA16200 can operate one source for an I/O interface and internal power source (LDO and DC/DC converter) so it is important to reduce the noise component in this power line. All the input de-coupling capacitors should be located nearby DA61200 and the thickness of power traces should be higher than 0.3 mm.

2.1.3 Internal DC/DC

DA16200 contains one DC/DC converter for the analog and digital part. This DC/DC converter needs to connect a series 4.7 µH power inductor for high-power efficiency and a shunt 10 µF capacitor to reduce switching noise, so the inductor and capacitor are located as close as possible for stable power supply. And 1 µF is required to other bypass capacitors for power supply.

2.2 RF

The RF application circuit is important to get an optimum performance from the device. An improper circuit and layout can cause performance degradation for sensitivity, output power, error vector magnitude (EVM) and spectral mask.

2.2.1 Antenna

The antenna is the element used to convert the guided waves on the PCB traces to free-space electromagnetic radiation. The position and layout of the antenna is very important to increase coverage and data rates. Section 2.2.2 has details about a tested antenna part.

2.2.2 Antenna information of DA16200 EVK

- Part number
  WALSIN RFECA32160AM1T62
- Dimension

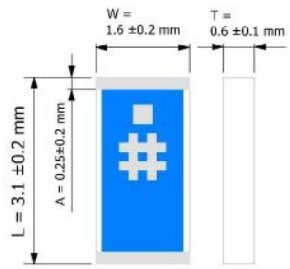
Figure	Symbol	Dimension (mm)
	L	3.10 ± 0.20
	W	1.60 ± 0.20
	T	0.60 ± 0.10
	A	0.25 ± 0.20

Figure 3: Tested Antenna Dimension

- Tested Antenna usage example

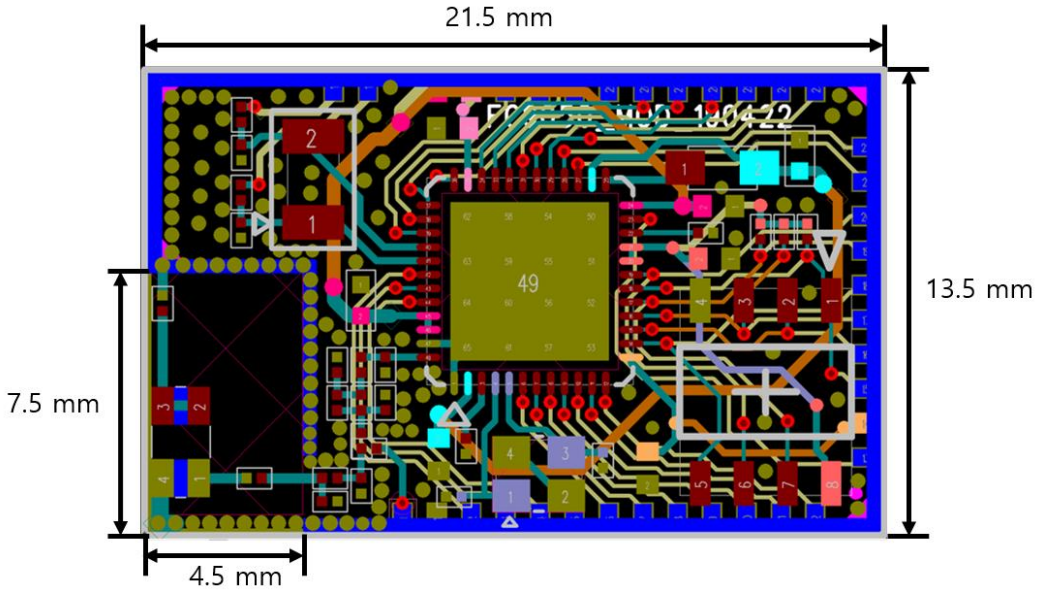


Figure 4: Tested Antenna Usage

- Radiation Pattern

Unit : dBm

Test Channel	2412 CH	2442 CH	2462 CH
T I S	72.28	72.49	72.46
Max.	75.51	76.02	76.52
Min.	67.29	67.38	64.82
NHPIS 30	70.98	71.12	71.02
UHIS	70.70	70.97	70.99
UHIS Ratio	55.27	56.61	57.46
Conduction	108.00	108.00	108.00

Unit : dBm

Test Channel	2412 CH	2442 CH	2462 CH
T R P (@30˚)	12.14	11.31	10.75
Max.	15.92	15.24	15.69
Min.	7.11	6.17	5.42
NHPRP 30˚	10.89	9.98	9.38
UHRP	10.51	9.84	9.29
UHRP Ratio	54.70%	56.48%	57.63%
Conduction	24.00	24.00	24.00

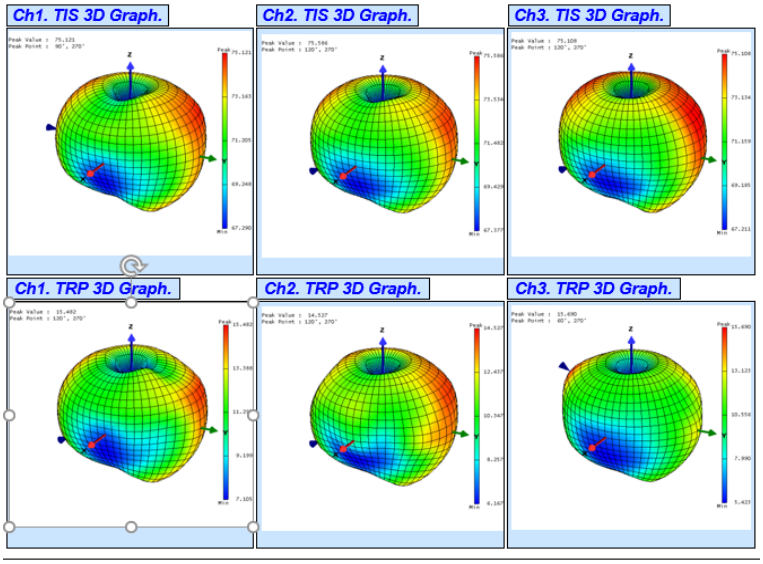


Figure 5: Tested Antenna Radiation Pattern

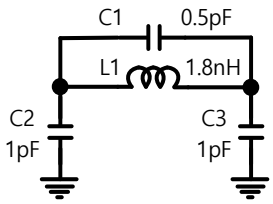
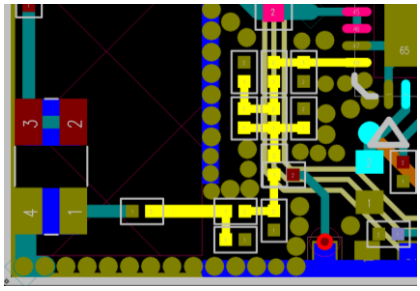
Below is the consideration for the antenna part.

1. Put the antenna on the edge or corner of the PCB.
2. Signal lines must not be routed across the antenna elements on all the layers of the PCB.
3. The ground is needed for copper keep-out on all layers include inner layers.
4. Matching components for the antenna are needed to optimize each board.
5. The return loss measured at the matching components of the antenna need to be better than -10 dB to get the optimum system performance.

2.2.3 RF Input Requirement

The RF part must have matching components and an RF filter to suppress any harmonic element. A Passive filter which is made by a lumped component can meet the system requirements because the DA16200 has good harmonic suppression performance.

Table 2 Recommended LC filter

LC filter circuit	LC filter layout
	

The RF line needs to be isolated by using ground plane with clearance to ensure good performance (output power, EVM, SEM and sensitivity).

2.3 Clock

2.3.1 Main Clock

DA16200 has a crystal oscillator for the main clock source, which supports the external crystal clock. Basically, the external clock is 40 MHz. Make sure that the load capacitance is tuned based on the board parasitic so that the frequency tolerance is within ±20 ppm. And the clock line needs to route closer to the XTAL routing to avoid any phase noise degradation.

2.3.2 RTC Clock

The 32.768 kHz RTC clock source is necessary for the free-running counter in the RTC block. The external clock is 32.768 kHz. Make sure that the load capacitance is tuned based on the board parasitic so that the frequency tolerance is within ±250 ppm.

2.4 Serial Flash

2.4.1 Serial Flash Interface

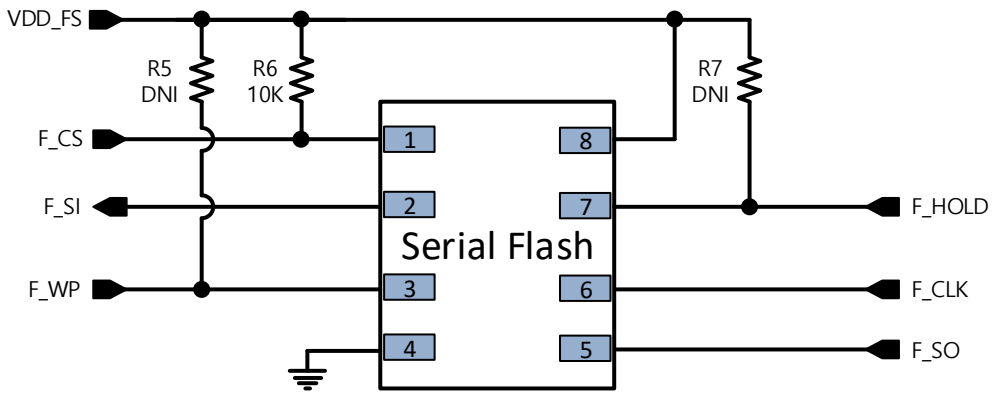


Figure 6: Serial Flash Application Schematic

The QSPI master supports 4-line SPI communication with commercial flash memory devices and uses a Motorola SPI-compatible interface among SPI communication modes. The highest communication speed is the same as the AMBA bus clock, and the speed is adjustable in integer multiples. The designed QSPI supports 4-/2-/1-line types depending on the purpose. These types should be combined. Especially when 1-line communication mode is used, it can be used as the SPI master.

2.4.2 Serial Flash Selection Guide

- The '.img' of DA16200 has a structure as shown in Figure 7.

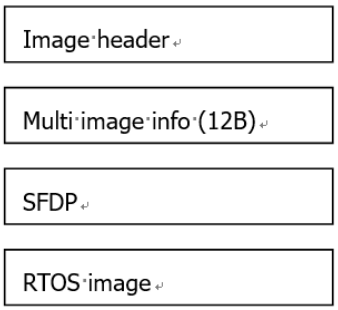


Figure 7: DA16200 Image Structure

- SFDP (Serial Flash Discoverable Parameters) is a standard table for the main parameters of serial flash defined by JEDEC. This is information about the characteristics - access timing, supported commands, and delay parameter - of each serial flash manufactured by various vendors, and those should be optimized for each serial flash.
- Currently the DA16200 SDK supports SFDP tables for 7 types of serial flashes listed in Table 3.

Table 3 Recommended Serial Flash List

Vendor	Part number
ISSI	IS25LQ032B
ISSI	IS25WP016D
ISSI	IS25LP032D (IS25LP016D)
Winbond	W25Q032JVSNIQ
Winbond	W25Q16JVSNIQ
Macronix	MX25L3233F
Macronix	MX25U3232F

- If customers want to use other types of serial flash, then the extraction (from serial flash specification) and optimization of the SFDP parameters is needed. And a new serial flash should be used, the schedule shown in Table 4 is required, which the customer should take into consideration in their project planning.

Table 4 New Flash verification process

New Flash verification process
'D': date of receiving the board-adopted new serial flash a. Extract SFDP parameter - D + 10 b. Apply SFDP table to img & function test - D + 15 - Function test in normal condition c. Reliability test - Function test in severe condition - D + 21 d. Final SDK release - D + 30

3 PCB Layout Example

3.1 Grounding

- Make the internal ground area as solid as possible. Do not break the ground into pieces.
- Provide good solid ground by using multiple vias
- Fill as much ground as possible in the area between the walls of shield cavities and the outline of the RF section
- Connect each ground pin or via to the ground plane individually.
- Put the Ground via on the PAD of the QFN package

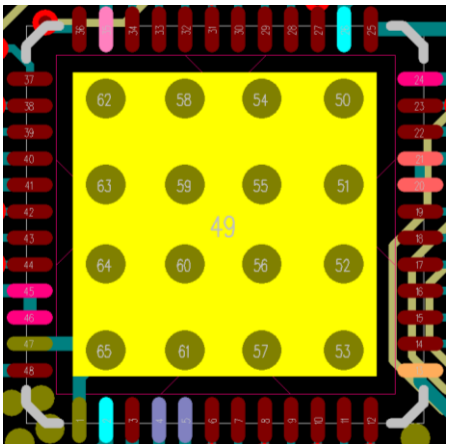


Figure 8: Ground vias on PAD

3.2 PCB Layout Example

- Layer 1 (Top)

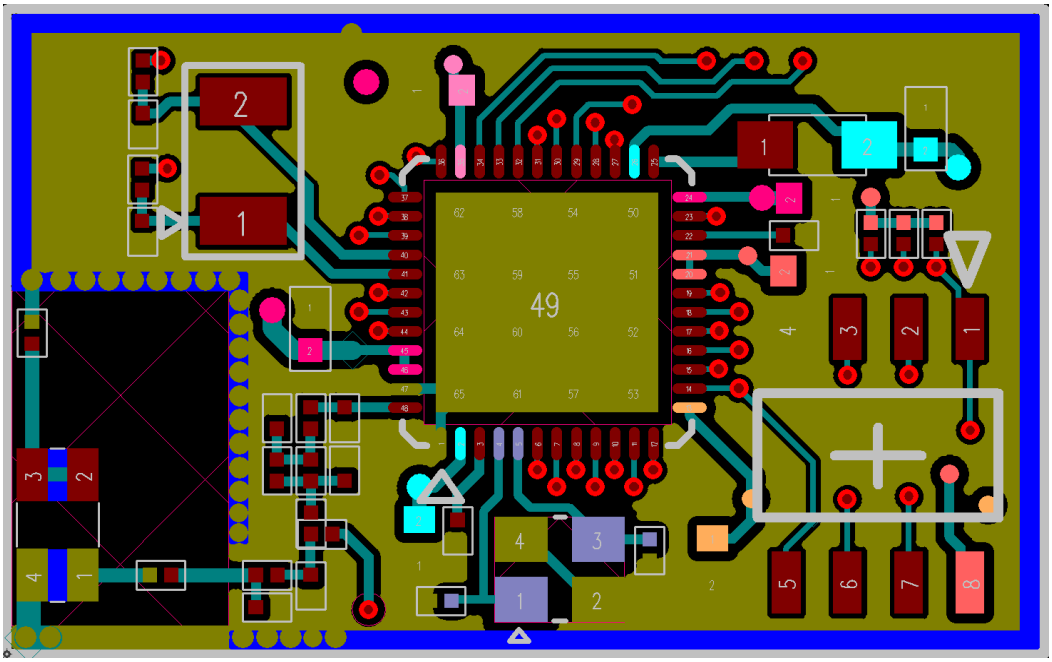


Figure 9: PCB Layout Example: Top layer

- Layer 2

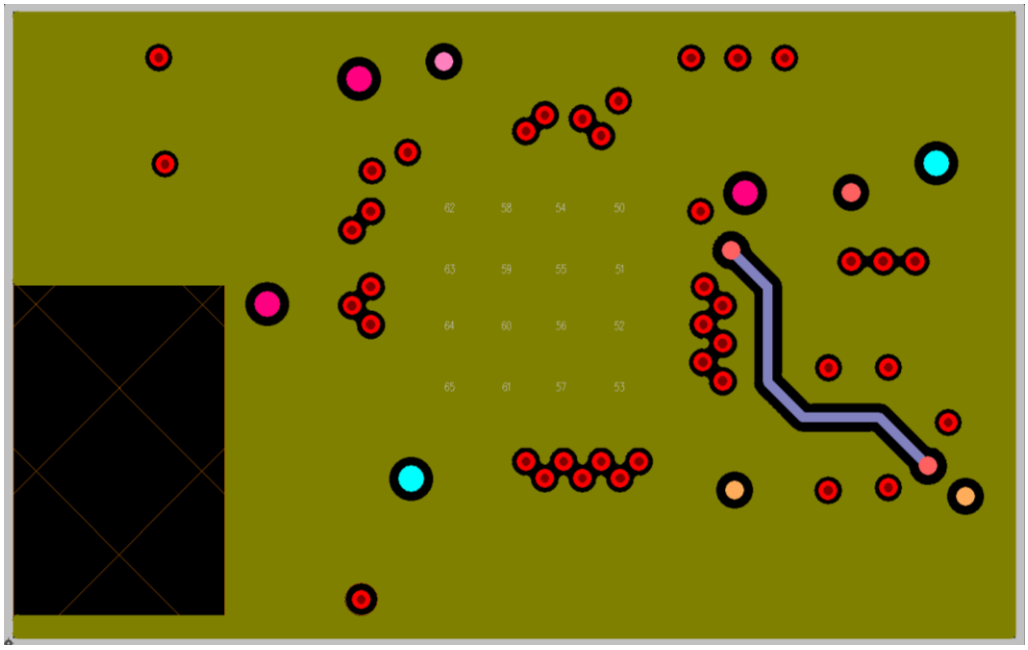


Figure 10: PCB Layout Example: 2nd layer

- Layer 3

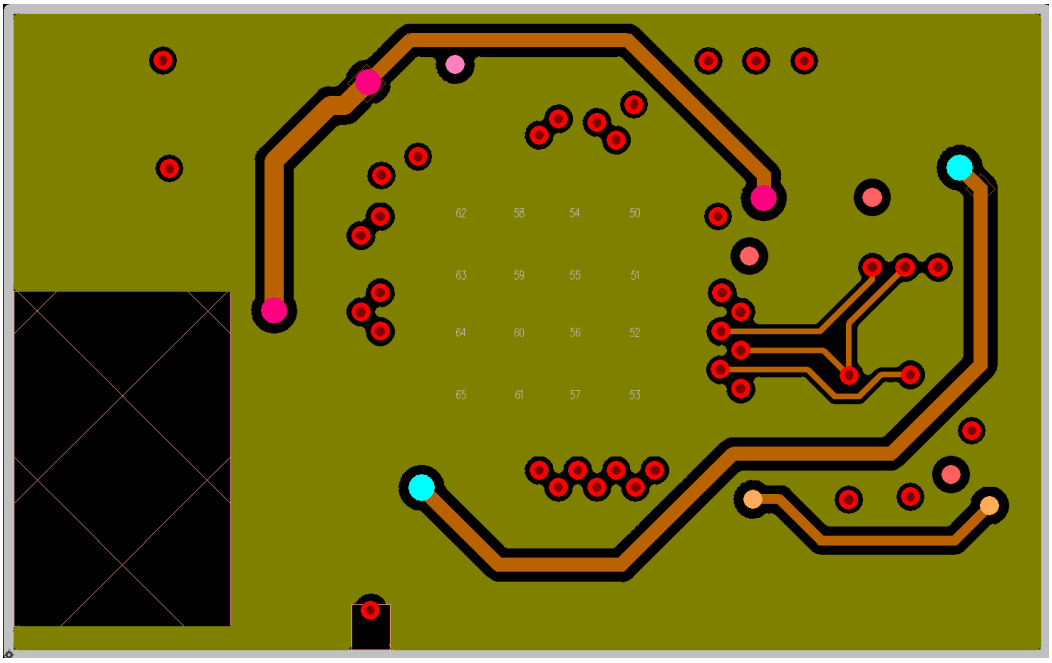


Figure 11: PCB Layout Example: 3rd layer

- Layer 4(Bottom)

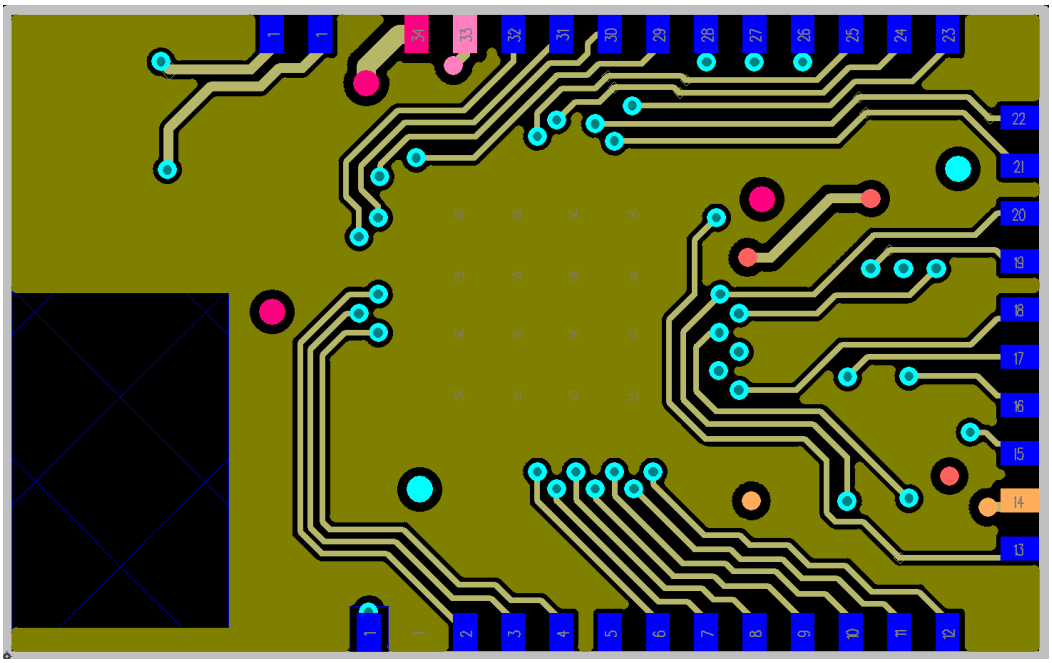


Figure 12: PCB Layout Example: Bottom layer

4 Recommended Footprint

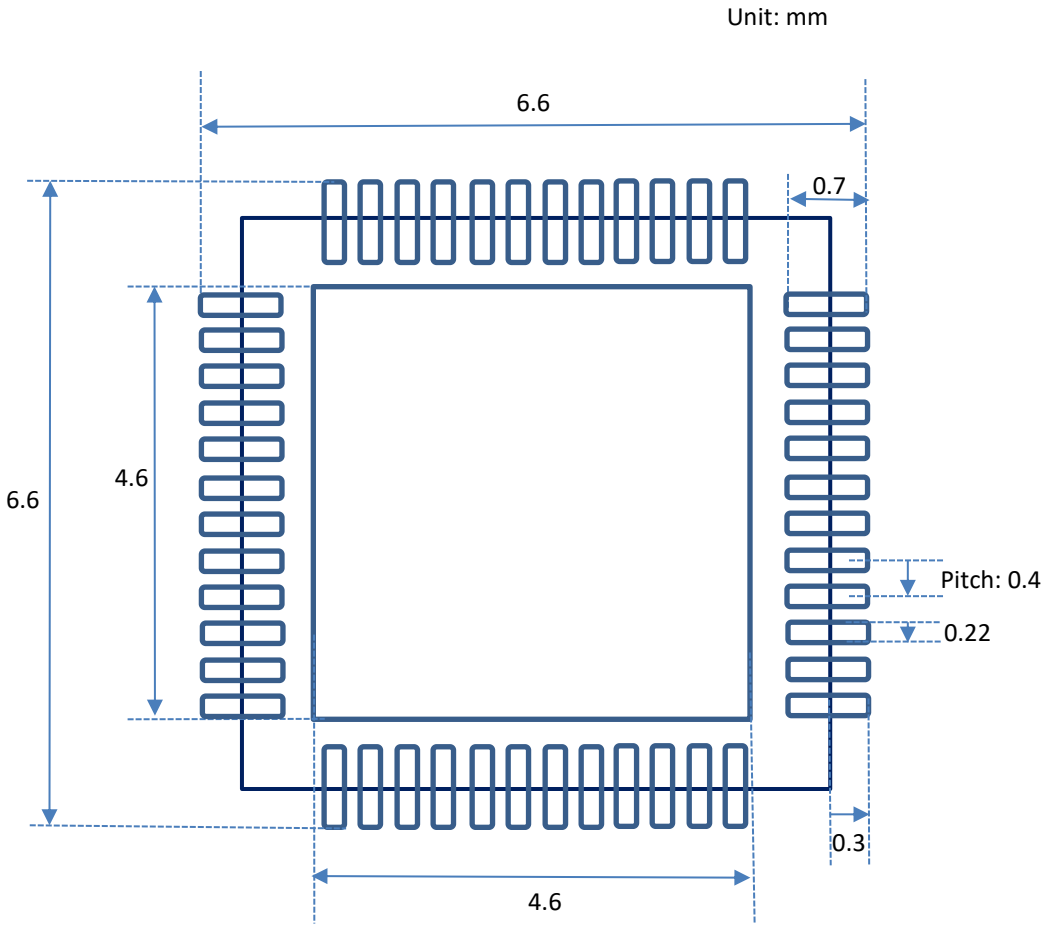


Figure 13: DA16200 Ground Footprint

Revision History

Revision	Date	Description
1.3	14-Oct-2020	Table 3 Updated, Section 2.1.1 Power Management Updated
1.2	29-Oct-2019	Removed Draft status; finalized for release
1.1	21-Oct-2019	Editorial review
1.0	30-Aug-2019	Preliminary DRAFT Release

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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