

Errata

CCE4502

CE-IO-002

Abstract

This document contains the known errata for CCE4502 and the recommended workarounds.

1 Information

Datasheet	CCE4502, rev. 2.4
Package(s)	QFN-24, CSP

2 Identifying the Silicon Revision

Read register REV (0x60) to determine the silicon revision. Affected revisions read 0xCC, 0xCD or 0x40.

3 Errata Summary

Table 1: Errata Summary

Issue #	Issue Title
1	Latch-up immunity

4 Errata Details

Table 2: Latch-up immunity

Issue #	Effect
1.	The specified latch-up immunity of VDD5 and VREF is only guaranteed within absolute maximum ratings.
	Conditions
	n. a.
	Technical Description
	Latch-up can occur at pins VDD5 and VREF if voltages at the pins or currents into or out of these pins exceed absolute maximum ratings. Latch-up can lead to malfunction or permanent damage of the device.
	Workaround
Do not connect VREF or VDD5 to external sources which may force voltages at the pins that exceed absolute maximum ratings, such as hot plugged connectors.	

Document Revision History

Revision	Date	Description
1	25-Jan-2021	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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