Auto Grade 0.8 mm Pitch Multi-Phase Buck Converter

General Description

DA9223-A and DA9224-A are PMICs optimized for the supply of CPUs, GPUs, and DDR memory rails in automotive in-vehicle infotainment systems, Advanced Driver Assistance Systems (ADAS), navigation and telematics applications. The fast transient response (10 A/µs) and load regulation are optimized for the latest generation of multi core application processors.

DA9223-A operates as a single four-phase buck converter delivering up to 16 A output current.

DA9224-A integrates two dual-phase buck converters, capable of delivering 2 x 8 A output current.

Each buck regulates a programmable output voltage in the range of 0.3 V to 1.57 V. With an external resistor divider the output voltage can be set to any voltage between 1.57 V and 4.3 V. The input voltage range of 2.8 V to 5.5 V makes it suited for a wide variety of low voltage systems, including all Li-Ion battery powered applications.

To guarantee the highest accuracy and to support multiple PCB routing scenarios without loss of performance, a remote sensing capability is implemented in both the DA9223-A and DA9224-A.

The power devices are fully integrated, so no external FETs or Schottky diodes are needed.

A programmable soft start-up can be enabled, which limits the inrush current from the input node and secures a slope controlled activation of the rail.

The Dynamic Voltage Control (DVC) supports adaptive adjustment of the supply voltage depending on the processor load, either via direct register writes through the communication interface (I^2C or SPI compatible) or via an input pin.

DA9223-A and DA9224-A feature integrated over-temperature and over-current protection for increased system reliability without the need for external sensing components. The safety feature set is completed by a VDDIO under voltage lockout.

The configurable I^2C address selection via GPI allows multiple instances of DA9223-A and DA9224-A to be placed in an application sharing the same communication interface with different addresses.

Key Features

- 2.8 V to 5.5 V input voltage
- 1 x 16 A DA9223-A
- 2 x 8 A DA9224-A
- 3 MHz nominal switching frequency (allows use of low profile [1 mm] inductors)
- ±1 % accuracy (static)
- ±3 % accuracy (dynamic)
- 0.3 V to 1.57 V output voltage
  1.57 V to 4.3 V with resistor divider
- Dynamic Voltage Control (DVC)
- Automatic phase shedding
- Integrated power switches
- Remote sensing at point of load
- I^2C/SPI compatible interface
- Adjustable soft start
- -40 °C to +105 ºC temperature range
- AEC-Q100 grade 2 qualified
- 66 TFBGA 0.8 mm pitch

Applications

- In-car infotainment
- Automotive display clusters
- Advanced Driver Assistance Systems (ADAS)
- Navigation and telematics
- Mobile computing
- Industrial embedded systems

System Diagrams

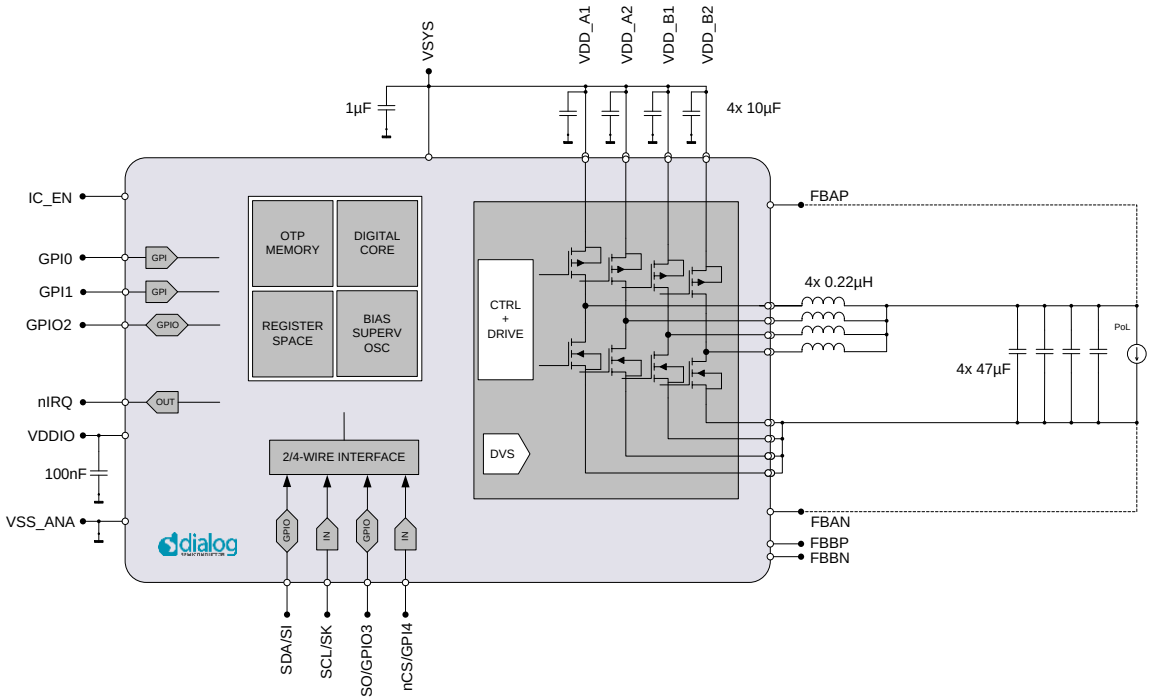

Figure 1: DA9223-A System Diagram

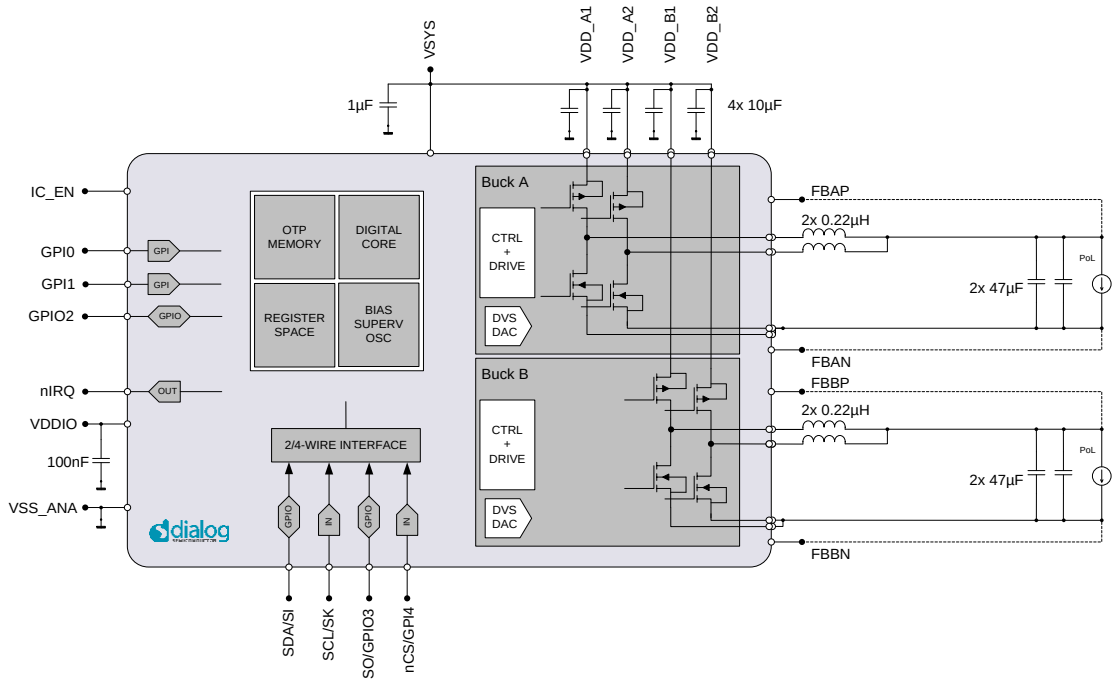

Figure 2: DA9224-A System Diagram

Contents

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Tables

1 Terms and Definitions

AP	Application Processor
CPU	Central Processing Unit
DDR	Dual Data Rate
DVC	Dynamic Voltage Control
FET	Field Effect Transistor
GPI	General Purpose Input
GPU	Graphic Processing Unit
IC	Integrated Circuit
OTP	One Time Programmable memory
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
POL	Point Of Load
PWM	Pulse Width Modulation

2 Pinout

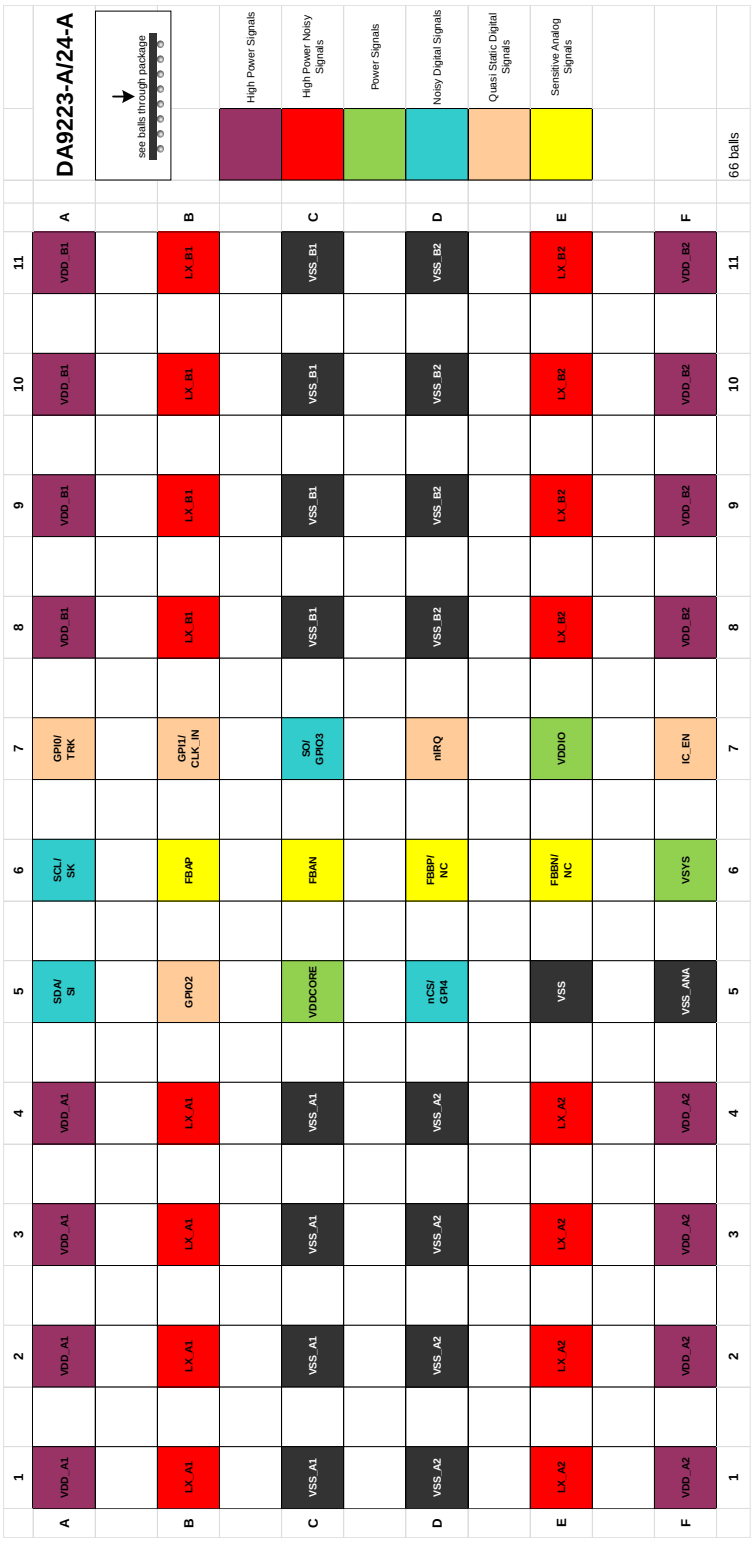


Figure 3: 66 TFBGA 0.8 mm Pitch Ball Map

Table 1: Pin Description

Pin Name	Signal Name	Second Function	Type (See Table 2)	Description
B1, B2, B3, B4	LX_A1		AO	Switching node for Buck A phase 1
E1, E2, E3, E4	LX_A2		AO	Switching node for Buck A phase 2
B8, B9, B10, B11	LX_B1		AO	Switching node for Buck B phase 1
E8, E9, E10, E11	LX_B2		AO	Switching node for Buck B phase 2
A1, A2, A3, A4	VDD_A1		PS	Supply voltage for Buck A phase 1 To be connected to VSYS
F1, F2, F3, F4	VDD_A2		PS	Supply voltage for Buck A phase 2 To be connected to VSYS
A8, A9, A10, A11	VDD_B1		PS	Supply voltage for Buck B phase 1 To be connected to VSYS
F8, F9, F10, F11	VDD_B2		PS	Supply voltage for Buck B phase 2 To be connected to VSYS
F7	IC_EN		DI	Integrated Circuit (IC) Enable Signal
D7	nIRQ		DO	Interrupt line towards the host
E7	VDDIO		PS	I/O Voltage Rail
B6	FBAP		AI	Positive sense node for Buck A
C6	FBAN		AI	Negative sense node for Buck A
D6	FBBP		AI	Positive sense node for Buck B of DA9224-A
	NC		AO	Do not connect for DA9223-A
E6	FBBN		AI	Negative sense node for Buck B of DA9224-A
	NC		AO	Do not connect for DA9223-A
A7	GPI0	TRK	DI/AI	General purpose input, input track
B7	GPI1		DI	General purpose input
B5	GPIO2		DIO	General purpose input/output
A5	SDA	SI	DIO	2-WIRE data, 4-WIRE data input/output
A6	SCL	SK	DI	2-WIRE clock, 4-WIRE clock
D5	nCS	GPI4	DI	4-WIRE chip select, general purpose input
C7	SO	GPIO3	DIO	4-WIRE data output, general purpose input/output
C5	VDDCORE		AO	Regulated supply for internal circuitry. Decouple with 150 nF (or 220 nF)
F6	VSYS		PS	Supply for IC and input for voltage supervision
E5	VSS		VSS	
F5	VSS_ANA		VSS	

Pin Name	Signal Name	Second Function	Type (See Table 2)	Description
C1, C2, C3, C4, D1, D2, D3, D4, C8, C9, C10, C11, D8, D9, D10, D11	VSS_A1, VSS_A2 VSS_B1 VSS_B2		VSS	Connect together

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital Input	AI	Analogue Input
DO	Digital Output	AO	Analogue Output
DIO	Digital Input/Output	AIO	Analogue Input/Output
PS	Power Supply	VSS	Ground

3 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions (Note 1)	Min	Typ	Max	Unit
T_{STG}	Storage temperature		-65		+150	°C
T_J	Junction temperature		-40		+150	°C
V_{DD_LIM}	Limiting supply voltage		-0.3		6.0	V
V_{PIN}	Limiting voltage at all pins except above		-0.3		V_{DD} + 0.3 (max 6.0)	V
V_{ESD_HBM}	Electrostatic discharge voltage	Human Body Model			2	kV

Note 1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions (Note 1)	Min	Typ	Max	Unit
V_{DD}	Supply voltage		2.8		5.5	V
T_{J_OP}	Operating junction temperature		-40		125	°C
T_A	Ambient temperature		-40		105	°C
V_{DDIO}	Input/output supply voltage		1.2		3.6 (Note 2)	V
P_{TOT}	Total power dissipation (Note 3)	TFBGA 0.8 mm pitch Derating factor above T_A = 70 °C: 29.3 mW/°C		1620		mW
θ_{JA}	Thermal resistance junction to ambient (Note 3)	TFBGA 0.8 mm pitch		34.2		°C/W

Note 1 Within the specified limits, a lifetime of 10 years is guaranteed. If operating outside of these recommended conditions, please consult with Dialog Semiconductor.

Note 2 V_{DDIO} is not allowed to be higher than V_{DD}.

Note 3 Obtained from measurement on a 6-layer evaluation board. Influenced by PCB technology and layout.

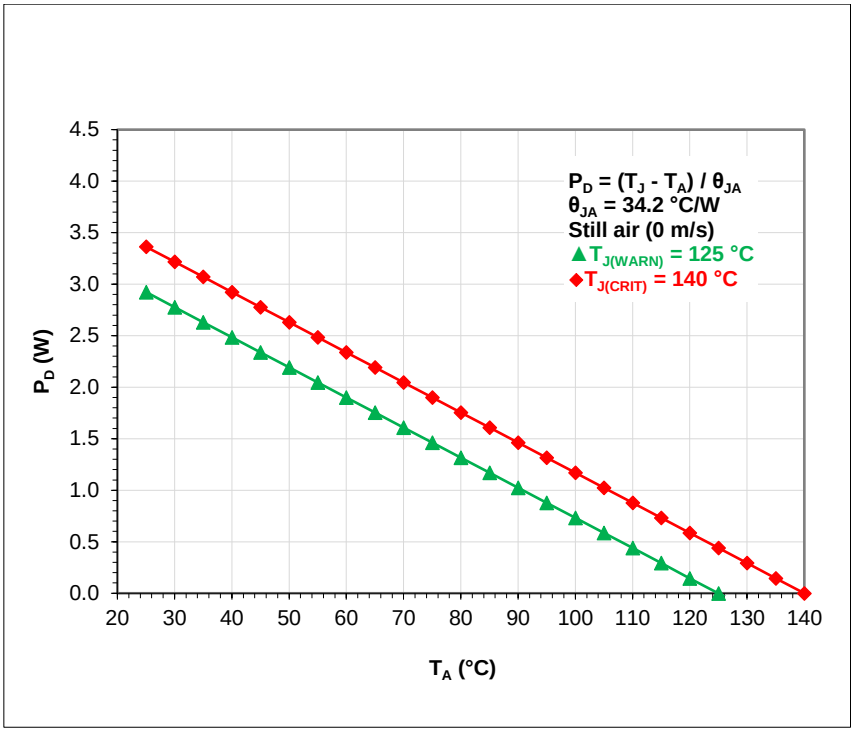


Figure 4: 66 TFBGA 0.8 mm Pitch Power Derating Curve

5 Electrical Characteristics

Unless otherwise noted, the following is valid for T_J = -40 to +125 ºC, V_{DD} = 2.8 V to 5.5 V, C_{OUT} = 47 µF per phase, local sensing.

Table 5: Buck Converters Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Component Electrical Conditions						
C_{OUT}	Output capacitance (per phase)	Including voltage and temperature coefficient	23	47	62	µF
ESR_{COUT}	Equivalent series resistance (per phase)	f > 100 kHz			10	mΩ
L_{PHASE}	Inductance (per phase)	Including current and temperature dependence	0.11	0.22	0.29	µH
DCR_{LPHASE}	Inductor resistance				100	mΩ
Electrical Characteristics						
V_{DD}	Supply voltage	VDD_x = VSYS	2.8		5.5	V
V_{BUCK}	Buck output voltage (Note 1)	I_O = 0 to I_{O_MAX}	0.3		1.57	V
V_{OACC}	Output voltage accuracy PWM mode	Incl. static line/load reg and voltage ripple V_{BUCK} ≥ 1 V	-2.0		+2.0	%
		Incl. static line/load reg and voltage ripple V_{BUCK} < 1 V		±20		mV
		V_{BUCK} = 1 V V_{DD} = 3.8 V no load	-1.0		+1.0	%
		V_{BUCK} = 1 V V_{DD} = 3.8 V no load T_A = 27 ºC	-0.5		+0.5	%
V_{TR_LOAD}	Load regulation transient voltage (Note 2)	DA9223-A I_O = 0 to 5 A, tr = 500 ns PWM 4-phase V_{BUCK} ≥ 1 V V_{BUCK} < 1 V		±2 ±20		% mV
		DA9223-A IO = 0 to 5 A, tr = 500 ns auto mode, ph shedding V_{BUCK} = 1 V		±3.5		%
	Load regulation transient voltage (Note 2)	DA9224-A I_O = 0 to 5 A, tr = 500 ns PWM 2-phase V_{BUCK} = 1 V		±3.5		%
V_{TR_LINE}	Line regulation transient voltage	V_{DD} = 3 to.3.6 V dt =10 µs I_O = IO(MAX)/2		15		mV
I_{O_MAX}	Maximum output current	Per phase	4000			mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{LIM_MIN}	Minimum current limit per phase (programmable) (Note 3)	BUCKA_ILIM BUCKB_ILIM = 0000	-20%	4000	20%	mA
I_{LIM_MAX}	Maximum current limit per phase (programmable) (Note 3)	BUCKA_ILIM BUCKB_ILIM = 1111	-20%	7000	20%	mA
I_{Q_PWM}	Quiescent current synchronous rectification mode	Per phase No load V_{DD} = 3.7 V		17		mA
f_{SW}	Switching frequency			3		MHz
t_{STUP}	Startup time	V_{OUT} = 1.0 V BUCKA_UP_CTRL BUCKB_UP_CTRL = 100		50 (Note 4)		µs
R_{O_PD}	Output pull-down resistance	For each phase at the LX node at 0.5 V, (see BUCKx_PD_DIS)		150	200	Ω
R_{ON_PMOS}	PMOS on-resistance	Incl. pin and routing V_{DD} = 3.7 V per phase		29		mΩ
R_{ON_NMOS}	NMOS on-resistance	Incl. pin and routing V_{DD} = 3.7 V per phase		21		mΩ
PFM Mode						
V_{BUCK_PFM}	Buck output voltage in PFM	I_O = 0 mA to I_{O_MAX}	0.3		1.57	V
I_{MIN_PFM}	Minimum output current in PFM	Static output voltage, no DVC	2			mA
$I_{Q\_PFM\_A2}$	DA9224-A quiescent current Buck A enabled	No switching V_{DD} = 3.7 V (Note 5)		58		µA
$I_{Q\_PFM\_A4}$	DA9223-A quiescent current Buck enabled	No switching V_{DD} = 3.7 V (Note 5)		72		µA
$I_{Q\_PFM\_A2B2}$	DA9224-A quiescent current Buck A enabled Buck B enabled	No switching V_{DD} = 3.7 V (Note 5)		106		µA

Note 1 Programmable in 10 mV increments.

Note 2 Additional to the dc accuracy. Inductor value 0.22 uH. The value is measured directly at $C_{OUT(EXT)}$. In case of remote sensing, parasitics of PCB and external components may affect this value.

Note 3 On-time > 50 ns.

Note 4 Time from beginning to end of the voltage ramp. Additional 10 µs typical delay, plus internal sync to the enable port.

Note 5 For the total quiescent current of the IC, the I_{DD_ON} should be added.

Table 6: IC Performance and Supervision

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{DD_OFF}	Off state supply current	IC_EN = 0 T_A = 27 °C		0.1	1	µA
I_{DD_ON}	On state supply current	IC_EN = 1 Buck A/B off T_A = 27 °C		14		µA
V_{TH_PG}	Power good threshold voltage	referred to VBUCK		-50		mV
V_{HYS_PG}	Power good hysteresis voltage			50		mV
$V_{TH\_UVLO\_VDD}$	Under voltage lockout threshold at VDD	BUCK_EN = 0		2.0		V
		BUCK_EN = 1		2.55		V
$V_{TH\_UVLO\_IO}$	Under voltage lockout threshold at VDDIO		1.315	1.45	1.55	V
$V_{HYS\_UVLO\_IO}$	Under voltage lockout hysteresis at VDDIO			70		mV
T_{TH_WARN}	Thermal warning threshold temperature		110	125	140	°C
T_{TH_CRIT}	Thermal critical threshold temperature		125	140	155	ºC
T_{TH_POR}	Thermal power on reset threshold temperature		135	150	165	°C
f_{OSC}	Internal oscillator frequency		-7%	6.0	+7%	MHz

Table 7: Digital I/O Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH_EN}	HIGH level input voltage at pin IC_EN		1.1			V
V_{IL_EN}	LOW level input voltage at pin IC_EN				0.35	V
t_{EN}	Enable time	I/F operating		750		µs
$R_{O\_PU\_GPO}$	Pull up resistor at GPO	V_{DDIO} = 1.8 V V_{GPO} = 0 V		100		kΩ
$R_{I\_PD\_GPI}$	Pull down resistor at GPI	V_{DDIO} = 1.8 V V_{GPI} = VDDIO		150		kΩ
V_{IH}	GPI0-4, SCL, SDA, (2-WIRE mode) HIGH level input voltage	VDDCORE mode VDDIO mode	1.75 0.7*V_{DDIO}			V
V_{IL}	GPI0-4, SCL, SDA, (2-WIRE mode) LOW level input voltage	VDDCORE mode VDDIO mode			0.75 0.3*V_{DDIO}	V
V_{IH_4WIRE}	SK, nCS, SI (4-WIRE Mode) HIGH level input voltage		0.7*V_{DDIO}			V
V_{IL_4WIRE}	SK, nCS, SI (4-WIRE Mode) LOW level input voltage				0.3*V_{DDIO}	V
V_{OH}	GPO2-3, SO (4-WIRE mode) HIGH level output voltage	push-pull mode at 1 mA V_{DDIO} ≥ 1.5 V	0.8*V_{DDIO}			V
V_{OL1}	GPO2-3, SDA (2-WIRE mode) SO (4-WIRE mode) LOW level output voltage at I_{OL} = 1 mA				0.3	V
V_{OL3}	SDA (2-WIRE Mode) LOW level output voltage at I_{OL} = 3 mA				0.24	V
V_{OL20}	SDA (2-WIRE Mode) LOW level output voltage at I_{OL} = 20 mA				0.4	V
C_{IN}	CLK, SDA (2-WIRE Mode) input capacitance			2.5	10	pF
t_{SP}	CLK, SDA (2-WIRE Mode) spike suppression pulse width	Fast/Fast+ mode High Speed mode	0 0		50 10	ns
t_{fDA}	Fall time of SDA signal (2-WIRE Mode)	Fast at C_B < 550 pF HS at 10 < C_B <100 pF HS at C_B < 400 pF	20+0.1 C_B 10 20		120 80 160	ns

Table 8: 2-WIRE Control Bus Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{BUF}	Bus free time from STOP to START condition		0.5			µs
C_B	Bus line capacitive load				150	pF
Standard/Fast/Fast+ Mode						
f_{SCL}	Clock frequency at pin SCL		0 (Note 1)		1000	kHz
t_{SU_STA}	START condition set-up time		0.26			µs
t_{H_STA}	START condition hold time		0.26			µs
t_{W_CL}	Clock LOW duration		0.5			µs
t_{W_CH}	Clock HIGH duration		0.26			µs
t_R	Rise time at pin CLK and DATA	Input requirement			1000	ns
t_F	Fall time at pin CLK and DATA	Input requirement			300	ns
t_{SU_D}	Data set-up time		50			ns
t_{H_D}	Data hold time		0			ns
High Speed Mode						
f_{SCL_HS}	Clock frequency at pin SCL		0 (Note 1)		3400	kHz
$t_{SU\_STA\_HS}$	START condition set-up time		160			ns
$t_{H\_STA\_HS}$	START condition hold time		160			ns
$t_{W\_CL\_HS}$	Clock LOW duration		160			ns
$t_{W\_CH\_HS}$	Clock HIGH duration		60			ns
t_{R_HS}	Rise time at pin CLK and DATA	Input requirement			160	ns
t_{F_HS}	Fall time at pin CLK and DATA	Input requirement			160	ns
$t_{SU\_D\_HS}$	Data set-up time		10			ns
$t_{H\_D\_HS}$	Data hold time		0			ns
$t_{SU\_STO\_HS}$	STOP condition set-up time		160			ns

Note 1 Minimum clock frequency is 10 kHz if 2WIRE_TO is enabled.

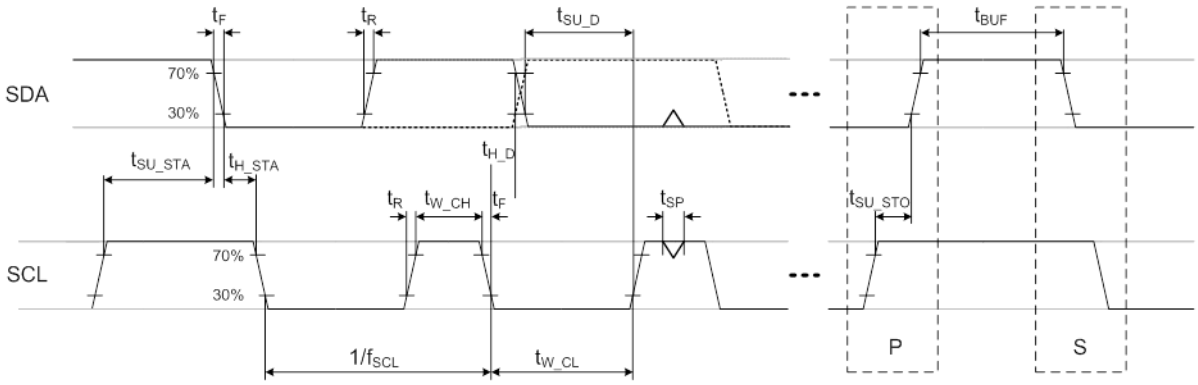


Figure 5: 2-WIRE Bus Timing

Table 9: 4-WIRE Control Bus Characteristics

Parameter	Description	Label in Plot	Min	Typ	Max	Unit
C_B	Bus line capacitive load				100	pF
t_C	Cycle time	1	70			ns
t_{SU_CS}	Chip select setup time	2, from CS active to first SK edge	20			ns
t_{H_CS}	Chip select hold time	3, from last SK edge to CS idle	20			ns
t_{W_CL}	Clock LOW duration	4	0.4 x t_C			ns
t_{W_CH}	Clock HIGH duration	5	0.4 x t_C			ns
t_{SU_SI}	Data input setup time	6	10			ns
t_{H_SI}	Data input hold time	7	10			ns
t_{V_SO}	Data output valid time	8			22	ns
t_{H_SO}	Data output hold time	9	6			ns
t_{W_CS}	Chip select HIGH duration	10	20			ns

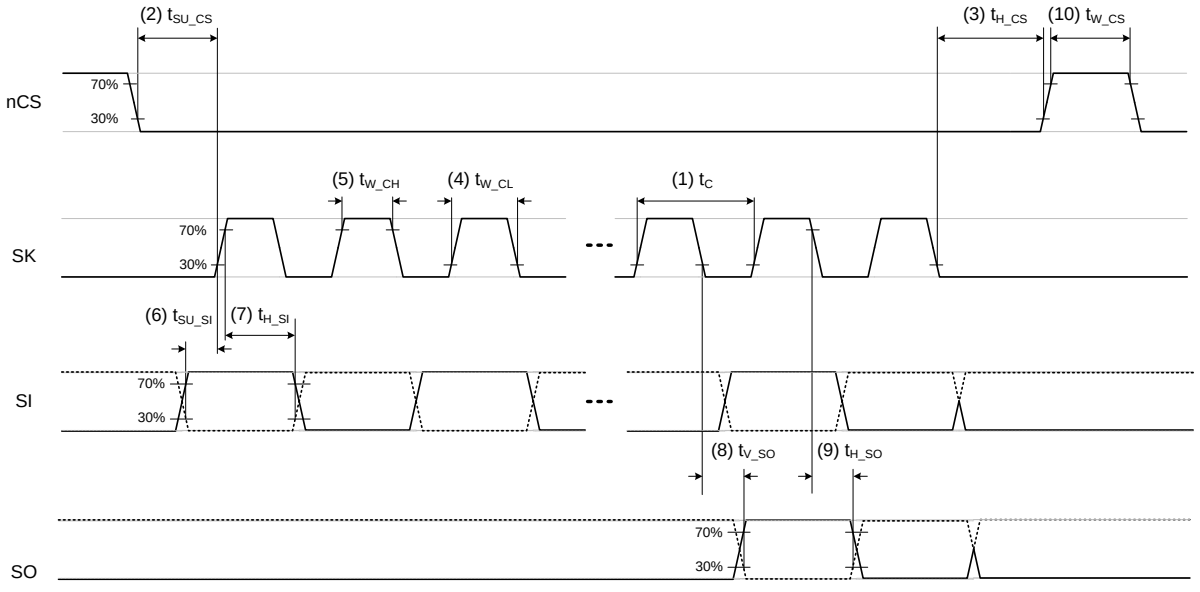


Figure 6: 4-WIRE Bus Timing

6 Efficiency Measurements

The efficiency measurements for DA9223-A and DA9224-A (in TFBGA 0.8 mm pitch package) are shown with phase shedding enabled in each plot and were measured using 2520 size inductor with typ. 8 mΩ DCR.

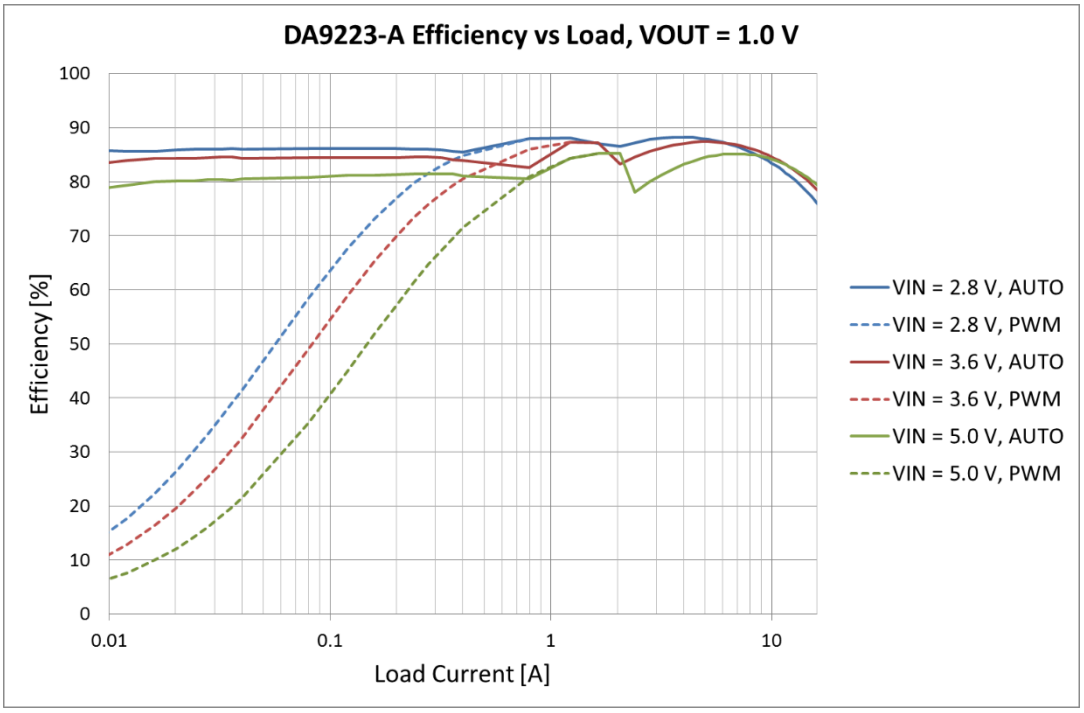


Figure 7: DA9223-A Efficiency vs Load, V_{OUT} = 1.0 V, 0-16 A

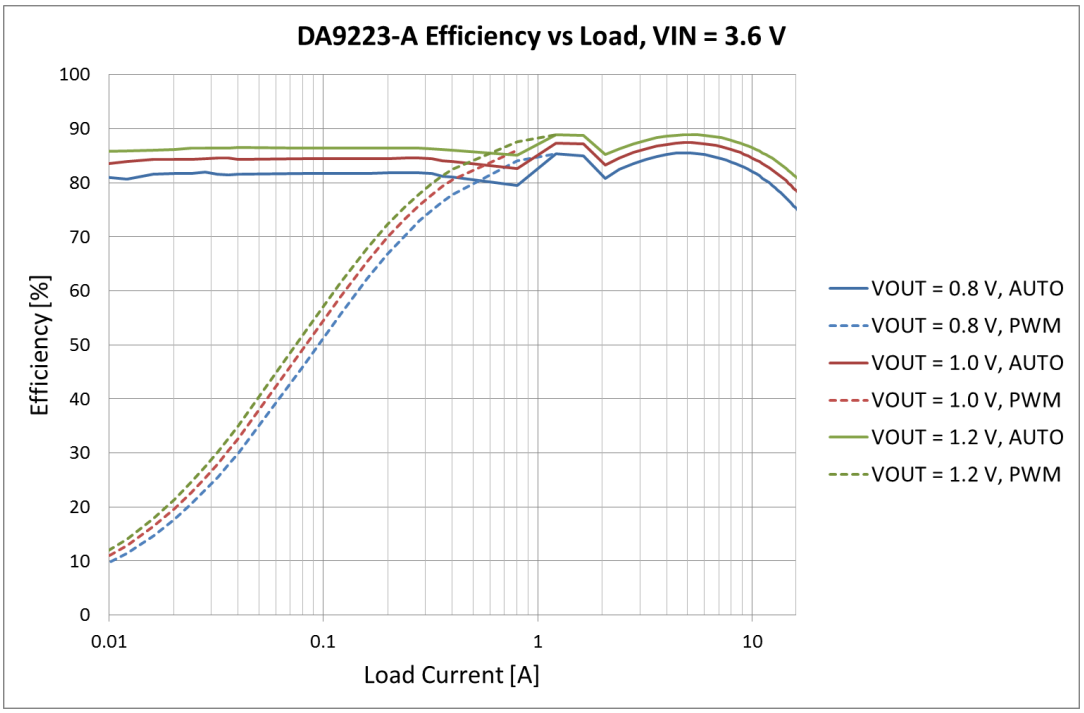


Figure 8: DA9223-A Efficiency vs Load, V_{IN} = 3.6 V, 0-16 A

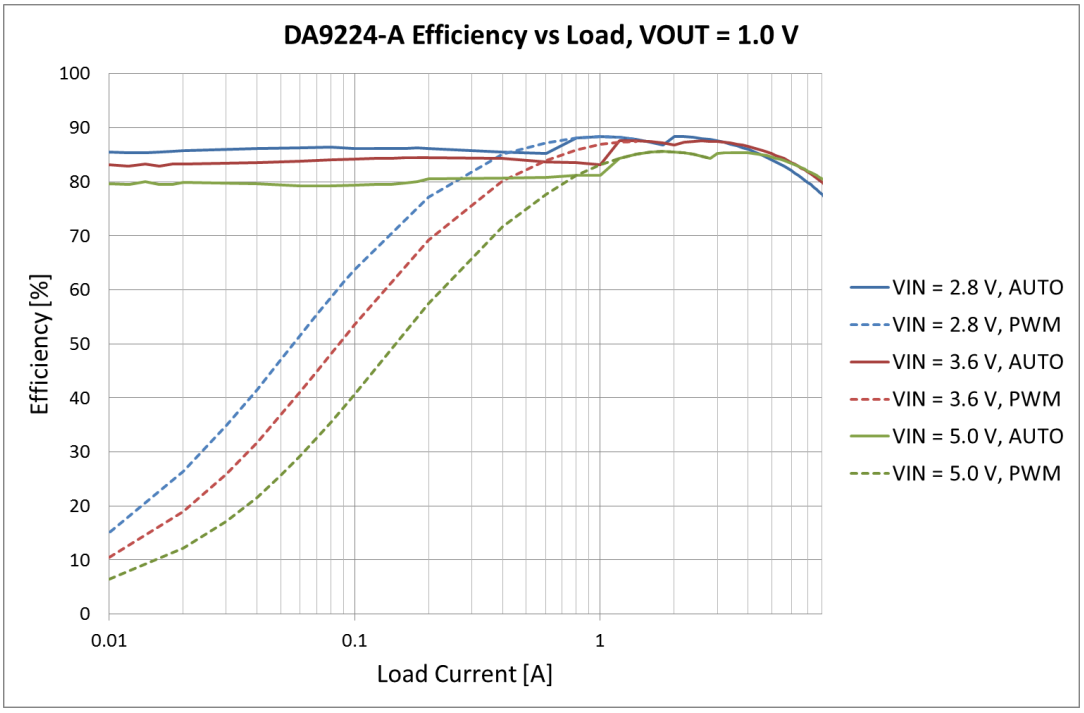


Figure 9: DA9224-A Efficiency vs Load, V_{OUT} = 1.0 V, 0-8 A

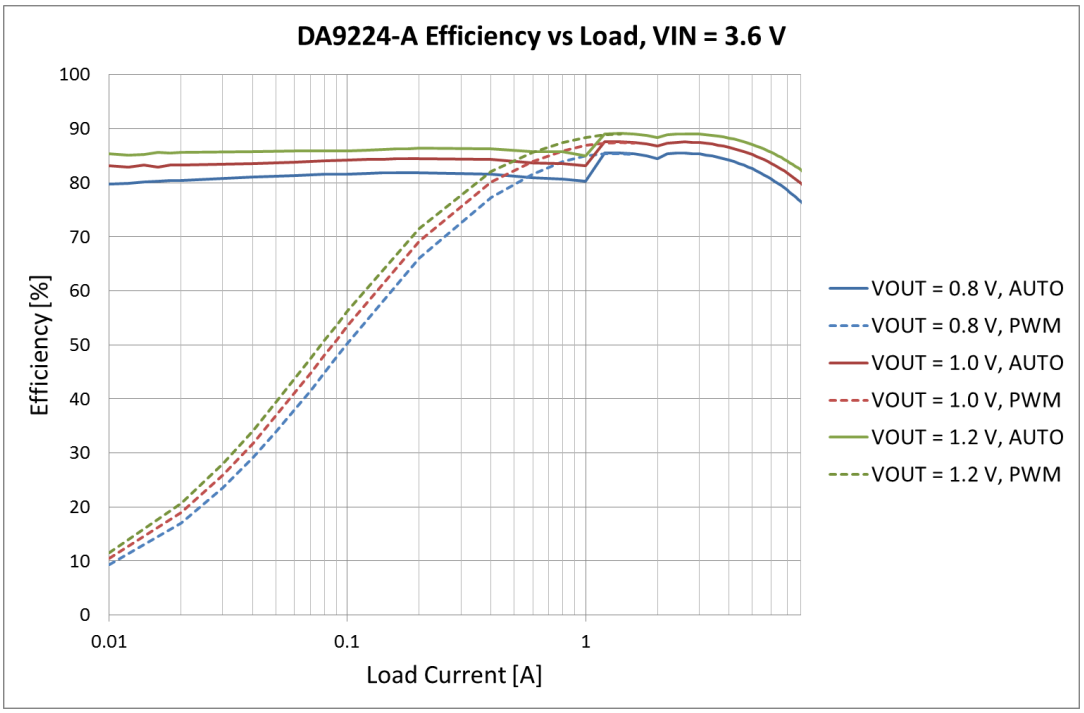


Figure 10: DA9224-A Efficiency vs Load, V_{IN} = 3.6 V, 0-8 A

7 Functional Description

Flexible configurability and the availability of different control schemes make both DA9223-A and DA9224-A the ideal single/dual buck companion ICs to expand the existing capabilities of a system PMIC such as DA9063.

Due to the advanced compatibility between both DA9223-A and DA9224-A and the DA9063, they offer several advantages when they are operated together. These advantages include:

- DA9223-A and DA9224-A can be enabled and controlled by DA9063 during the power up sequence, thanks to DA9063's dedicated output signals during power-up, and compatible input controls in both DA9223-A and DA9224-A.
- DA9223-A and DA9224-A can be used in a completely transparent way for the host processor and can share the same Control Interface (same SPI chip select or I^2C address), thanks to the compatible registers map. DA9223-A and DA9224-A have a dedicated register space for configuration and control which doesn't conflict with DA9063.
- DA9223-A and DA9224-A support a power-good configurable port for enhanced communication to the host processor and improved power-up sequencing.
- DA9223-A and DA9224-A can both share the same interrupt line with DA9063.

In addition, the 2-WIRE / 4-WIRE interfaces allow DA9223-A and DA9224-A to fit to many standard PMU parts and power applications.

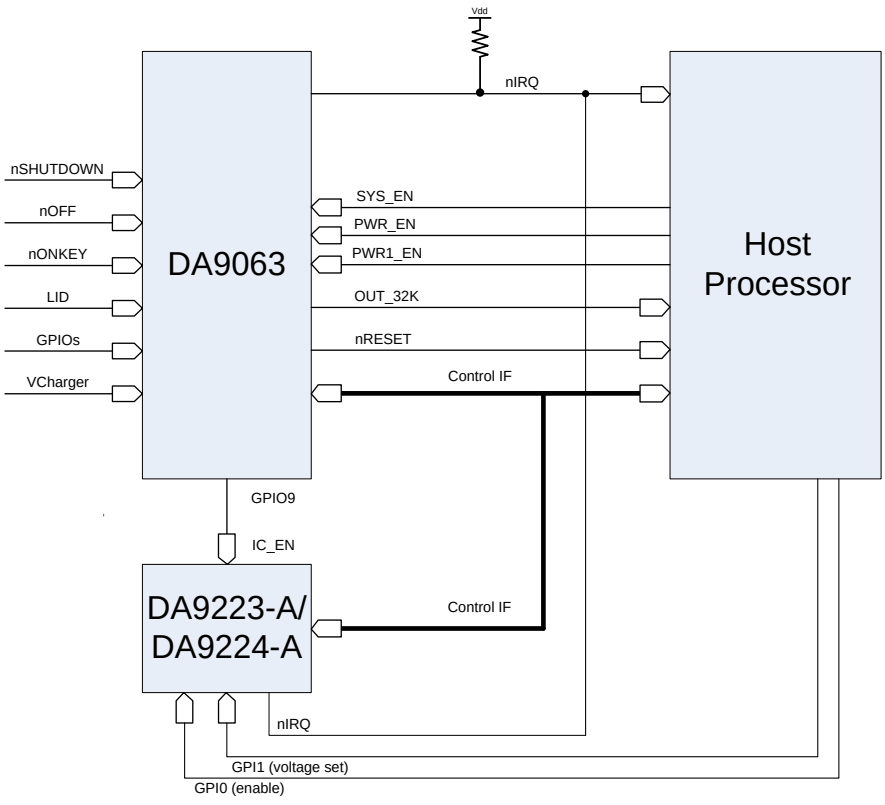


Figure 11: Interface of DA9223-A/24-A with DA9063 and the Host Processor

As shown in Figure 11, a typical application case includes a host processor, a main PMIC (for example, DA9063) and DA9223-A or DA9224-A used as companion IC for the high power core supply.

The easiest way of controlling DA9223-A and DA9224-A is through the Control Interface. The master initiating the communication must always be the host processor that reads and writes to the main PMIC, and to the DA9223-A and DA9224-A registers. To poll the status of DA9223-A or DA9224-A, the host processor must access the dedicated register area through the Control Interface. DA9223-A and DA9224-A can additionally be controlled by means of hardware inputs.

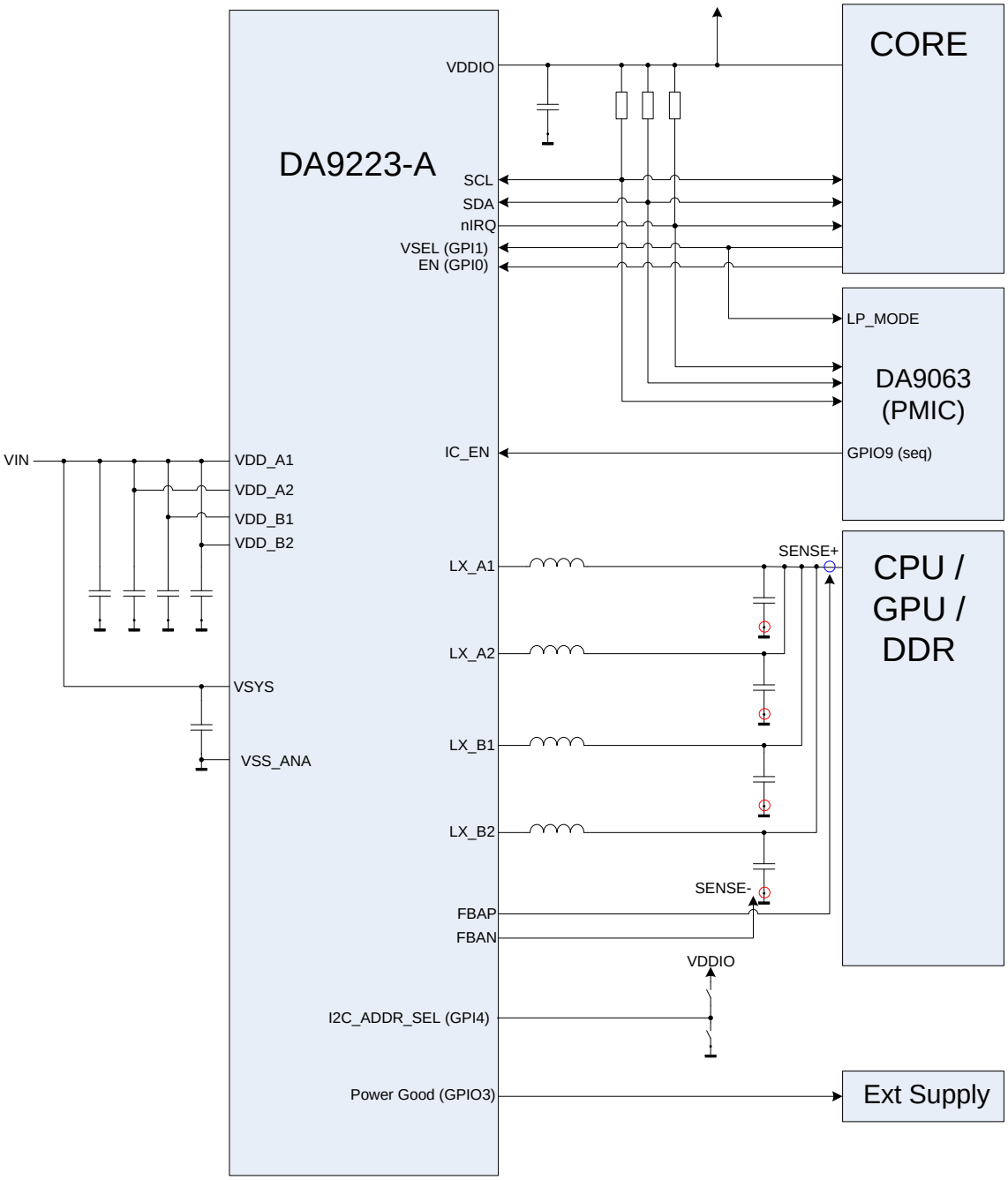


Figure 12: Typical Application of DA9223-A

Figure 12 shows a typical use case of DA9223-A for the supply of CPU, GPU, or DDR rails. The IC is enabled and disabled by the main PMIC via IC_EN port as part of its sequencer. Once the IC is enabled, the CORE application processor enables the buck converter with the EN1 signal and manages the output voltage selection with the VSEL signal.

The VSEL signal can be shared between the main PMIC and the DA9223-A. Three GPI/GPIOs embedded in DA9223-A are used in this case:

- GPIO2 signals the insertion of an external charger in the application (through interrupt to the host processor)
- GPIO3 indicates a power-good-condition, either to proceed with the power up sequence or to enable an external supply connected to the port
- GPI4 is used for the I^2C interface address hardware selection

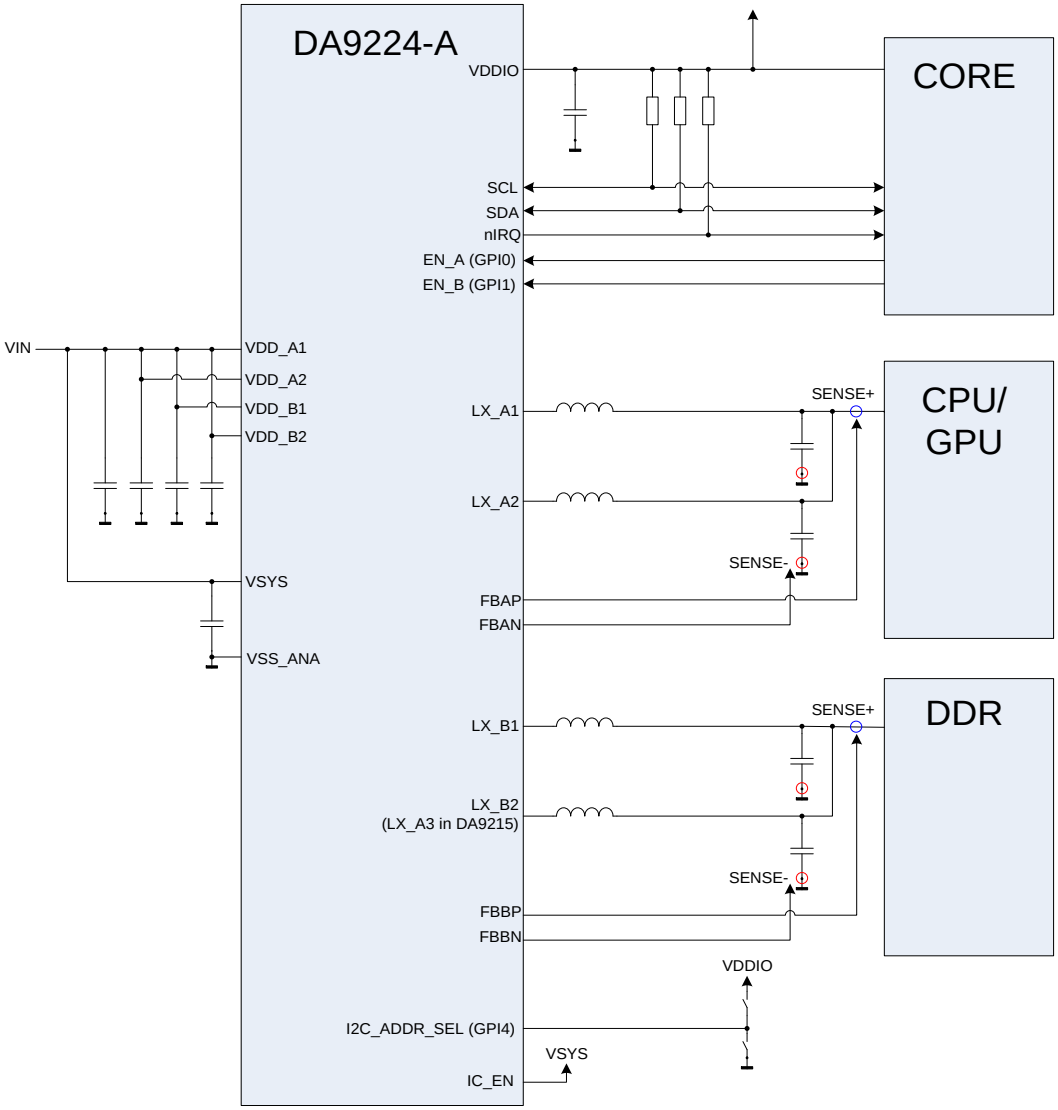


Figure 13: Typical Application of DA9224-A

Figure 13 shows a typical use case of DA9224-A for the simultaneous supply of a CPU and a GPU rail. The IC is always enabled because IC_EN is shorted to the battery voltage. The CORE application processor enables and disables the CPU/GPU and the DDR individually via dedicated ports on DA9224-A.

7.1 DC-DC Buck Converter

DA9223-A is a four-phase 16 A high efficiency synchronous step-down DVC regulator, operating at a high frequency of typically 3 MHz. It supplies an output voltage of typically 1.0 V for a CPU rail, configurable in the range 0.3 – 1.57 V, with high accuracy in steps of 10 mV.

DA9224-A contains two buck converters, Buck A and Buck B, each capable of delivering 8 A.

To improve the accuracy of the delivered voltage, each buck converter can support a differential se nsing of the configured voltage directly at the point of load via dedicated positive and negative sense pins.

Both Buck A and Buck B have two voltage registers each. One defines the normal output voltage, while the other offers an alternative retention voltage. In this way different application power modes can easily be supported. The voltage selection can be operated either via GPI or via control interface to guarantee the maximum flexibility according to the specific host processor status in the application.

When a buck is enabled, its output voltage is monitored and a power-good signal indicates that the buck output voltage has reached a level higher than the VTH(PG) threshold. The power-good is lost when the voltage drops below VTH(PG) - VHYS(PG), which is the level at which the signal is de-asserted. The power good signaling should not be used in conjunction with fast start up rates, configured in BUCKx_UP_CTRL register fields and can be individually masked during DVC transitions using the PGA_DVC_MASK and PGB_DVC_MASK bits. For each of the buck converters the status of the power-good indicator can be read back via I²C from the PWRGOOD_A and PWRGOOD_B status bits. It can be also individually assigned to either GPIO2 or GPIO3 using BUCKA_PG_SEL and BUCKB_PG_SEL. For correct functionality, the GPIO ports need to be configured as output. An I²C write in GPIOx_MODE can overwrite the internal configuration so that a new update will be automatically done only when the internal power-good indicator changes status.

The buck converters are capable of supporting DVC transitions that occur:

- When they are active and the selected A-voltage or B-voltage is updated to a new target value.
- When the voltage selection is changed from the A-voltage to the B-voltage (or B-voltage to the A-voltage) using VBUCKA_SEL and VBUCKB_SEL.

The DVC controller operates in Pulse Width Modulation (PWM) mode with synchronous rectification. When the host processor changes the output voltage, the voltage transition of each buck converter can be individually signaled with a READY signal routed to either GPIO2 or GPIO3. The port has to be configured as GPO and selected for the functionality via READYA_CONF or READYB_CONF. In contrast to the power-good signal, the READY only informs the host processor about the completion of the digital DVC ramp without confirming that the target voltage has actually been reached.

The slew rate of the DVC transition is individually programmed for each buck converter at 10mV per (4, 2, 1 or 0.5 µs) via control bit SLEW_RATE_A and SLEW_RATE_B.

The typical supply current in PWM mode is in the order of 17 mA per phase (quiescent current and charge/discharge current) and drops to <1 µA when the buck is turned off.

When the buck is disabled, a pull-down resistor (typically 150 Ω) for each phase is activated depending on the value stored in register bits BUCKA_PD_DIS and BUCKB_PD_DIS. Phases disabled using PHASE_SEL_A and PHASE_SEL_B will not have any pull-down. The pull-down resistor is always disabled at all phases when DA9223-A and DA9224-A are OFF.

7.1.1 Switching Frequency

The switching frequency is chosen to be high enough to allow the use of a small 0.22 µH inductor (see a complete list of coils in the Application Information, Section 9). The buck switching frequency can be tuned using register bit OSC_TUNE. The internal 6 MHz oscillator frequency is tuned in steps of 180 kHz. This impacts the buck converter frequency in steps of 90 kHz and helps to mitigate possible disturbances to other HF systems in the application.

7.1.2 Operation Modes and Phase Selection

The buck converters can operate in synchronous PWM mode and PFM mode. The operating mode is selected using register bits BUCKA_MODE and BUCKB_MODE.

An automatic phase shedding can be enabled for each buck converter in PWM mode via EF PH_SH_EN_A \h * MERGEFORMAT PH_SH_EN_A, PH_SH_EN_B, thereby automatically reducing or increasing the number of active phases depending on the output load current. For DA9224-A the phase shedding will automatically change between 1-phase and 2-phase operation at a typical current of 2.0 A. For DA9223-A the phase shedding will automatically change between 1-phase and 4-phase operation at a typical current of 2.5 A. The PHASE_SEL_A and PHASE_SEL_B register fields limit the maximum number of active phases under any conditions.

If the automatic operation mode is selected on BUCKA_MODE or BUCKB_MODE, the buck converters will automatically change between synchronous PWM mode and PFM depending on the load current. This improves the efficiency of the converters across the whole range of output load currents.

7.1.3 Output Voltage Selection

The switching converter can be configured using either a 2-WIRE or a 4-WIRE interface. For security reasons, the re-programming of registers that can cause damage when wrongly programmed (for example, the voltage settings) can be disabled by asserting the control V_LOCK. When V_LOCK is asserted, reprogramming the registers 0xD0 to 0x14F from control interfaces is disabled.

For each buck converter two output voltages can be pre-configured inside registers VBUCKA_A and VBUCKB_A, and registers VBUCKA_B and VBUCKB_B. The output voltage can be selected by either toggling register bits VBUCKA_SEL and VBUCKB_SEL or by re-programming the selected voltage control register. Both changes will result in ramped voltage transitions, during which the READY signal is asserted. After being enabled, the buck converter will by default use the register settings in VBUCKA_A and VBUCKB_A unless the output voltage selection is configured via the GPI port.

If “00” has been selected in BUCKA_MODE or BUCKB_MODE, A-/B- voltage selection registers VBUCKx_x control the operation of the PWM and PFM modes.

Regardless of the values programmed in the VBUCKx_A and VBUCKx_B registers, the registers VBUCKA_MAX, VBUCKB_MAX will individually limit the maximum output voltage that can be set for each of the buck converters.

The buck converter provides an optional hardware enable/disable via selectable GPI, and configured via control register bits BUCKA_GPI and BUCKB_GPI. A change of the output voltage controlled by the state of a GPI is enabled via control register bits VBUCKA_GPI and VBUCKB_GPI. A rising or falling edge at the related GPI, DA9223-A and DA9224-A will configure the buck converters according to the status of the GPI.

In addition to selecting between the A/B voltages, a track mode can be activated for Buck A to set the output voltage. In the DA9223-A, the track mode is applied to the 4-phase buck converter. This feature can be enabled on GPI0 via GPI0_PIN. The output voltage will be configured to follow the voltage applied at a selected GPI pin. The voltage applied at GPI0 must be in the same range as the nominal output voltage selectable for the buck rail (see VBUCKA_A and VBUCKA_B registers). In Track Mode, only single ended remote sensing is possible.

In Track Mode, the content of the VBUCKA_SEL bit is ignored, as well as VBUCKA_A and VBUCKA_B bits. They will become active again once the voltage track mode is disabled. The GPI0 does not generate any event in this case.

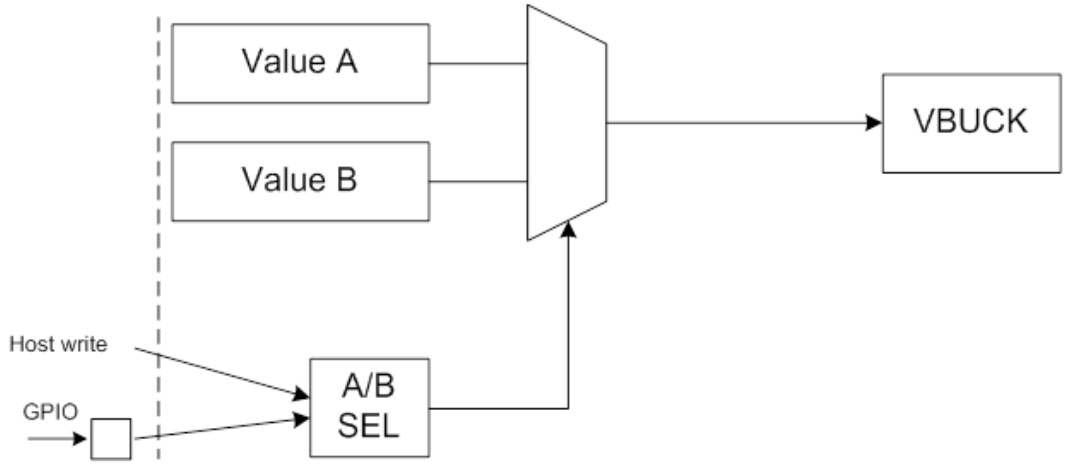


Figure 14: Concept of Control of the Buck’s Output Voltage

7.1.4 Soft Start Up

To limit in-rush current from VSYS, the buck converters can perform a soft-start after being enabled. The start-up behavior is a compromise between acceptable inrush current from the battery and turn-on time. In DA9223-A and DA9224-A different ramp times can be individually configured for each buck converter on register BUCKA_UP_CTRL and BUCKB_UP_CTRL. Rates higher than 20 mV/µs may produce overshoot during the start-up phase, so they should be considered carefully. It is also recommended to place a decoupling capacitor on the feedback lines if slow ramp-up slew rate; slower than 2.5 mV/µs is used.

A ramped power-down can be selected on register bits BUCKA_DOWN_CTRL and BUCKB_DOWN_CTRL. When no ramp is selected, the output node will only be discharged by the pull-down resistor, if enabled via BUCKA_PD_DIS and BUCKB_PD_DIS.

7.1.5 Current Limit

The integrated current limit is meant to protect DA9223-A and DA9224-A power stages and the external coil from excessive current. The bucks' current limit should be configured to be at least 40% higher than the required maximum continuous output current.

When reaching the current limit, each buck converter generates an event and an interrupt to the host processor unless the interrupt has been masked using the OCx_MASK controls. These OCA_MASK and OCB_MASK control bits can be used to mask the generation of over-current events during DVC transitions. An extra masking time as defined in OCx_MASK will be automatically added to the DVC interval after the DVC has finished in order to ensure that the possible high current levels needed for DVC do not influence the event generation.

7.1.6 Variable VOUT above 1.57 V

The whole product family is also available with an adjustable output voltage up to 4.3V. A resistive divider from VOUT to FBAN (or FBBN) can be used to set the output voltage higher than 1.57 V, see Figure 15.

The value of the output voltage VOUT is set by the selection of the resistive divider shown in equation 1. The total resistance of the divider resistors (R1+R2) should be less than 40 kΩ.

$$VOUT = \left(1 + \frac{R1}{R2}\right) \cdot VREF$$

Equation 1

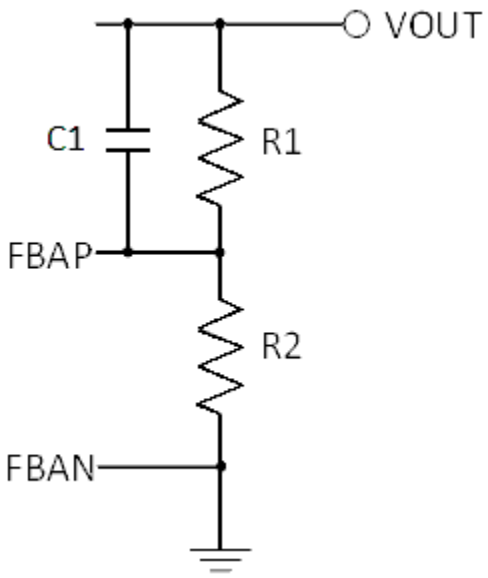


Figure 15: Resistive Divider from VOUT to FBAN

For example, to program the output voltage VOUT to 1.8 V, with VREF set to 1.2 V, suggest 10 kΩ on R1 and 20 kΩ on R2.

Note 1 The resistors need to be properly selected since the output voltage accuracy will be directly affected by any errors on the resistors. The voltage across FBAP and FBAN (VREF) is guaranteed, but not the output voltage accuracy.

Note 2 For best accuracy and tracking R1 = R2 and VREF is adjusted to be 1/2 x Vout.

Note 3 Capacitor C1 is used to provide feed forward control to improve transient response. The value of C1 should be between 1 nF and 10 nF.

CAUTION

The followings are important notes that need to be considered before using resistive divider on DA9223-A and DA9224-A:

1. Please contact your region's Dialog representative when adopting the resistive divider technique. Dialog need to prepare a special OTP because incorrect OTP settings may result in a different output voltage than expected.
2. The voltage difference between input voltage and output voltage needs to be: above 1.2 V, VIN-VOUT > 1.2 V.
3. The total resistance (R1+R2) is less than 40 kΩ.
4. It is recommended that the device is operated in PWM mode only.

7.2 Ports Description

This section describes the functionality of each input / output port.

7.2.1 VDDIO

VDDIO is an independent IO supply rail input to DA9223-A and DA9224-A that can be assigned to the power manager interface and to the GPIOs (see control PM_IF_V and GPI_V). The rail assignment determines the IO voltage levels and logical thresholds (see also the Digital I/O Characteristics in Table 7).

An integrated under voltage lockout circuit for the VDDIO prevents internal errors by disabling the I^2C communication when the voltage drops below VULO_IO. In that case the buck converters are also disabled and cannot be re-enabled (even via input port) until the VDDIO under-voltage condition has been resolved. At the exit of the VDDIO under voltage condition an event E_UVLO_IO is generated and the nIRQ line is driven active if the event is not masked.

The VDDIO under-voltage circuit monitors voltages relative to a nominal voltage of 1.8V. If a different rail voltage is being used, the under-voltage circuit can be disabled via UVLO_IO_DIS.

Note that the maximum speed at 4-WIRE interface is only available if the selected supply rail is greater than 1.6 V.

7.2.2 IC_EN

IC_EN is a general enable signal for DA9223-A and DA9224-A turning on and off the internal circuitry (for example, the reference, the digital core, etc.). Correct control of this port has a direct impact on the quiescent current of the whole application. A low level of IC_EN allows the device to reach the minimum quiescent current. The voltage at this pin is continuously sensed by a dedicated analogue circuit.

The host processor can begin to start communication with DA9223-A and DA9224-A through the Control Interface and, for example to turn on the buck converters, a delay time of t_{EN} after assertion of the IC_EN pin. If the bucks are enabled via OTP (see BUCKA_EN and BUCKB_EN controls), they will start up automatically after assertion of IC_EN.

The IC_EN activation threshold is defined with a built-in hysteresis to avoid glitching transitions that take place with unstable rising or falling edges.

7.2.3 nIRQ

The nIRQ port indicates that an interrupt-causing event has occurred and that the event/status information is available in the related registers. The nIRQ is an output signal that can either be push-pull or open drain (selected via IRQ_TYPE). If an active high IRQ signal is required, it can be achieved by asserting control IRQ_LEVEL (recommended for push-pull mode).

Examples of this type of information can be critical temperature and voltage, fault conditions, status changes at GPI ports, and so forth. The event registers hold information about the events that have occurred. Events are triggered by a status change at the monitored signals. When an event bit is set, the nIRQ signal is asserted unless this interrupt is masked by a bit in the IRQ mask register. The nIRQ will not be released until all event registers with asserted bits have been read and cleared. New events that occur during reading an event register are held until the event register has been cleared, ensuring that the host processor does not miss them.

7.2.4 GPIO Extender

DA9223-A and DA9224-A include a GPIO extender that offers up to five 5 V-tolerant general purpose input/output ports. Each port is controlled via registers from the host processor.

The GPIO3 and GPI4 ports are pin-shared with the 4-WIRE Control Interface. For instance, if GPIO3_PIN = 01, GPI4_PIN = 01 (Interface selected), the GPIO3 and GPI4 ports will be exclusively dedicated to output and chip-select signaling for 4-WIRE purposes. If the alternative function is selected, all GPIOs configuration as per registers 0x58 to 0x5A and 0x145 will be ignored.

GPIs are supplied from the internal rail VDDCORE or VDDIO (selected via GPI_V) and can be configured to be active high or active low (selected via GPIOx_TYPE). The input signals can be debounced or immediately change the state of the assigned status register GPIx to high or low, according to the setting of GPIOx_MODE. The debouncing time is configurable via control DEBOUNCE (10 ms default).

Whenever the status has changed to its configured active state (edge sensitive), the assigned event register is set and the nIRQ signal is asserted (unless this nIRQ is masked, see also Figure 16).

Whenever DA9223-A and DA9224-A is enabled and enters ON mode (also when enabled changing the setting of GPIOx_PIN) the GPI status bits are initiated towards their configured passive state. This ensures that already active signals are detected, and that they create an event immediately after the GPI comparators are enabled.

The buck enable signal (BUCKx_EN) can be controlled directly via a GPI, if so configured in the BUCKA_GPI and BUCKB_GPI registers. If it is required that GPI ports do not generate an event when configured for the HW control of the switching regulator, the relative mask bit should be set.

GPIs can alternatively be selected to toggle the VBUCKA_SEL and VBUCKB_SEL from rising and falling edges at these inputs. Apart from changing the regulator output voltage this also provides hardware control of the regulator mode (normal/low power mode) from the settings of BUCKA_SL_A, BUCKA_SL_B, BUCKB_SL_A, and BUCKB_SL_B (enabled if BUCKA_MODE or BUCKB_MODE = ‘00’).

All GPI ports have the additional option of activating a 100 kΩ pull-down resistor via GPIOx_PUPD, which ensures a well-defined level in case the input is not actively driven.

If enabled via ADDR_SEL_CONF, the I^2C address selection can be assigned to a specific GPI. An active voltage level at the selected GPI configures the slave address of DA9223-A and DA9224-A to IF_BASE_ADDR1 while a passive voltage level configures the slave address to IF_BASE_ADDR2. If no GPI is selected then the IF_BASE_ADDR1 is automatically used.

If defined as an output, GPIOs can be configured to be open-drain or push-pull. If configured as push-pull, the supply rail is VDDIO. By disabling the internal 120 kΩ pull-up resistor in open-drain mode, the GPO can also be supplied from an external rail. The output state will be assigned as configured by the GPIO register bit GPIOx_MODE.

A specific power-good port for each of the buck converters can be configured via BUCKA_PG_SEL and BUCKB_PG_SEL. The respective port must be configured as GPO for correct operation. If assigned to the same GPO, it is necessary that the power-good indicators for Buck A and Buck B are both active (supply voltages in range) to assert the overall power-good. The signal will be released as soon as one of the single power-good signals is not active (that is, at least one supply is out of range).

The power good signaling should not be used in conjunction with fast start up rates, configured in BUCKx_UP_CTRL register fields.

Once enabled via RELOAD_FUNC_EN the GPI0 can be used as input port to operate a partial OTP download. When the input level is changed to active, the registers 0x5D, 0x5E, 0xD1 to 0xDA are updated to their OTP default. This allows a complete buck re-configuration that resets all the changes done to those registers previously (soft reset). If the buck should be kept on during the soft reset, the OTP values for the enable bits should be asserted because they are also part of the re-load.

Whenever the GPIO unit is off (POR or OFF Mode) all ports are configured as open drain active high (pass device switched off, high impedance state). When leaving POR the pull-up or pull-down resistors will be configured from register GPIOx_PUPD.

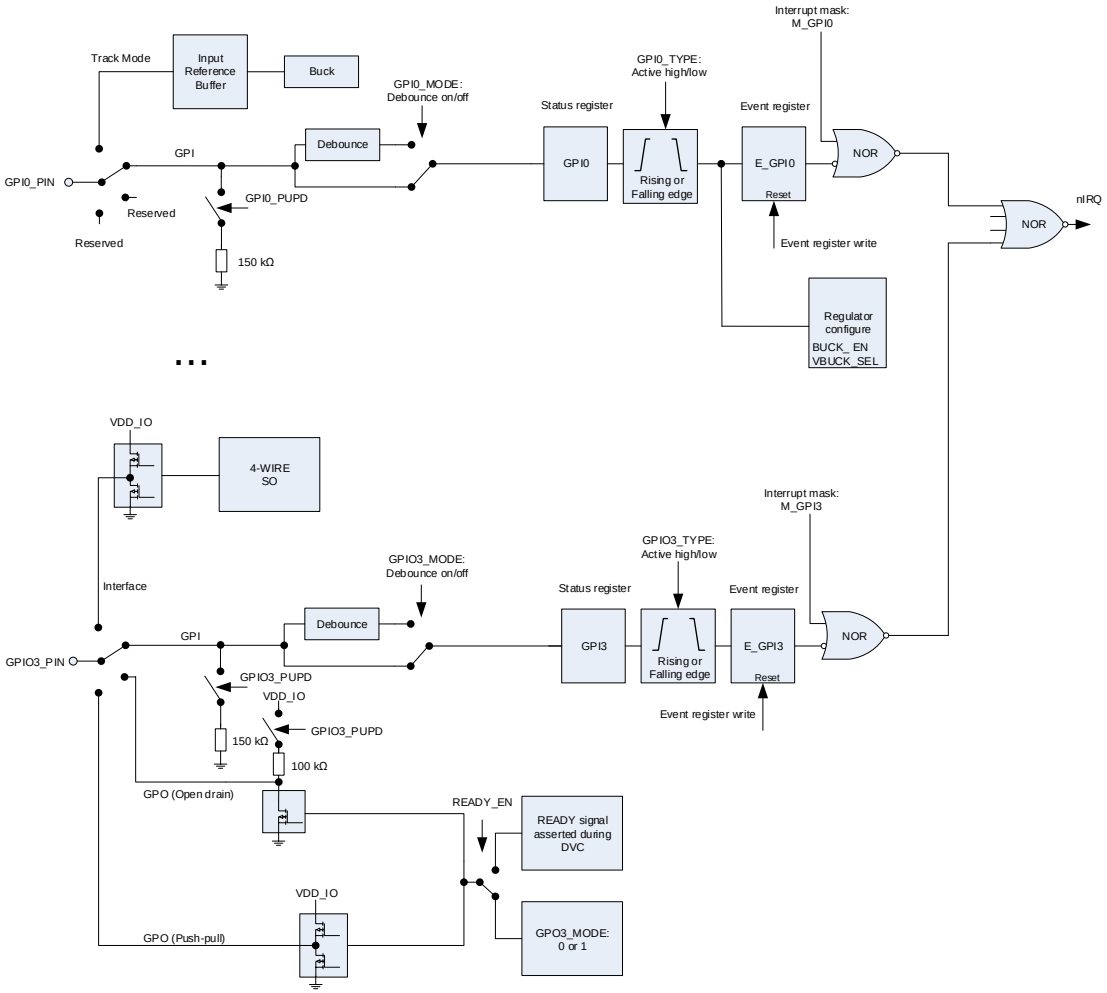


Figure 16: GPIO Principle of Operation (Example Paths)

7.3 Operating Modes

7.3.1 ON Mode

DA9223-A and DA9224-A are in ON Mode when the IC_EN port is higher than EN_ON and the supply voltage is higher than $V_{TH(UVLO)(VDD)}$. Once enabled, the host processor can start the communication with DA9223-A and DA9224-A via Control Interface after the t_{EN} delay needed for internal circuit start up.

If BUCKA_EN or BUCKB_EN is asserted when DA9223-A and DA9224-A are in ON Mode the power up of the related buck converter is initiated. If the bucks are controlled via GPI, the level of the controlling ports is checked when entering ON mode, so that an active level will immediately have effect on the buck. If BUCKA_EN or BUCKB_EN are not asserted and all controlling GPI ports are inactive, the buck converter will stay off with the output pull-down resistor enabled/disabled according to the setting of BUCKA_PD_DIS and BUCKB_PD_DIS.

7.3.2 OFF Mode

DA9223-A and DA9224-A are in OFF Mode when the IC_EN port is lower than EN_OFF. In OFF Mode, the bucks are always disabled and the output pull-down resistors are disabled independently of BUCKA_PD_DIS and BUCKB_PD_DIS. All I/O ports of DA9223-A and DA9224-A are configured as high impedance.

7.4 Control Interfaces

All the features of DA9223-A and DA9224-A can be controlled by SW through a serial control interfaces. The communication is selectable to be either a 2-WIRE (I^2C compliant) or a 4-WIRE connection (SPI compliant) via control IF_TYPE, which will be selected during the initial OTP read. If 4-WIRE is selected, the GPIO3 and GPI4 are automatically configured as interface pins. Data is shifted into or out of DA9223-A and DA9224-A under the control of the host processor, which also provides the serial clock. In a normal application case the interface is only configured once from OTP values, which are loaded during the initial start-up of DA9223-A and DA9224-A.

DA9223-A and DA9224-A react only on read/write commands where the transmitted register address (using the actual page bits as a MSB address range extensions) is within 0x50 to 0x67, 0xD0 to DF, 0x140 to 0x14F and (read only) 0x200 to 0x27F. Host access to registers outside these ranges will be ignored. This means there will be no acknowledge after receiving the register address in 2-WIRE Mode, and SO stays HI-Z in 4-WIRE Mode. During debug and production modes write access is available to page 4 (0x200 to 0x27F). DA9223-A and DA9224-A react only on write commands where the transmitted register address is 0x00, 0x80, 0x100 to0x106. The host processor must read the content of those registers before writing, thereby changing only the bit fields that are not marked as reserved (the content of the read back comes from the compatible PMIC, for example DA9063).

If the STAND_ALONE bit is asserted (OTP bit), DA9223-A and DA9224-A also react to read commands.

7.4.1 4-WIRE Communication

In 4-WIRE Mode the interface uses a chip-select line (nCS/nSS), a clock line (SK), data input (SI) and data output line (SO).

The DA9223-A and DA9224-A register map is split into four pages that each contain up to 128 registers. The register at address zero on each page is used as a page control register. The default active page after turn-on includes registers 0x50 to 0x6F. Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting bit REVERT. Unless the REVERT bit was asserted after modifying the active page, it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

All registers outside the DA9223-A and DA9224-A range are write only, that is, the DA9223-A and DA9224-A will not answer to a read command and the data bus is tri-state (they are implicitly directed to DA9063). In particular the information contained in registers 0x105 and 0x106 is used by

DA9223-A and DA9224-A to configure the control interface. They must be the same as the main PMIC (DA9063), so that a write to those registers configures both the main PMIC and DA9223-A and DA9224-A at the same time. The default OTP settings also need to be identical for a correct operation of the system.

The 4-WIRE interface features a half-duplex operation, that is, data can be transmitted and received within a single 16-bit frame at enhanced clock speed (up to 14 MHz). It operates at the clock frequencies provided by the host.

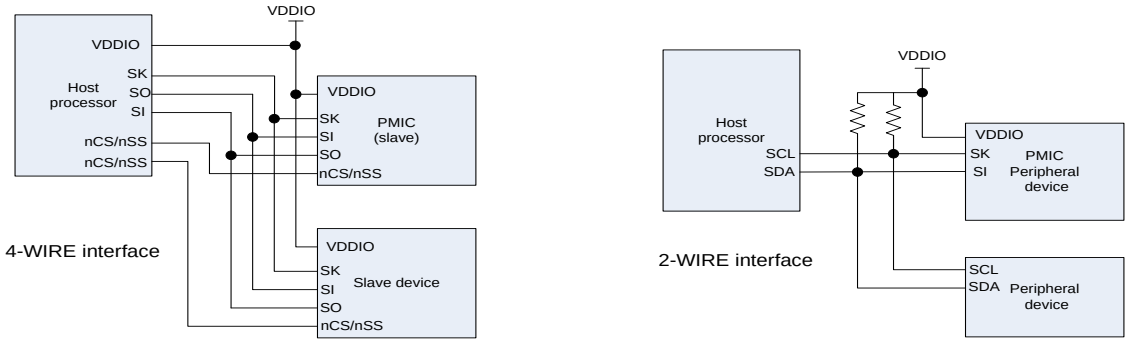


Figure 17: Schematic of 4-WIRE and 2-WIRE Power Manager Bus

A transmission begins when initiated by the host. Reading and writing is accomplished by the use of an 8-bit command, which is sent by the host prior to the exchanged 8-bit data. The byte from the host begins shifting in on the SI pin under the control of the serial clock SK provided from the host. The first seven bits specify the register address (0x01 to 0x07) that will be written or read by the host. The register address is automatically decoded after receiving the seventh address bit. The command word ends with an R/W bit, which together with the control bit R/W_POL specifies the direction of the following data exchange. During register writing the host continues sending out data during the following eight SK clocks. For reading, the host stops transmitting and the 8-bit register is clocked out of DA9223-A and DA9224-A during the consecutive eight SK clocks of the frame. Address and data are transmitted with MSB first. The polarity (active state) of nCS is defined by control bit nCS_POL. nCS resets the interface when inactive and it has to be released between successive cycles.

The SO output from DA9223-A and DA9224-A is normally in high-impedance state and active only during the second half of read cycles. A pull-up or pull-down resistor may be needed at the SO line if a floating logic signal can cause unintended current consumption inside other circuits.

Table 10: 4-WIRE Clock Configurations

Configurations			
CPHA **Clock Polarity**	CPOL **Clock Phase**	**Output Data is Updated at SK Edge**	**Input Data is Registered at SK Edge**
0 (idle low)	0	Falling	Rising
0 (idle low)	1	Rising	Falling
1 (idle high)	0	Rising	Falling
1 (idle high)	1	Falling	Rising

DA9223-A and DA9224-A's 4-WIRE interface offers two further configuration bits. Clock polarity (CPOL) and clock phase (CPHA) define when the interface will latch the serial data bits. CPOL determines whether SK idles high (CPOL = 1) or low (CPOL = 0). CPHA determines on which SK edge data is shifted in and out. With CPOL = 0 and CPHA = 0, DA9223-A and DA9224-A latch data on the SK rising edge. If the CPHA is set to 1 the data is latched on the SK falling edge. CPOL and CPHA states allow four different combinations of clock polarity and phase. Each setting is incompatible with the other three. The host and DA9223-A and DA9224-A must be set to the same CPOL and CPHA states to communicate with each other.

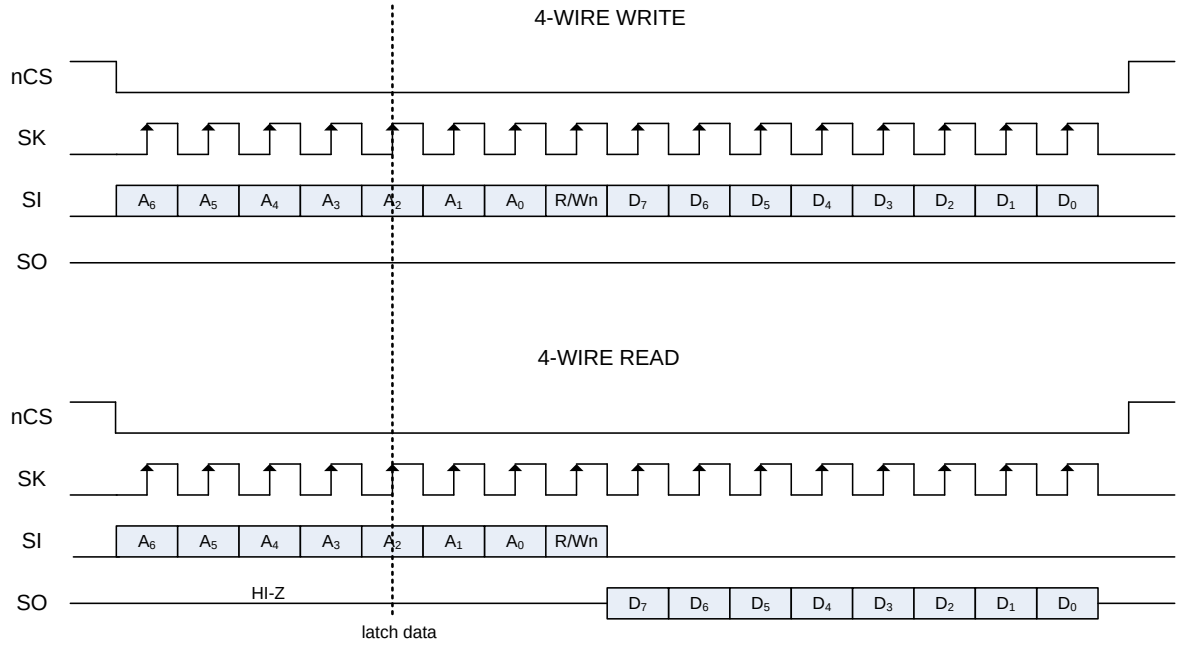


Figure 18: 4-WIRE Host Write and Read Timing (nCS_POL = '0', CPOL = '0', CPHA = '0')

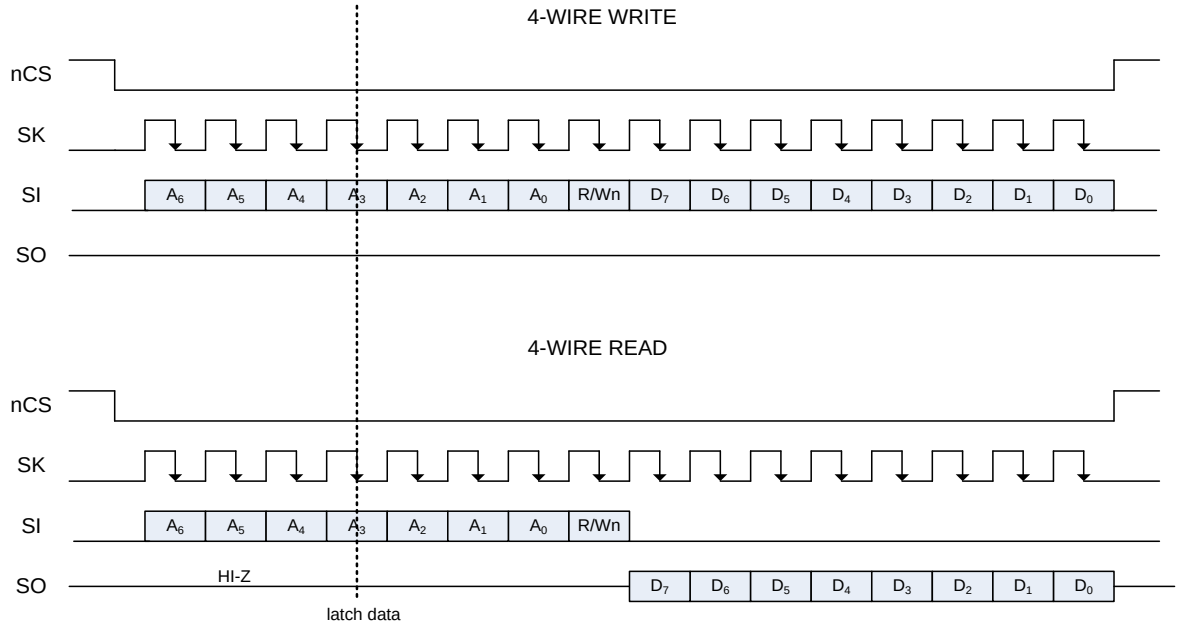


Figure 19: 4-WIRE Host Write and Read Timing (nCS_POL= '0', CPOL = '0', CPHA = '1')

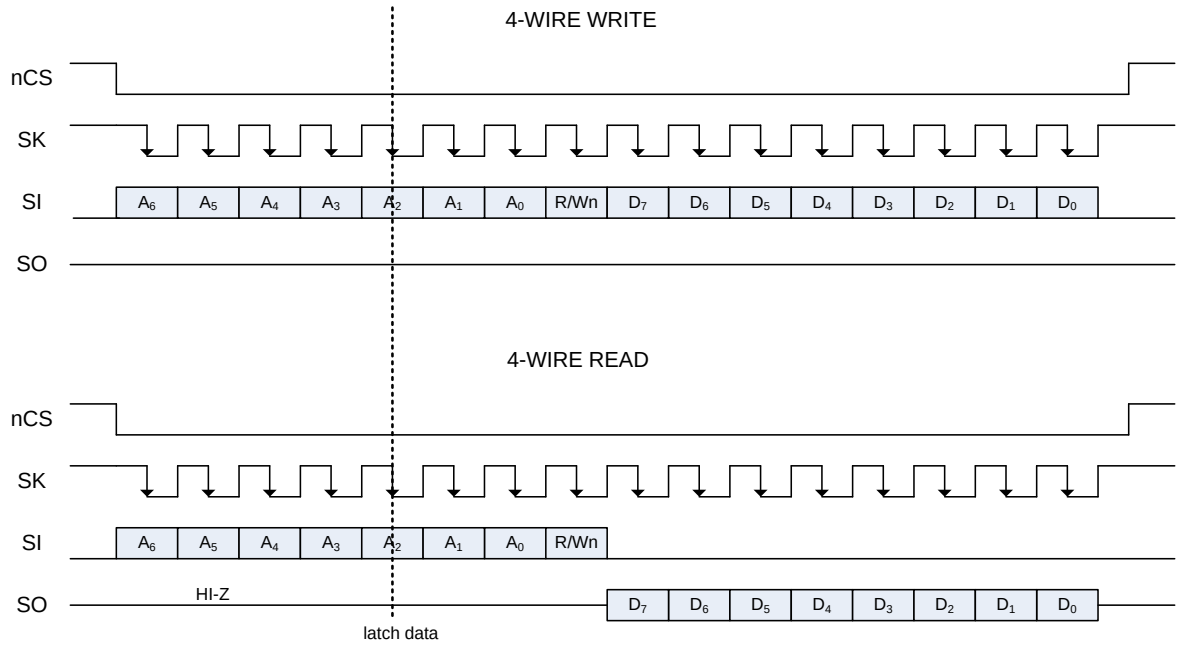


Figure 20: 4-WIRE Host Write and Read Timing (nCS_POL = '0', CPOL = '1', CPHA = '0')

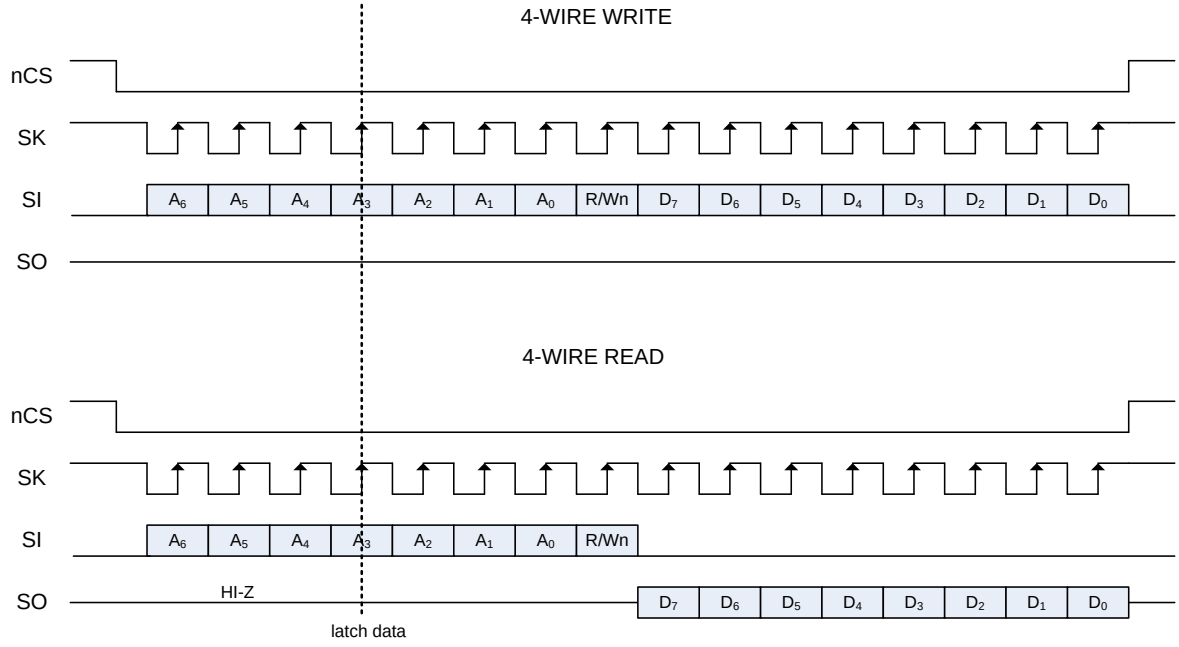


Figure 21: 4-WIRE Host Write and Read Timing (nCS_POL = '0', CPOL = '1', CPHA = '1')

Table 11: 4-WIRE Interface Summary

Parameters		
Signal Lines	nCS	Chip select
	SI Serial input data	Master out Slave in
	SO Serial output data	Master in Slave out
	SK	Transmission clock
Interface	Push-pull with tristate	
Supply voltage	Selected from VDDIO	1.6 V to 3.3 V
Data rate	Effective read/write data	Up to 7 Mbps
Transmission	Half-duplex	MSB first
	16 bit cycles	7-bit address, 1 bit read/write, 8-bit data
Configuration	CPOL	Clock polarity
	CPHA	Clock phase
	nCS_POL	nCS is active low/high

Note that reading the same register at high clock rates directly after writing it does not guarantee a correct value. It is recommended to keep a delay of one frame until re-accessing a register that has just been written (for example, by writing/reading another register address in between).

7.4.2 2-WIRE Communication

The IF_TYPE bit in the INTERFACE2 register can be used to configure the DA9223-A and DA9224-A control interface as a 2-WIRE serial data interface. In this case the GPIO3 and GPI4 are free for regular input/output functions. DA9223-A and DA9224-A has a configurable device write address (default: 0xD0) and a configurable device read address (default: 0xD1). See control IF_BASE_ADDR1 for details of configurable addresses. The ADDR_SEL_CONF bit is used to configure the device address as IF_BASE_ADDR1 or IF_BASE_ADDR2 depending on the voltage level applied at a configurable GPI port (see Section 7.2.4).

The SK port functions as the 2-WIRE clock and the SI port carries all the power manager bi-directional 2-WIRE data. The 2-WIRE interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled HIGH by external pull-up resistors (in the 2 kΩ to 20 kΩ range). The attached devices only drive the bus lines LOW by connecting them to ground. As a result two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and does not have any relation to the DA9223-A and DA9224-A internal clock signals. DA9223-A and DA9224-A will follow the host clock speed within the described limitations, and does not initiate any clock arbitration or slow down. An automatic interface reset can be triggered using control 2WIRE_TO if the clock signal stops to toggle for more than 35 ms.

The interface supports operation compatible to Standard, Fast, Fast-Plus and High Speed mode of the I^2C-bus specification Rev 4. Operation in high speed mode at 3.4 MHz requires mode changing in order to set spike suppression and slope control characteristics to be compatible with the I^2C-bus specification. The high speed mode can be enabled on a transfer by transfer basis by sending the master code (0000 1XXX) at the beginning of the transfer. DA9223-A and DA9224-A do not make use of clock stretching, and deliver read data without additional delay up to 3.4 MHz.

Alternatively, PM_IF_HSM configures the interface to use high speed mode continuously. In this case, the master code is not required at the beginning of every transfer. This reduces the communication overhead on the bus but limits the slaves attachable to the bus to compatible devices.

The communication on the 2-WIRE bus always takes place between two devices, one acting as the master and the other as the slave. The DA9223-A and DA9224-A will only operate as a SLAVE.

In contrast to the 4-WIRE mode, the 2-WIRE interface has direct access to two pages of the register map (up to 256 addresses). The register at address zero on each page is used as a page control register (with the 2-WIRE bus ignoring the LSB of control REG_PAGE). Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting control REVERT. Unless REVERT was asserted after modifying the active page, it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

In 2-WIRE operation DA9223-A and DA9224-A offer an alternative way to access register page 2 and page 3. It removes the need for preceding page selection writes by incrementing the device write/read address by one (default 0xD2/0xD3) for any direct access of page 2 and page 3 (page 0 and 1 access requires the basic write/read device address with the MSB of REG_PAGE to be '0').

7.4.3 Details of the 2-WIRE Control Bus Protocol

All data is transmitted across the 2-WIRE bus in groups of eight bits. To send a bit the SDA line is driven towards the intended state while the SCL is LOW (a low on SDA indicates a zero bit). Once the SDA has settled, the SCL line is brought HIGH and then LOW. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one byte for address and one byte data. Data and address transfer are transmitted MSB first for both read and write operations. All transmissions begin with the START condition from the master while the bus is in IDLE state (the bus is free). It is initiated by a high to low transition on the SDA line while the SCL is in the high state (a STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state).

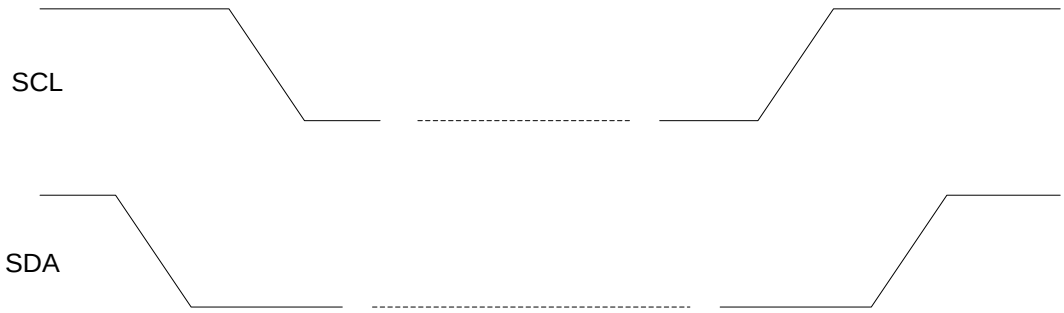


Figure 22: Timing of 2-WIRE START and STOP Condition

The 2-WIRE bus is monitored by DA9223-A and DA9224-A for a valid SLAVE address whenever the interface is enabled. It responds immediately when it receives its own slave address. The acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with 'A' in Figure 23 to Figure 27).

The protocol for a register write from master to slave consists of a start condition, a slave address with read/write bit and the 8-bit register address followed by eight bits of data terminated by a STOP condition. DA9223-A and DA9224-A respond to all bytes with Acknowledge. This is illustrated in Figure 23.

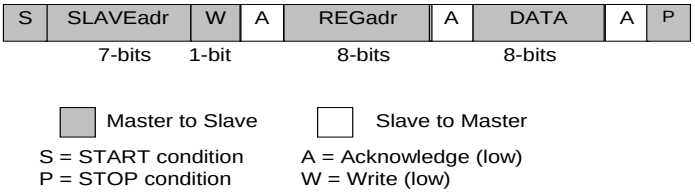


Figure 23: 2-WIRE Byte Write (SDA Line)

When the host reads data from a register it first has to write to DA9223-A and DA9224-A with the target register address and then read from DA9223-A and DA9224-A with a Repeated START or alternatively a second START condition. After receiving the data, the host sends No Acknowledge and terminates the transmission with a STOP condition. This is illustrated in Figure 24.

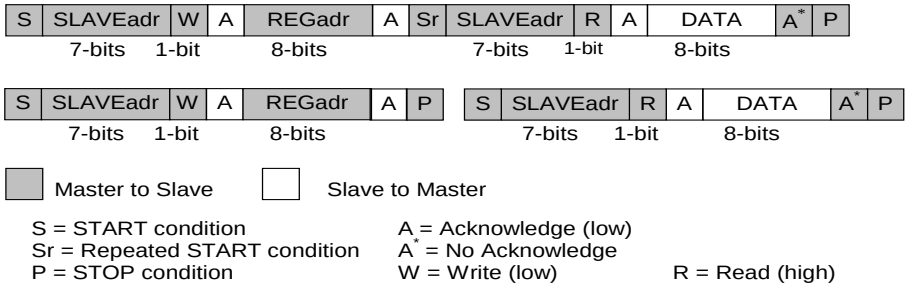


Figure 24: Examples of 2-WIRE Byte Read (SDA Line)

Consecutive (page) read out mode is initiated from the master by sending an Acknowledge instead of Not acknowledge after receipt of the data word. The 2-WIRE control block then increments the address pointer to the next 2-WIRE address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a Not acknowledge directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent 2-WIRE address is read out, the DA9223-A and DA9224-A will return code zero. This is illustrated in Figure 25.

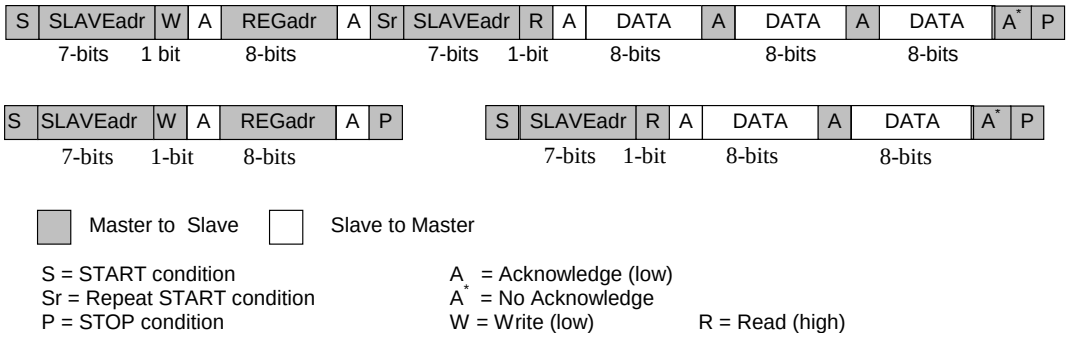


Figure 25: Examples of 2-WIRE Page Read (SDA Line)

Note that the slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the Master sends several data bytes following a slave register address. The 2-WIRE control block then increments the address pointer to the next 2-WIRE address, stores the received data and sends an Acknowledge until the master sends the STOP condition. This is illustrated in Figure 26.

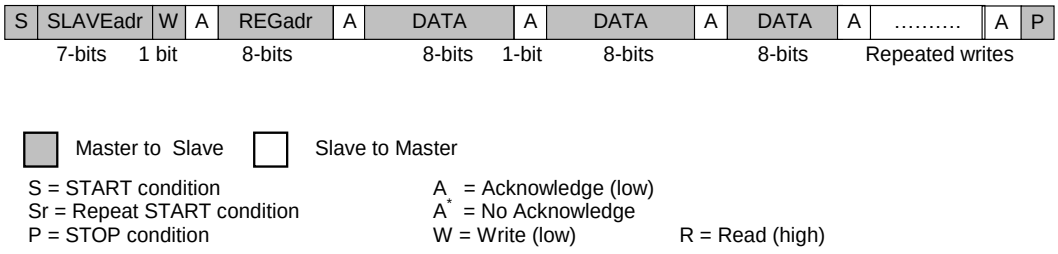


Figure 26: 2-WIRE Page Write (SDA Line)

Via control WRITE_MODE an alternate write mode can be configured. Register addresses and data are sent in alternation like in Figure 27 to support host repeated write operations that access several non-consecutive registers. Data will be stored at the previously received register address.

An update of WRITE_MODE cannot be done without interruption within a transmission frame. Thus, if not previously selected or not set as OTP default, the activation of Repeated Write must be done with a regular write on WRITE_MODE followed by a stop condition. The next frame after a start condition can be written in Repeated Write.

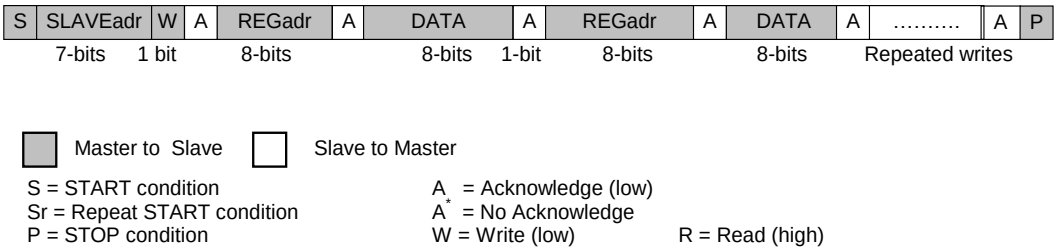


Figure 27: 2-WIRE Repeated Write (SDA Line)

If a new START or STOP condition occurs within a message, the bus will return to IDLE-mode.

7.5 Internal Temperature Supervision

To protect DA9223-A and DA9224-A from damage due to excessive power dissipation, the internal temperature is continuously monitored. There are three temperature thresholds:

Table 12: Over-Temperature Thresholds

Temperature Threshold	Typical Temperature Setting	Interrupt Event	Status Bit	Masking Bit
TEMP_WARN	125 °C	E_TEMP_WARN	TEMP_WARN	M_TEMP_WARN
TEMP_CRIT	140 °C	E_TEMP_CRIT	TEMP_CRIT	M_TEMP_CRIT
TEMP_POR	150 °C			

When the junction temperature reaches the TEMP_WARN threshold, DA9223-A and DA9224-A will assert the bit TEMP_WARN and will generate the event E_TEMP_WARN. If not masked using bit M_TEMP_WARN, the output port nIRQ will be asserted. The status bit TEMP_WARN will remain asserted as long as the junction temperature remains higher than TEMP_WARN.

When the junction temperature increases further to TEMP_CRIT, DA9223-A and DA9224-A will immediately disable the buck converter, assert the bit TEMP_CRIT, and will generate the event E_TEMP_CRIT. If not masked via bit M_TEMP_CRIT, the output port nIRQ will be asserted. The status bit TEMP_CRIT will remain asserted as long as the junction temperature remains higher than TEMP_CRIT. The buck converter will be kept disabled as long as the junction temperature is above TEMP_CRIT. It will not be automatically re-enabled even after the temperature drops below the valid threshold (even if the controlling GPI is asserted). A direct write into BUCKA_EN or BUCKB_EN, or a toggling of the controlling GPI, is needed to enable the buck converter.

Whenever the junction temperature exceeds TEMP_POR, a power on reset to the digital core is immediately asserted, which will stops all functionalities of DA9223-A and DA9224-A. This is needed to prevent possible permanent damage in the case of a rapid temperature increase.

8 Register Definitions

8.1 Register Map

Table 13 displays the register map, where all bits loaded from OTP are marked in bold.

Table 13: Register Map

Addr	Function	7	6	5	4	3	2	1	0
Register Page 0									
0x00	PAGE_CON	REVERT	WRITE_MODE	Reserved	Reserved	Reserved	REG_PAGE		
0x50	STATUS_A	Reserved	Reserved	Reserved	GPI4	GPI3	GPI2	GPI1	GPI0
0x51	STATUS_B	RAMP_READY_B	RAMP_READY_A	OV_CURR_B	OV_CURR_A	TEMP_CRIT	TEMP_WARN	PWRGOOD_B	PWRGOOD_A
0x52	EVENT_A	Reserved	E_UVLO_IO	Reserved	E_GPI4	E_GPI3	E_GPI2	E_GPI1	E_GPI0
0x53	EVENT_B	Reserved	Reserved	E_OV_CURR_B	E_OV_CURR_A	E_TEMP_CRIT	E_TEMP_WARN	E_PWRGOODB	E_PWRGOOD_A
0x54	MASK_A	Reserved	M_UVLO_IO	Reserved	M_GPI4	M_GPI3	M_GPI2	M_GPI1	M_GPI0
0x55	MASK_B	Reserved	Reserved	M_OV_CURR_B	M_OV_CURR_A	M_TEMP_CRIT	M_TEMP_WARN	M_PWRGOOD_B	M_PWRGOOD_A
0x56	CONTROL_A	V_LOCK	SLEW_RATE_B		SLEW_RATE_A		DEBOUNCING		
0x58	GPI0-1	GPI1_MODE	GPI1_TYPE	GPI1_PIN		GPI0_MODE	GPI0_TYPE	GPI0_PIN	
0x59	GPIO2-3	GPIO3_MODE	GPIO3_TYPE	GPIO3_PIN		GPIO2_MODE	GPIO2_TYPE	GPIO2_PIN	
0x5A	GPI4	Reserved	Reserved	Reserved		GPI4_MODE	GPI4_TYPE	GPI4_PIN	
0x5D	BUCKA_CONT	Reserved	VBUCKA_GPI		VBUCKA_SEL	BUCKA_PD_DIS	BUCKA_GPI		BUCKA_EN
0x5E	BUCKB_CONT	Reserved	VBUCKB_GPI		VBUCKB_SEL	BUCKB_PD_DIS	BUCKB_GPI		BUCKB_EN
Register Page 1									
0x80	PAGE_CON	REVERT	WRITE_MODE	Reserved	Reserved	Reserved	REG_PAGE		
0xD0	BUCK_ILIM	BUCKB_ILIM				BUCKA_ILIM			
0xD1	BUCKA_CONF	BUCKA_DOWN_CTRL			BUCKA_UP_CTRL			BUCKA_MODE	
0xD2	BUCKB_CONF	BUCKB_DOWN_CTRL			BUCKB_UP_CTRL			BUCKB_MODE	
0xD3	BUCK_CONF	Reserved	Reserved	Reserved	PH_SH_EN_B	PH_SH_EN_A	PHASE_SEL_B	PHASE_SEL_A	
0xD5	VBUCKA_MAX	Reserved	VBUCKA_MAX						
0xD6	VBUCKB_MAX	Reserved	VBUCKB_MAX						
0xD7	VBUCKA_A	BUCKA_SL_A	VBUCKA_A						
0xD8	VBUCKA_B	BUCKA_SL_B	VBUCKA_B						
0xD9	VBUCKB_A	BUCKB_SL_A	VBUCKB_A						
0xDA	VBUCKB_B	BUCKB_SL_B	VBUCKB_B						
Register Page 2									
0x100	PAGE_CON	REVERT	WRITE_MODE	Reserved	Reserved	Reserved	REG_PAGE		
0x105	INTERFACE	IF_BASE_ADDR1				R/W_POL	CPHA	CPOL	nCS_POL
0x106	INTERFACE2	IF_TYPE	PM_IF_HSM	PM_IF_FMP	PM_IF_V	Reserved	Reserved	Reserved	Reserved
0x143	CONFIG_A	Reserved	Reserved	Reserved	2WIRE_TO	GPI_V	Reserved	IRQ_TYPE	IRQ_LEVEL
0x144	CONFIG_B	UVLO_IO_DIS	PGB_DVC_MASK	PGA_DVC_MASK	OCB_MASK		OCA_MASK		RELOAD_FUNC_EN
0x145	CONFIG_C	Reserved	Reserved	Reserved	GPI4_PUPD	GPIO3_PUPD	GPIO2_PUPD	GPI1_PUPD	GPI0_PUPD
0x146	CONFIG_D	BUCKB_PG_SEL		BUCKA_PG_SEL		READYB_CONF		READYA_CONF	
0x147	CONFIG_E	STAND_ALONE	Reserved	Reserved	Reserved	Reserved	OSC_TUNE		
0x148	CONFIG_F	IF_BASE_ADDR2				Reserved	Reserved	ADDR_SEL_CONF	
Register Page 4									
0x200	PAGE_CON	REVERT	WRITE_MODE	Reserved	Reserved	Reserved	REG_PAGE		
0x201	DEVICE_ID	DEV_ID							
0x202	VARIANT_ID	MRC				VRC			
0x203	CUSTOMER_ID	CUST_ID							
0x204	CONFIG_ID	CONFIG_REV							

8.2 Register Definitions

8.2.1 Register Page Control

Register	Bit	Type	Label	Description
0x00 PAGE_CON	7	R/W	REVERT	Resets REG_PAGE to 000 after read/write access has finished
	6	R/W	WRITE_MODE	2-WIRE multiple write mode (Note 1) 0: Page Write Mode 1: Repeated Write Mode
	5:3	R/W	(reserved)	
	2:0	R/W	REG_PAGE	I^2C 00x: Selects Register 0x00 to 0xFF 01x: Selects Register 0x100 to 0x17F 10x: Selects Register 0x200 to 0x27F SPI 000: Selects Register 0x00 to 0x7F 001: Selects Register 0x80 to 0xFF 010: Selects Register 0x100 to 0x17F 100: Selects Register 0x200 to 0x27F

Note 1 Not used for 4-WIRE-IF.

8.2.2 Register Page 0

8.2.2.1 System Control and Event

The STATUS registers report the current value of the various signals at the time that it is read out.

Register	Bit	Type	Label	Description
0x50 STATUS_A	7:5	R	(reserved)	
	4	R	GPI4	GPI4 level
	3	R	GPI3	GPI3 level
	2	R	GPI2	GPI2 level
	1	R	GPI1	GPI1 level
	0	R	GPI0	GPI0 level

Register	Bit	Type	Label	Description
0x51 STATUS_B	7	R	RAMP_READY_B	De-asserted during Buck A DVC, power up and power down
	6	R	RAMP_READY_A	De-asserted during Buck B DVC, power up and power down
	5	R	OV_CURR_B	Asserted as long as the current limit for Buck B is hit
	4	R	OV_CURR_A	Asserted as long as the current limit for Buck A is hit
	3	R	TEMP_CRIT	Asserted as long as the thermal shutdown threshold is reached
	2	R	TEMP_WARN	Asserted as long as the thermal warning threshold is reached

Register	Bit	Type	Label	Description
	1	R	PWRGOOD_B	Asserted as long as the Buck B output voltage is in range
	0	R	PWRGOOD_A	Asserted as long as the Buck A output voltage is in range

The EVENT registers hold information about events that have occurred in DA9223-A and DA9224-A. Events are triggered by a change in the status register which contains the status of monitored signals. When an EVENT bit is set in the event register, the IRQ signal is asserted unless the event is masked by a bit in the mask register. **The IRQ triggering event register will be cleared from the host by writing back its read value.** New events occurring during clearing will be delayed before they are passed to the event register, ensuring that the host controller does not miss them.

Register	Bit	Type	Label	Description
0x52 EVENT_A	7	R	(reserved)	
	6	R	E_UVLO_IO	UVLO_IO caused event
	5	R	(reserved)	
	4	R	E_GPI4	GPI4 event according to active state setting
	3	R	E_GPI3	GPI3 event according to active state setting
	2	R	E_GPI2	GPI2 event according to active state setting
	1	R	E_GPI1	GPI1 event according to active state setting
	0	R	E_GPI0	GPI0 event according to active state setting

Register	Bit	Type	Label	Description
0x53 EVENT_B	7:6	R	(reserved)	
	5	R	E_OV_CURR_B	OV_CURR Buck B caused event
	4	R	E_OV_CURR_A	OV_CURR Buck A caused event
	3	R	E_TEMP_CRIT	TEMP_CRIT caused event
	2	R	E_TEMP_WARN	TEMP_WARN caused event
	1	R	E_PWRGOOD_B	PWRGOOD loss at Buck B caused event
	0	R	E_PWRGOOD_A	PWRGOOD loss at Buck A caused event

Register	Bit	Type	Label	Description
0x54 MASK_A	7	R/W	(reserved)	
	6	R/W	M_UVLO_IO	Mask UVLO_IO caused nIRQ
	5	R/W	(reserved)	
	4	R/W	M_GPI4	Mask nIRQ interrupt at GPI4
	3	R/W	M_GPI3	Mask nIRQ interrupt at GPI3
	2	R/W	M_GPI2	Mask nIRQ interrupt at GPI2
	1	R/W	M_GPI1	Mask nIRQ interrupt at GPI1
	0	R/W	M_GPI0	Mask nIRQ interrupt at GPI0

Register	Bit	Type	Label	Description
0x55 MASK_B	7:6	R/W	(reserved)	
	5	R/W	M_OV_CURR_B	Mask OV_CURR Buck B caused nIRQ and event
	4	R/W	M_OV_CURR_A	Mask OV_CURR Buck A caused nIRQ and event
	3	R/W	M_TEMP_CRIT	Mask TEMP_CRIT caused nIRQ
	2	R/W	M_TEMP_WARN	Mask TEMP_WARN caused nIRQ
	1	R/W	M_PWRGOOD_B	Mask PWRGOOD Buck B caused nIRQ
	0	R/W	M_PWRGOOD_A	Mask PWRGOOD Buck A caused nIRQ

Register	Bit	Type	Label	Description
0x56 CONTROL_A	7	R/W	V_LOCK	0: Allows host writes into registers 0xD0 to 0x14F 1: Disables register 0xD0 to 0x14F re-programming from control interfaces
	6:5	R/W	SLEW_RATE_B	Buck B DVC slewing is executed at 00: 10mV every 4.0 µs 01: 10mV every 2.0 µs 10: 10mV every 1.0 µs 11: 10mV every 0.5 µs
	4:3	R/W	SLEW_RATE_A	Buck A DVC slewing is executed at 00: 10mV every 4.0 µs 01: 10mV every 2.0 µs 10: 10mV every 1.0 µs 11: 10mV every 0.5 µs
	0:2	R/W	DEBOUNCE	Input signals debounce time: 000: no debounce time 001: 0.1 ms 010: 1.0 ms 011: 10 ms 100: 50 ms 101: 250 ms 110: 500 ms 111: 1000 ms

8.2.2.2 GPIO Control

Register	Bit	Type	Label	Description
0x58 GPI0-1	7	R/W	GPI1_MODE	0: GPI: debouncing off 1: GPI: debouncing on
	6	R/W	GPI1_TYPE	0: GPI: active low 1: GPI: active high
	5:4	R/W	GPI1_PIN	PIN assigned to: 00: GPI >00: Reserved
	3	R/W	GPI0_MODE	0: GPI: debouncing off 1: GPI: debouncing on

Register	Bit	Type	Label	Description
	2	R/W	GPI0_TYPE	0: GPI: active low 1: GPI: active high
	1:0	R/W	GPI0_PIN	PIN assigned to: 00: GPI 01: Track enable 1x: Reserved

Register	Bit	Type	Label	Description
0x59 GPIO2-3	7	R/W	GPIO3_MODE	0: GPI: debouncing off **GPO: Sets output to passive level** 1: GPI: debouncing on GPO: Sets output to active level
	6	R/W	GPIO3_TYPE	0: GPI/GPO: active low 1: GPI/GPO: active high
	5:4	R/W	GPIO3_PIN	PIN assigned to: 00: GPI 01: Reserved 10: GPO (Open drain) 11: GPO (Push-pull)
	3	R/W	GPIO2_MODE	0: GPI: debouncing off **GPO: Sets output to passive level** 1: GPI: debouncing on GPO: Sets output to active level
	2	R/W	GPIO2_TYPE	0: GPI/GPO: active low 1: GPI/GPO: active high
	1:0	R/W	GPIO2_PIN	PIN assigned to: 00: GPI 01: Reserved 10: GPO (Open drain) 11: GPO (Push-pull)

Register	Bit	Type	Label	Description
0x5A GPI4	7:4	R/W	(reserved)	
	3	R/W	GPI4_MODE	0: GPI: debouncing off 1: GPI: debouncing on
	2	R/W	GPI4_TYPE	0: GPI: active low 1: GPI: active high
	1:0	R/W	GPI4_PIN	PIN assigned to: 00: GPI 01: Reserved 1x: Reserved

8.2.2.3 Regulators Control

Register	Bit	Type	Label	Description
0x5D BUCKA_CONT	7	R/W	(reserved)	
	6:5	R/W	VBUCKA_GPI	Selects the GPI that specifies the target voltage of VBUCKA. This is VBUCKA_A on active to passive transition, VBUCKA_B on passive to active transition. Active high/low is controlled by GPIx_TYPE. 00: Not controlled by GPIO 01: GPI1 controlled 10: GPIO2 controlled 11: GPI4 controlled
	4	R/W	VBUCKA_SEL	Buck A voltage is selected from (ramping): 0: VBUCKA_A 1: VBUCKA_B
	3	R/W	BUCKA_PD_DIS	0: Enable pull-down resistor of Buck A when the buck is disabled 1: Disable pull-down resistor of Buck A when the buck is disabled
	2:1	R/W	BUCKA_GPI	GPI enables the Buck A on passive to active state transition, disables the Buck A on active to passive state transition 00: Not controlled by GPIO 01: GPI0 controlled 10: GPI1 controlled 11: GPIO3 controlled
	0	R/W	BUCKA_EN	0: Buck A disabled 1: Buck A enabled

Register	Bit	Type	Label	Description
0x5E BUCKB_CONT	7	R/W	(reserved)	
	6:5	R/W	VBUCKB_GPI	Selects the GPI that specifies the target voltage of VBUCKB. This is VBUCKB_A on active to passive transition, VBUCKB_B on passive to active transition. Active high/low is controlled by GPIx_TYPE 00: Not controlled by GPIO 01: GPI1 controlled 10: GPIO2 controlled 11: GPI4 controlled
	4	R/W	VBUCKB_SEL	Buck A voltage is selected from (ramping): 0: VBUCKB_A 1: VBUCKB_B
	3	R/W	BUCKB_PD_DIS	0: Enable pull-down resistor of Buck B when the buck is disabled 1: Disable pull-down resistor of Buck B when the buck is disabled

Register	Bit	Type	Label	Description
	2:1	R/W	BUCKB_GPI	GPI enables the Buck B on passive to active state transition, disables the Buck B on active to passive state transition 00: Not controlled by GPIO 01: GPI0 controlled 10: GPI1 controlled 11: GPIO3 controlled
	0	R/W	BUCKB_EN	0: Buck B disabled 1: Buck B enabled

8.2.3 Register Page 1

Register	Bit	Type	Label	Description
0x80 PAGE_CON	7	R/W	REVERT	Resets REG_PAGE to 000 after read/write access has finished
	6	R/W	WRITE_MODE	2-WIRE multiple write mode 0: Page Write Mode 1: Repeated Write Mode
	5:3	R/W	(reserved)	
	2:0	R/W	REG_PAGE	I^2C 00x: Selects Register 0x00 to 0xFF 01x: Selects Register 0x100 to 0x17F 10x: Selects Register 0x200 to 0x27F SPI 000: Selects Register 0x00 to 0x7F 001: Selects Register 0x80 to 0xFF 010: Selects Register 0x100 to 0x17F 100: Selects Register 0x200 to 0x27F

8.2.3.1 Regulators Settings

Register	Bit	Type	Label	Description
0xD0 BUCK_ILIM	7:4	R/W	BUCKB_ILIM	Current limit per phase: 0000: 4000 mA 0001: 4200 mA 0010: 4400 mA continuing through… 1001: 5800 mA to… 1110: 6800 mA 1111: 7000 mA

Register	Bit	Type	Label	Description
	3:0	R/W	BUCKA_ILIM	Current limit per phase: 0000: 4000 mA 0001: 4200 mA 0010: 4400 mA continuing through… 1001: 5800 mA to… 1110: 6800 mA 1111: 7000 mA

Register	Bit	Type	Label	Description
0xD1 BUCKA_CONF	7:5	R/W	BUCKA_DOWN_CTRL	Buck A voltage ramping during power down 000: 1.25 mV/µs 001: 2.5 mV/µs 010: 5 mV/µs 011: 10 mV/µs 100: 20 mV/µs 101: 30 mV/µs 110: 40 mV/µs 111: Reserved
	4:2	R/W	BUCKA_UP_CTRL	Buck A voltage ramping during start up 000: 1.25 mV/µs 001: 2.5 mV/µs 010: 5 mV/µs 011: 10 mV/µs 100: 20 mV/µs (Note 1) 101: 30 mV/µs 110: 40 mV/µs 111: target voltage applied immediately (no soft start)
	1:0	R/W	BUCKA_MODE	00: PFM/PWM mode controlled via voltage A and B registers 01: Automatic mode (1-phase) 10: Buck A always operates in PWM mode 11: Automatic mode

Note 1 Settings higher than 20 mV/µs may cause significant overshoot.

Register	Bit	Type	Label	Description
0xD2 BUCKB_CONF	7:5	R/W	BUCKB_DOWN_CTRL	Buck B voltage ramping during power down 000: 1.25 mV/µs 001: 2.5 mV/µs 010: 5 mV/µs 011: 10 mV/µs 100: 20 mV/µs 101: 30 mV/µs 110: 40 mV/µs 111: Reserved
	4:2	R/W	BUCKB_UP_CTRL	Buck B voltage ramping during start up 000: 1.25 mV/µs 001: 2.5 mV/µs 010: 5 mV/µs 011: 10 mV/µs 100: 20 mV/µs (Note 1) 101: 30 mV/µs 110: 40 mV/µs 111: target voltage applied immediately (no soft start)
	1:0	R/W	BUCKB_MODE	00: PFM/PWM mode controlled via voltage A and B registers 01: Automatic mode (1-phase) 10: Buck B always operates in PWM mode 11: Automatic mode

Note 1 Settings higher than 20mV/µs may cause significant overshoot.

Register	Bit	Type	Label	Description
0xD3 BUCK_CONF	7:5	R/W	(reserved)	
	4	R/W	PH_SH_EN_B	Enable current dependent phase shedding in PWM for Buck B
	3	R/W	PH_SH_EN_A	Enable current dependent phase shedding in PWM for Buck A
	2	R/W	PHASE_SEL_B	Phase selection for Buck B in PWM 0: 1 phase is selected 1: 2 phases are selected
	1:0	R/W	PHASE_SEL_A	Phase selection for Buck A in PWM mode. Settings >01 apply only for DA9223-A otherwise the number of phases is limited to max 2 00: 1 phase is selected 01: 2 phases are selected 10: 3 phases are selected (uneven 0/90/180 phase shift) 11: 4 phases are selected

Register	Bit	Type	Label	Description
0xD5 VBUCKA_MAX	7	R/W	(reserved)	
	6:0	R	VBUCKA_MAX	Sets the maximum voltage allowed for Buck A (OTP programmed, access only in test mode) 0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V Continuing through… 1000110: 1.0 V to… 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

Register	Bit	Type	Label	Description
0xD6 VBUCKB_MAX	7	R/W	(reserved)	
	6:0	R	VBUCKB_MAX	Sets the maximum voltage allowed for Buck B (OTP programmed, access only in test mode) 0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V Continuing through… 1000110: 1.0 V to… 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

Register	Bit	Type	Label	Description
0xD7 VBUCKA_A	7	R/W	BUCKA_SL_A	0: Configures Buck A to PWM mode whenever selecting A voltage setting 1: Configures Buck A to automatic mode whenever selecting A voltage setting
	6:0	R/W	VBUCKA_A	0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V Continuing through… **1000110: 1.0 V** to… 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

Register	Bit	Type	Label	Description
0xD8 VBUCKA_B	7	R/W	BUCKA_SL_B	0: Configures Buck A to PWM mode, whenever selecting B voltage setting 1: Configures Buck A to automatic mode, whenever selecting B voltage setting
	6:0	R/W	VBUCKA_B	0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V Continuing through… **1000110: 1.0 V** to… 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V
Register	**Bit**	**Type**	**Label**	**Description**
0xD9 VBUCKB_A	7	R/W	BUCKB_SL_A	0: Configures Buck B to PWM mode, whenever selecting A voltage setting 1: Configures Buck B to automatic mode, whenever selecting A voltage setting
	6:0	R/W	VBUCKB_A	0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V Continuing through… **1000110: 1.0 V** to… 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

Register	Bit	Type	Label	Description
0xDA VBUCKB_B	7	R/W	BUCKB_SL_B	0: Configures Buck B to PWM mode, whenever selecting B voltage setting 1: Configures Buck B to automatic mode, whenever selecting B voltage setting
	6:0	R/W	VBUCKB_B	0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V Continuing through… **1000110: 1.0 V** to… 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

8.2.4 Register Page 2

Register	Bit	Type	Label	Description
0x100 PAGE_CON	7	R/W	REVERT	Resets REG_PAGE to 000 after read/write access has finished
	6	R/W	WRITE_MODE	2-WIRE multiple write mode 0: Page Write Mode 1: Repeated Write Mode
	5:3	R/W	(reserved)	
	2:0	R/W	REG_PAGE	I^2C 00x: Selects Register 0x00 to 0xFF 01x: Selects Register 0x100 to 0x17F 10x: Selects Register 0x200 to 0x27F SPI 000: Selects Register 0x00 to 0x7F 001: Selects Register 0x80 to 0xFF 010: Selects Register 0x100 to 0x17F 100: Selects Register 0x200 to 0x27F

8.2.4.1 Interface and OTP Settings (Shared with DA9063)

Register	Bit	Type	Label	Description
0x105 INTERFACE	7:4	R/W	IF_BASE_ADDR 1	4 MSB of 2-WIRE control interfaces base address XXXX0000 11010000 = 0xD0 write address of PM 2-WIRE interface (page 0 and 1) 11010001 = 0xD1 read address of PM 2-WIRE interface (page 0 and 1) 11010010 = 0xD2 write address of PM-2-WIRE interface (page 2 and 3) 11010011 = 0xD3 read address of PM-2-WIRE interface (page 2 and 3) 11010101 = 0xD5 read address of PM-2-WIRE interface (page 4 and 5) Code '0000' is reserved for unprogrammed OTP (triggers start-up with hardware default interface address)
	3	R/W	R/W_POL	4-WIRE: Read/Write bit polarity 0: Host indicates reading access via R/W bit = '0' 1: Host indicates reading access via R/W bit = '1'
	2	R/W	CPHA	4-WIRE interface clock phase (see Table 10)
	1	R/W	CPOL	4-WIRE interface clock polarity 0: SK is low during idle 1: SK is high during idle
	0	R/W	nCS_POL	4-WIRE chip select polarity 0: nCS is low active 1: nCS is high active

Register	Bit	Type	Label	Description
0x106 INTERFACE2	7	R/W	IF_TYPE	0: Power manager interface is 4-WIRE. Automatically configures GPIO3 and GPI4 as interface signals. The GPIO configuration is overruled. 1: Power manager interface is 2-WIRE
	6	R/W	PM_IF_HSM	Enables continuous high speed mode on 2-WIRE interface if asserted (no master code required)
	5	R/W	PM_IF_FMP	Enables 2-WIRE interface operating with fast mode+ timings if asserted
	4	R/W	PM_IF_V	0: Power manager interface in 2-WIRE mode is supplied from VDDCORE (4-WIRE always from VDDIO) 1: Power manager interface in 2-WIRE mode is supplied from VDDIO (4-WIRE always from VDDIO)
	0:3	R/W	(reserved)	

8.2.4.2 Application Configuration Settings

Register	Bit	Type	Label	Description
0x143 CONFIG_A	7:5	R/W	(reserved)	
	4	R/W	2WIRE_TO	Enables automatic reset of 2-WIRE interface if the clock stays low for >35 ms 0: Disabled 1: Enabled
	3	R/W	GPI_V	GPIs are supplied from: 0: VDDCORE 1: VDDIO
	2	R/W	(reserved)	
	1	R/W	IRQ_TYPE	nIRQ output port is: 0: Push-pull 1: Open drain (requires external pull-up resistor)
	0	R/W	IRQ_LEVEL	nIRQ output port is: 0: Active low 1: Active high

Register	Bit	Type	Label	Description
0x144 CONFIG_B	7	R/W	UVLO_IO_DIS	Disable the UVLO for the VDDIO rail and its comparator (suggested for rail voltages different to 1.8 V and to save quiescent current)
	6	R/W	PGB_DVC_MASK	Power-good configuration for Buck B 0: Power-good signal not masked during DVC transitions 1: Power-good signal masked during DVC transitions (keep previous status)
	5	R/W	PGA_DVC_MASK	Power-good configuration for Buck A 0: Power-good signal not masked during DVC transitions 1: Power-good signal masked during DVC transitions (keep previous status)

Register	Bit	Type	Label	Description
	4:3	R/W	OCB_MASK	Over Current configuration for Buck B 00: Event generation due to over current hit is always active during DVC transitions of the Buck converter 01: Event generation due to over current hit is masked during DVC transitions of the buck converter + 2 µs extra masking at the end 10: Event generation due to over current hit is masked during DVC transitions of the buck converter + 10 µs extra masking at the end 11: Event generation due to over current hit is masked during DVC transitions of the buck converter + 50 µs extra masking at the end
	2:1	R/W	OCA_MASK	Over Current configuration for Buck A 00: Event generation due to over current hit is always active during DVC transitions of the buck converter 01: Event generation due to over current hit is masked during DVC transitions of the buck converter + 2 µs extra masking at the end 10: Event generation due to over current hit is masked during DVC transitions of the buck converter + 10 µs extra masking at the end 11: Event generation due to over current hit is masked during DVC transitions of the buck converter + 50 µs extra masking at the end
	0	R/W	RELOAD_FUNC_EN	Enable the OTP re-load function for GPI0 when configured as input port

Register	Bit	Type	Label	Description
0x145 CONFIG_C	7:5	R/W	(reserved)	
	4	R/W	GPI4_PUPD	0: GPI: pull-down resistor disabled 1: GPI: pull-down resistor enabled
	3	R/W	GPIO3_PUPD	0: GPI: pull-down resistor disabled GPO (open drain): pull up resistor disabled (external pull-up resistor) 1: GPI: pull-down resistor enabled GPO (open drain): pull up resistor
	2	R/W	GPIO2_PUPD	0: GPI: pull-down resistor disabled GPO (open drain): pull up resistor disabled (external pull-up resistor) 1: GPI: pull-down resistor enabled GPO (open drain): pull up resistor enabled
	1	R/W	GPI1_PUPD	0: GPI: pull-down resistor disabled 1: GPI: pull-down resistor enabled
	0	R/W	GPI0_PUPD	0: GPI: pull-down resistor disabled 1: GPI: pull-down resistor enabled

Register	Bit	Type	Label	Description
0x146 CONFIG_D	7:6	R/W	BUCKB_PG_SEL	Selection of the PG signal for Buck B 00: none 01: GPO2 10: GPO3 11: reserved
	5:4	R/W	BUCKA_PG_SEL	Selection of the PG signal for Buck A 00: none 01: GPO2 10: GPO3 11: reserved
	3:2	R/W	READYB_CONF	Selection of the READY signal for Buck B 00: none 01: GPO2 10: GPO3 11: reserved
	1:0	R/W	READYA_CONF	Selection of the READY signal for Buck A 00: none 01: GPO2 10: GPO3 11: reserved

Register	Bit	Type	Label	Description
0x147 CONFIG_E	7	R/W	STAND_ALONE	0: DA9223-A and DA9224-A **is** used as companion IC to DA9063 or DA9063-compliant 1: DA9223-A and DA9224-A is stand alone or as companion IC with another PMU not DA9063-compliant
	6:5	R/W	(reserved)	
	4:3	R/W	(reserved)	
	2:0	R/W	OSC_TUNE	Tune the main 6 MHz oscillator frequency: 000: no tune 001: +180 kHz 010: +360 kHz 011: +540 kHz 100: +720 kHz 101: +900 kHz 110: +1080 kHz 111: +1260 kHz

Register	Bit	Type	Label	Description
0x148 CONFIG_F	7:4	R/W	IF_BASE_ADDR 2	If a second I²C address is to be selected on ADR_SEL_CONF, this field configures the second address. 4 MSB of 2-WIRE control interfaces base address XXXX0000 11010000 = 0xD0 write address of PM 2-WIRE interface (page 0 and 1) 11010001 = 0xD1 read address of PM 2-WIRE interface (page 0 and 1) 11010010 = 0xD2 write address of PM-2-WIRE interface (page 2 and 3) 11010011 = 0xD3 read address of PM-2-WIRE interface (page 2 and 3) 11010101 = 0xD5 read address of PM-2-WIRE interface (page 4 and 5) Code ‘0000’ is reserved for unprogrammed OTP (triggers start-up with hardware default interface address)
	3:2	R	(reserved)	
	1	R/W	ADDR_SEL_CONF	Selects the GPI for the alternative I²C address selection: 00: none 01: GPI0 10: GPI1 11: GPI4

8.2.5 Register Page 4

Register	Bit	Type	Label	Description
0x200 PAGE_CON	7	R/W	REVERT	Resets REG_PAGE to 000 after read/write access has finished
	6	R/W	WRITE_MODE	2-WIRE multiple write mode 0: Page Write Mode 1: Repeated Write Mode
	5:3	R/W	(reserved)	
	2:0	R/W	REG_PAGE	I^2C 00x: Selects Register 0x00 to 0xFF 01x: Selects Register 0x100 to 0x17F 10x: Selects Register 0x200 to 0x27F SPI 000: Selects Register 0x00 to 0x7F 001: Selects Register 0x80 to 0xFF 010: Selects Register 0x100 to 0x17F 100: Selects Register 0x200 to 0x27F

8.2.5.1 Chip and OTP IDs

Register	Bit	Type	Label	Description
0x201 DEVICE_ID	7:0	R	DEV_ID	Device ID

Register	Bit	Type	Label	Description
0x202 VARIANT_ID	7:4	R	MRC	Mask Revision Code
	3:0	R	VRC	Chip Variant Code

Register	Bit	Type	Label	Description
0x203 CUSTOMER_ID	7:0	R	CUST_ID	Customer ID

Register	Bit	Type	Label	Description
0x204 CONFIG_ID	7:0	R	CONFIG_REV	OTP Variant

9 Application Information

The following recommended components are examples selected from requirements of a typical application.

9.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

Table 14: Recommended Capacitor Types

Application	Value	Size	Temp Char	Tol	V-Rate	Type
VOUT output bypass	47 uF	1210	X7R ±15 %	±10 %	6.3 V	Murata GCM32ER70J476KE19
	22 uF	1206	X7R ±15 %	±10 %	6.3 V	Murata GCM31CR70J226KE23
	10 uF	0805	X7R ±15 %	±10 %	6.3 V	Murata GCM21BR70J106KE22
VDDx bypass	10 uF	0805	X7R ±15 %	±10 %	10 V	Murata GCM21BR71A106KE22
VSYS bypass	1 uF	0603	X7R ±15 %	±10 %	16 V	Murata GCM188R71C105KA64
VDDIO bypass	100 nF	0402	X7R ±15 %	±10 %	50 V	Murata GCM155R71H104KE02

9.2 Inductor Selection

Inductors should be selected based upon the following parameters:

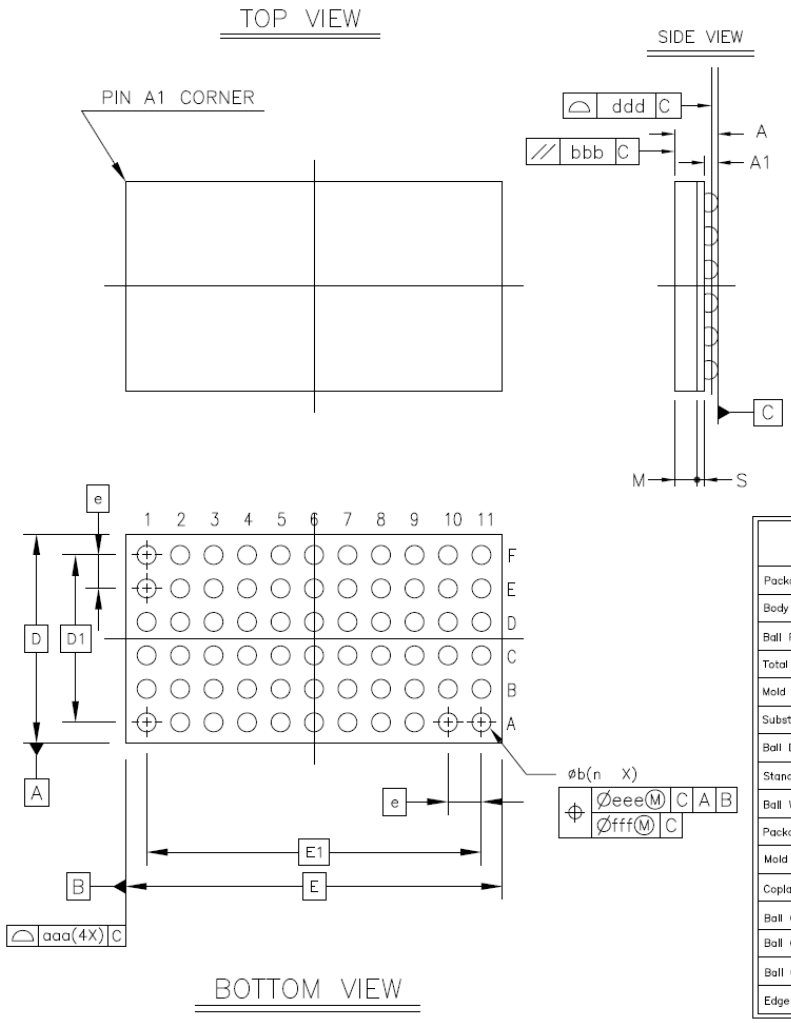
- Rated max. current: usually a coil provides two current limits: The Isat specifies the maximum current at which the inductance drops by 30 % of the nominal value. The Imax is defined by the maximum power dissipation and is applied to the effective current.
- DC resistance: critical for the converter efficiency and should therefore be minimized.
- The typical recommended output inductance is 0.22 µH per phase. Use of larger output inductance degrades the load transient performance of the buck converter.

Table 15: Recommended Inductor Types

Application	Value	Size	Imax(dc)	Isat	Tol	DC res	Type
BUCK	0.22 uH	2.5 mm x 2.0 mm x 1.0 mm	7.1 A	8.0 A	±20%	12 mΩ	TDK TFM252010ALMAR22M TAA
	0.22 uH	2.5 mm x 2.0 mm x 1.2 mm	8.5 A	10 A	±20%	8 mΩ	TDK TFM252012ALMAR22M TAA
	0.24 uH	2.0 mm x 1.6 mm x 1.0 mm	7.0 A	7.5 A	±20%	15 mΩ	TDK TFM201610ALMAR24M TAA
	0.24 uH	2.0 mm x 1.6 mm x 1.2 mm	4.8 A	5.9 A	±20%	16 mΩ	TOKO DFE201612PD-R24M
	0.47 uH	2.5 mm x 2.0 mm x 1.0 mm	5.4 A	6.5 A	±20%	20 mΩ	TDK TFM252010ALMAR47M TAA
	0.47 uH	2.5 mm x 2.0 mm x 1.2 mm	5.6 A	6.5 A	±20%	19 mΩ	TDK TFM252012ALMAR47M TAA
	0.47 uH	2.5 mm x 2.0 mm x 1.2 mm	4.7 A	6.1 A	±20%	21 mΩ	TOKO DFE252012PD-R47M
	0.47 uH	2.0 mm x 1.6 mm x 1.0 mm	5.0 A	5.8 A	±20%	28 mΩ	TDK TFM201610ALMAR47M TAA
	0.47 uH	2.0 mm x 1.6 mm x 1.2 mm	3.8 A	4.5 A	±20%	26 mΩ	TOKO DFE201612PD-R47M
	0.24 uH	2.0 mm x 1.6 mm x 1.2 mm	5.0 A	7.7 A	±20%	16 mΩ	Taiyo Yuden MEMK2016TR24MV
	0.47 uH	2.0 mm x 1.6 mm x 1.2 mm	3.8 A	5.5 A	±20%	28 mΩ	Taiyo Yuden MEMK2016TR47MV
	0.24 uH	2.5 mm x 2.0 mm x 1.2 mm	5.9 A	8.5 A	±20%	13 mΩ	Taiyo Yuden MEMK2520TR24MV
	0.47 uH	2.5 mm x 2.0 mm x 1.2 mm	4.7 A	6.2 A	±20%	21 mΩ	Taiyo Yuden MEMK2520TR47MV

10 Package Information

10.1 Package Outlines



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			MFC TFBGA		
Body Size:	X	E	9.000		
	Y	D	5.000		
Ball Pitch :		e	0.800		
Total Thickness :		A	0.949	1.049	1.163
Mold Thickness :		M	0.540 Ref.		
Substrate Thickness :		S	0.184 Ref.		
Ball Diameter :			0.450		
Stand Off :		A1	0.250	–	0.400
Ball Width :		b	0.400	–	0.500
Package Edge Tolerance :		aaa	0.070		
Mold Parallelism :		bbb	0.100		
Coplanarity:		ddd	0.080		
Ball Offset (Package) :		eee	0.120		
Ball Offset (Ball) :		fff	0.050		
Ball Count :		n	66		
Edge Ball Center to Center :	X	E1	8.000		
	Y	D1	4.000		

Figure 28: DA9223-A/24-A 66 TFBGA 0.8 mm Pitch Package Outline Drawing

10.2 Package Marking

Table 16: Package Marking

Package Marking		
A1 Corner >	Marking Content	Format
1st		Orientation
2nd		Logo
3rd		Part No.
4th		OTP/Silicon Version/Option
5th		Date Code
Date Code Format: yy = Year, ww = Week, zzzz = Traceability		
xx identifies the OTP Variant, vv may be used to show the silicon version.		
-A and -AT optionally indicate the Automotive and Automotive high temp test options.		

11 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's website or your local sales representative.

Table 17: Ordering Information

Part Number	Package	Package Description	Comment	Package Outline
DA9223-xxFT1BB-A	66 TFBGA	Tray	Auto Grade 2	Figure 28
DA9223-xxFT2BB-A, Note 1	66 TFBGA	T&R, 3000pcs	Auto Grade 2	
DA9223-xxFTDBB-A	66 TFBGA	T&R, 2200pcs	Auto Grade 2	
DA9224-xxFT1BB-A	66 TFBGA	Tray	Auto Grade 2	
DA9224-xxFT2BB-A, Note 1	66 TFBGA	T&R, 3000pcs	Auto Grade 2	
DA9224-xxFTDBB-A	66 TFBGA	T&R, 2200pcs	Auto Grade 2	
DA9223-xxFT1BB-AT	66 TFBGA	Tray	Auto Grade 2 with High Temp screening	
DA9223-xxFT2BB-AT, Note 1	66 TFBGA	T&R, 3000pcs	Auto Grade 2 with High Temp screening	
DA9223-xxFTDBB-AT	66 TFBGA	T&R, 2200pcs	Auto Grade 2 with High Temp screening	
DA9224-xxFT1BB-AT	66 TFBGA	Tray	Auto Grade 2 with High Temp screening	
DA9224-xxFT2BB-AT, Note 1	66 TFBGA	T&R, 3000pcs	Auto Grade 2 with High Temp screening	
DA9224-xxFTDBB-AT	66 TFBGA	T&R, 2200pcs	Auto Grade 2 with High Temp screening	

Note 1 Large reel sizes are no longer supported, contact sales for further information

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

Disclaimer

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email:
enquiry@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5769 5100

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 2607 4271

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058