Errata

SLG47105

CE-GP-003

Abstract

This document contains the known errata for SLG47105 and the recommended workarounds.

1 Information

Package(s)	20-pin STQFN: 2 mm x 3 mm x 0.55 mm, 0.4 mm pitch

2 Errata Summary

Table 1: Errata Summary

Issue #	Issue Title
1	Dependence of Current Consumption on I2C Read/Write Operation
2	Shifted Rising Edge of the Cycle when the Fast Decay is Applied
3	Incorrect 32 mV and 64 mV Hysteresis Operation with ACMPxH
4	ACMPxH erroneous behavior when used with Wake-Sleep controller for certain Vref selection

3 Errata Details

3.1 Dependence of Current Consumption on I²C Read/Write Operation

3.1.1 Effect

Chip Current Consumption

3.1.2 Conditions

When I²C Read/Write operation stops at certain addresses.

3.1.3 Technical Description

Read/Write operation at certain addresses via I²C can cause significant current consumption increase. The amount of current drawn by the chip is highly dependent on V_{DD} voltage that is applied to the IC, please see Table 2.

Table 2: Chip Current Consumption

V_{DD}	Current Consumption After I²C Interaction with Problematic Addresses	Normal Current Consumption After I²C Interaction
2.3 V	39-150 µA	0.033 µA
2.5 V	45-93 µA	0.033 µA
3.3 V	84-339 µA	0.035 µA
4.0 V	121-488 µA	0.035 µA
5.0 V	177-710 µA	0.040 µA
5.5 V	206-822 µA	0.040 µA

I²C Address pointer increases after the stop of I²C operation. So, in case when Read/Write command stops right before the problematic address, the current consumption increase will appear.

Value of an excess current changes relative to the value of a register being read/written. Most likely, current consumption will increase in the case of reading «1» from the problematic register or writing «0» to it.

3.1.4 Workaround

The best workaround is not to stop the I²C Read/Write operation on the problematic addresses (for example, instead of reading just 0x4E and 0x4F addresses, the Sequential Read Command should include addresses 0x4E, 0x4F, 0x50). This helps to keep an increase time as short as possible.

Also, the problem could be solved by initiating another Read/Write operation with an unaffected address. For the known problematic addresses refer to Table 3.

Table 3: Known Problematic Addresses

Address	0x48	0x49	0x4A	0x4B	0x4D	0x4E	0x4F	0x89
Operation	R/W	R/W	R/W	R/W	R/W	R/W	W	W

Address	0x8A	0x8B	0xA4	0xA5	0xF9	0xFB	0xFC	
Operation	R	W	R/W	R/W	W	R/W	W	

3.2 Shifted Rising Edge of the Cycle when the Fast Decay is Applied

3.2.1 Effect

High Side Pin

3.2.2 Conditions

When Fast Decay mode is applied.

3.2.3 Technical Description:

In the Fast Decay mode, the negative voltage, created by the inductive load on the HV_GPO_HD pin, discharges the internal Charge Pump due to the parasitic p-n junction. Because of this, the Rising Edge on the High Side pin shifts. The duration of the shift depends on the Duty Cycle, the High Side input voltage (V_{DD2}), and the PWM frequency.

For example, the PWM Duty Cycle values higher than 75 % in a combination with V_{DD2} voltage lower than 3.75 V, and the Fast Decay settings applied can cause this problem, please see Figure 1 and Figure 2.

Note: HV GPO_0/1 are set to H-Bridge, Slow Slew Rate, Mode Control: PH-EN. In this case, EN is «HIGH», DECAY MODE Input is «LOW» (Fast Decay).

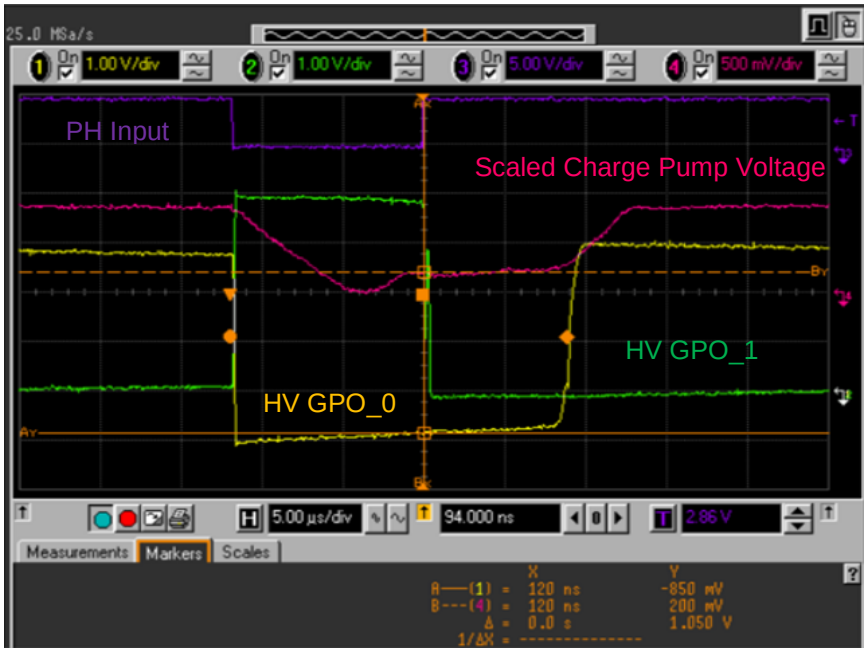

Figure 1: Shifted Rising Edge (V_{DD2} = 3.0 V, Fast Decay, PWM = 75+ %)

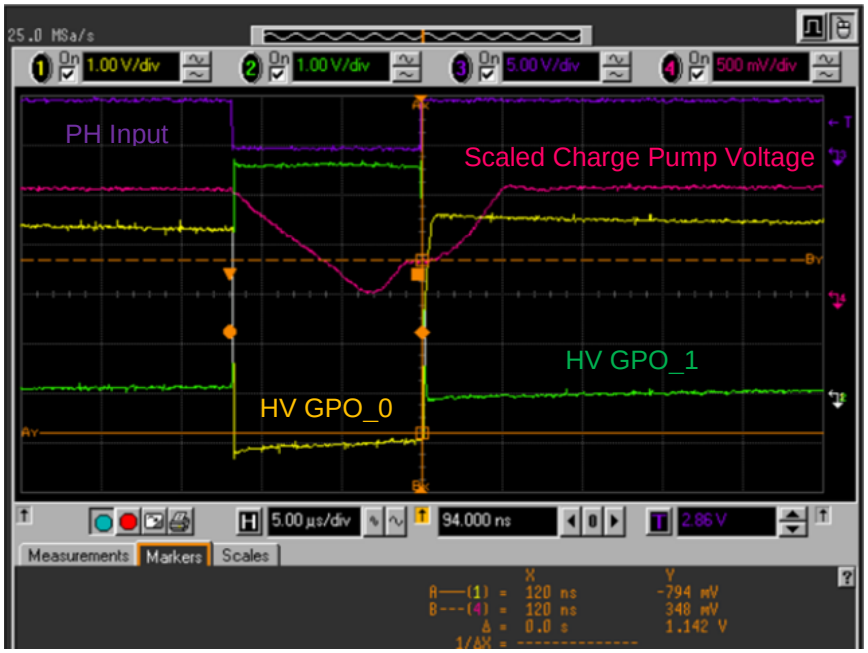

Figure 2: Discharge of the Internal Charge Pump (V_{DD2} = 3.75 V, Fast Decay, PWM = 75+ %)

3.2.4 Workaround:

The best way to exclude a possibility of such a malfunction is to use the Slow Decay option for the H-Bridge instead of the Fast Decay. No evidence of improper behavior has been discovered when V_{DD2} is higher than 3.75 V and the Fast Decay settings are applied. The chip is not affected by this problem when the load is resistive, because the negative voltage will appear on a pin only when the inductive load discharges.

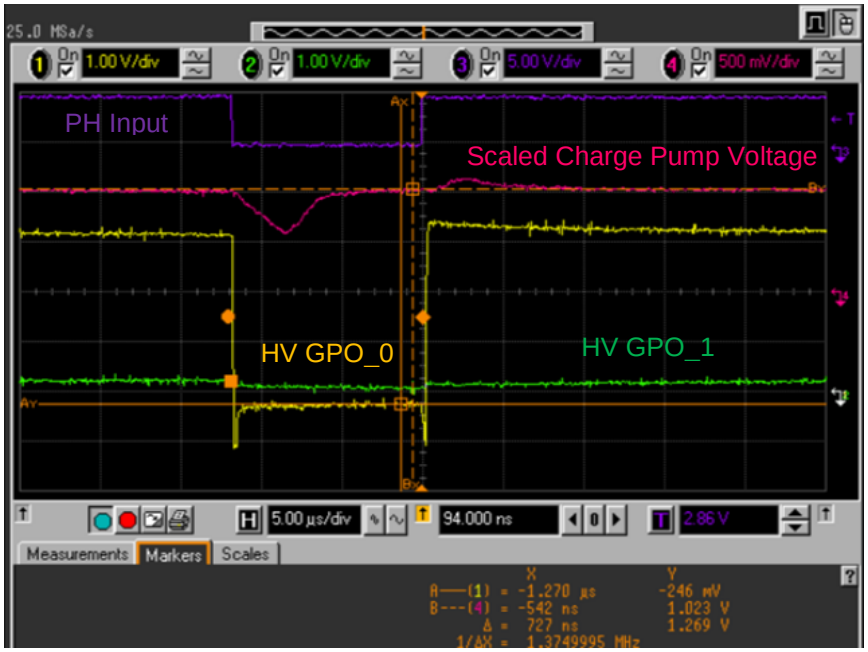

Figure 3: Rising Edge is Not Shifted (V_{DD2} = 3.75 V, Slow Decay, PWM = 75+ %)

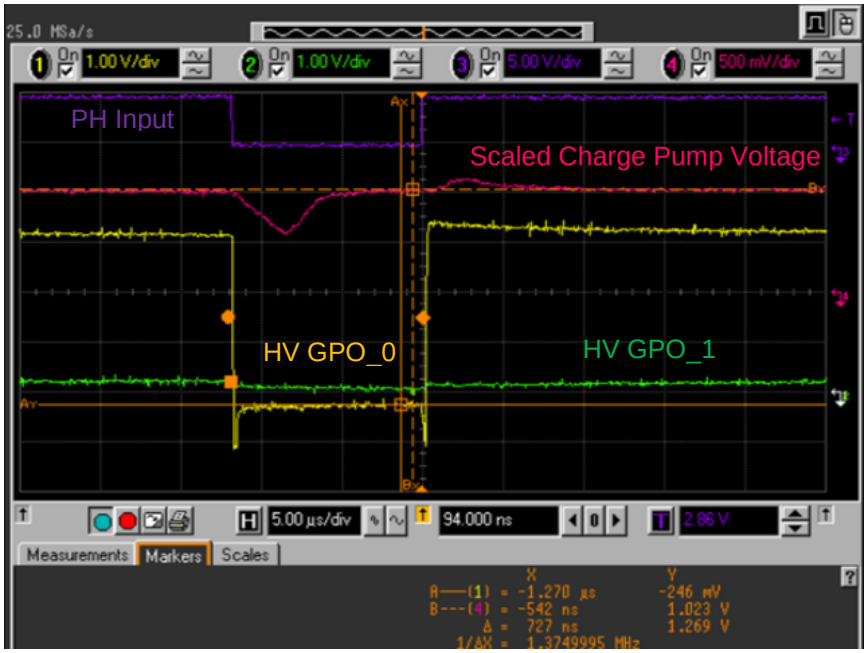

Figure 4: Low V_{DD2} Voltage Operation (V_{DD2} = 2.75 V, Slow Decay, PWM = 75+ %)

3.3 Incorrect 32 mV and 64 mV Hysteresis Operation with ACMPxH

3.3.1 Effect

ACMP0H and ACMP1H

3.3.2 Conditions

V_{DD} > 4.6 V, with hysteresis 32 mV at Vref range 1.344 V to 2.016 V.

V_{DD} > 3.6 V, with hysteresis 32 mV at Vref range 1.344 V to 1.504 V.

V_{DD} > 4.6 V, with hysteresis 64 mV at Vref range 1.376 V to 1.664 V.

3.6 V < V_{DD} < 4.6 V, with hysteresis 64 mV only when Vref is set to 1.376 V.

3.3.3 Technical Description

If using ACMPxH in with 32 mV or 64 mV hysteresis, ACMPxH output could be glitching when ACMPxH positive input (IN+) is close to the negative input (IN-). It can happen when V_{DD} higher 4.6 V and Vref is in a range from 1.344 V to 2.016 V for 32 mV hysteresis, and Vref is in a range from 1.376 V to 1.664 V for 64 mV hysteresis.

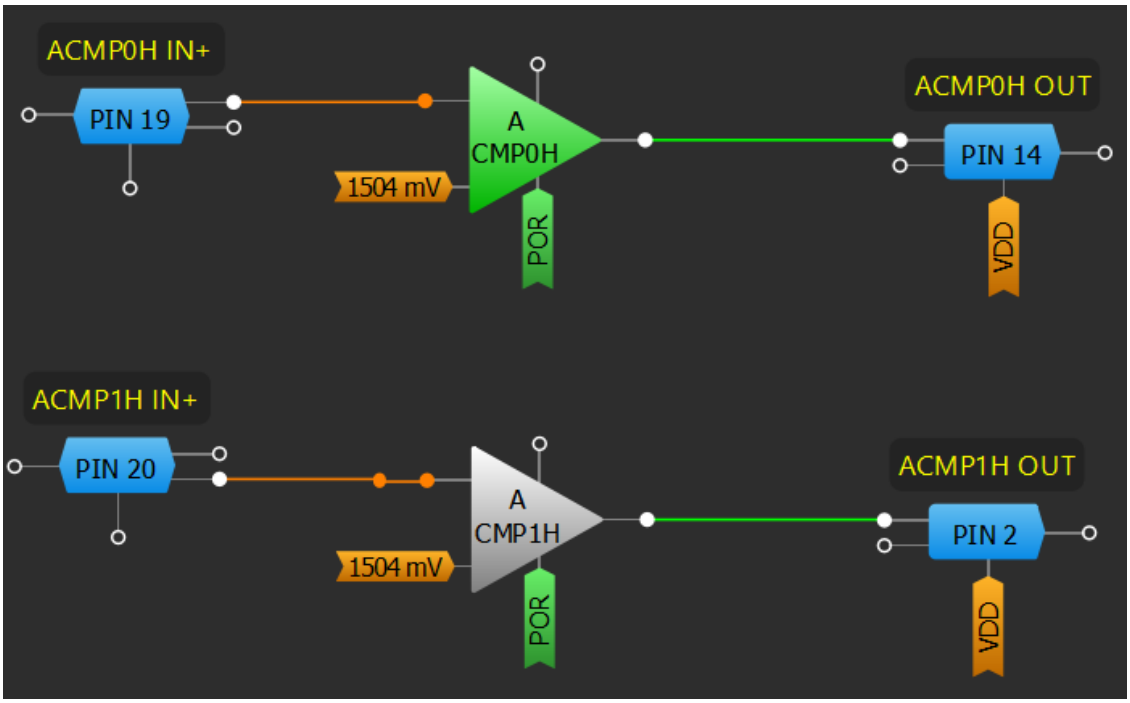

Figure 5: Testing Design

Channel 1 (yellow/top line) - PIN#19 (ACMP0H IN+)

Channel 2 (light blue/2nd line) - PIN#14 (ACMP0H OUT)

1. Waveform at Vref = 1504 mV, hysteresis is equal to 32 mV.

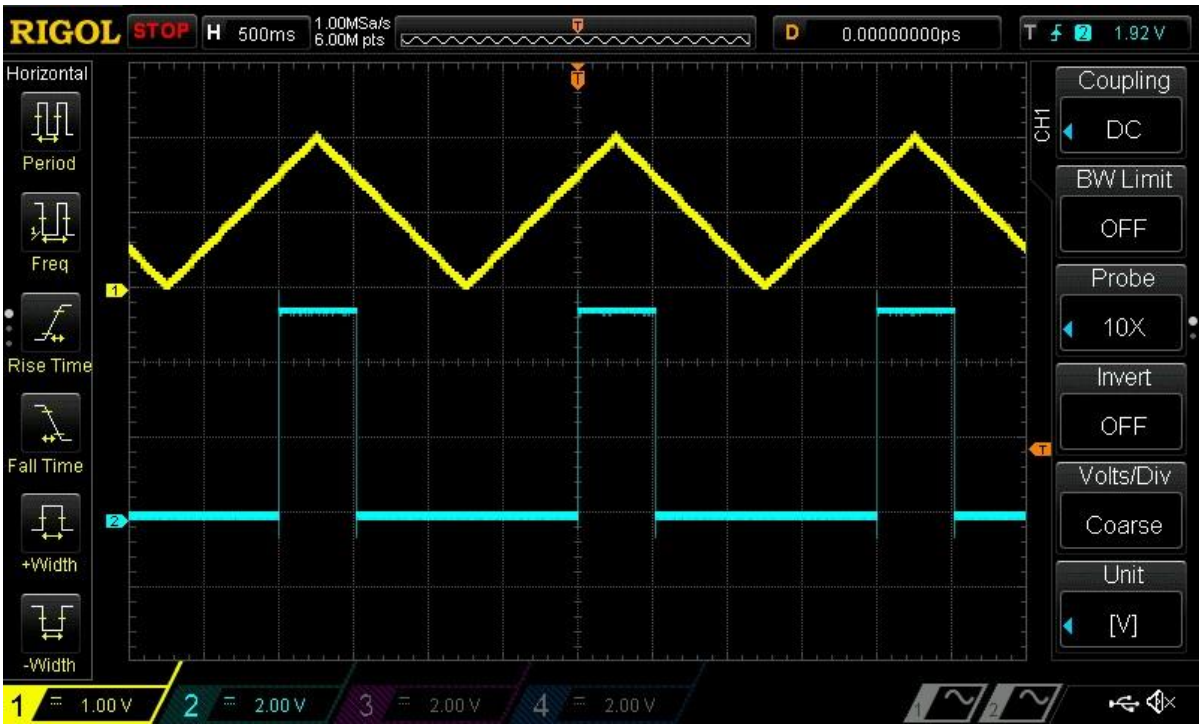

Figure 6: ACMP Output during Glitching

2. Waveform at Vref = 1504 mV, hysteresis is equal to 32 mV (zoomed rising edge).

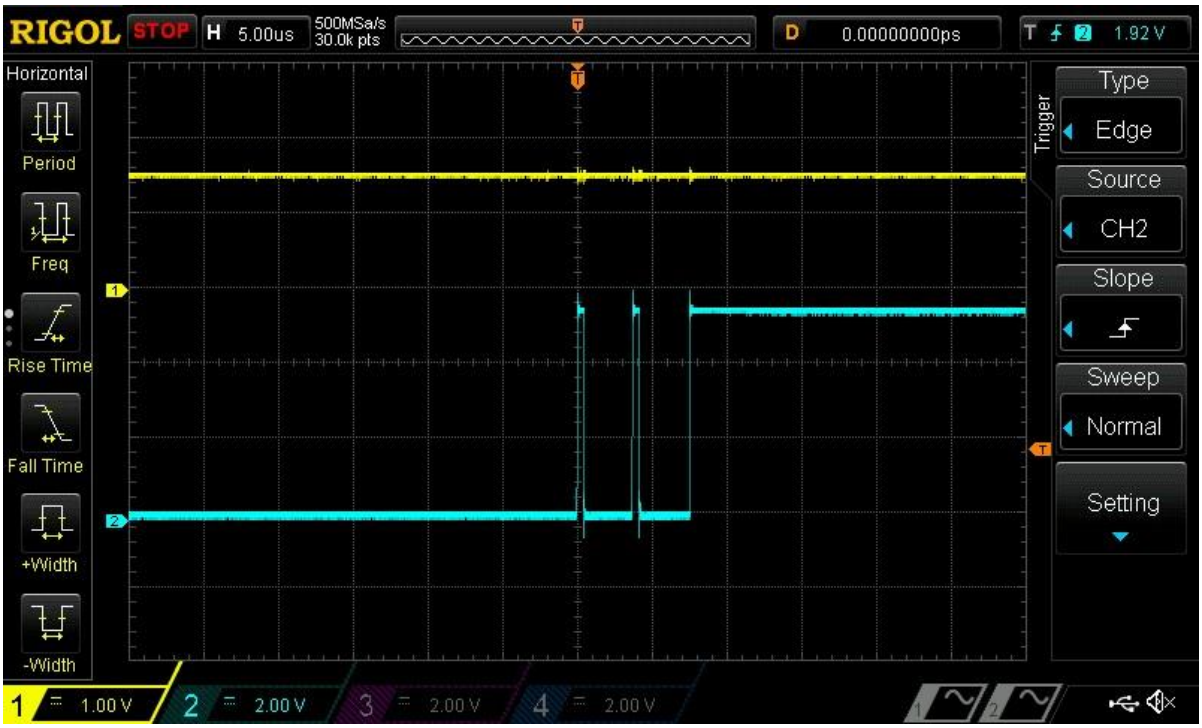

Figure 7: Zoomed ACMP Output during Glitching

3.3.4 Workaround

Use the deglitch filter connected to the ACMPxH output.

Avoid conditions described in paragraph 3.3.2.

Decrease the reference to avoid conditions described in paragraph 3.3.2 at IN- and add the IN+ gain to keep the needed threshold.

3.4 ACMPxH erroneous behavior when used with Wake-Sleep controller for certain Vref selection

3.4.1 Effect

ACMP0H and ACMP1H

3.4.2 Conditions

ACMPxH is used with the macrocell CNT0 configured as a wake-sleep controller (WS Ctrl).

WS Ctrl Short wake time mode is selected, for Vref range 1.312 V to 1.440 V.

WS Ctrl Normal wake time is selected, for two Vref ranges 0.832 V to 0.896 V and 1.312 V to 1.440 V.

3.4.3 Technical Description

When WS Ctrl is used for controlling the power on/off of analog macrocells ACMPs for power saving, ACMPxH shows erroneous behavior for certain Vref selection. Vref transient settling error is observed for both WS Ctrl Wake time modes, Short wake time and Normal wake time (selections under CNT0 settings).

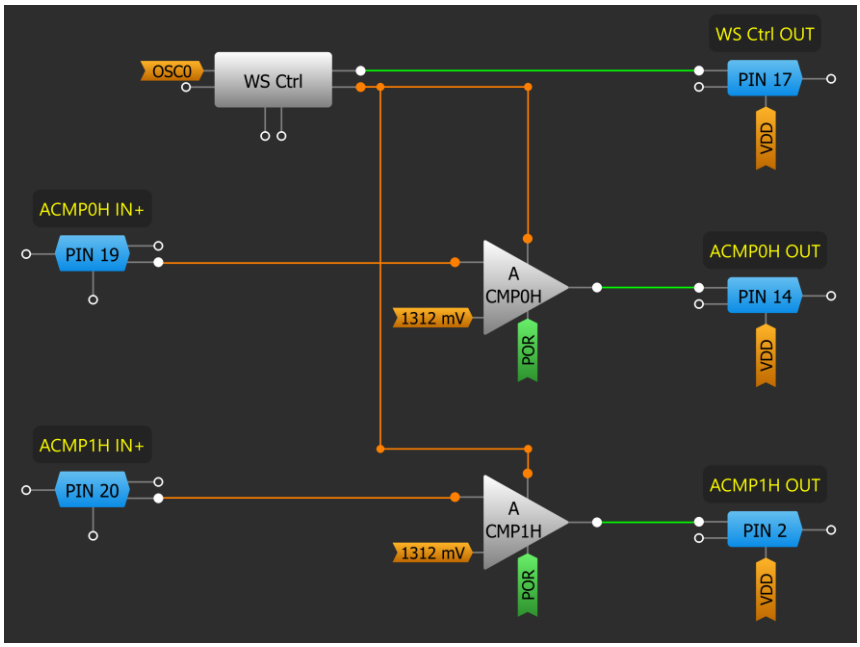

Figure 8: Testing Design

Channel 1 (yellow/top line) - PIN#19 (ACMP0H IN+)

Channel 2 (light blue/2nd line) - PIN#17 (WS Ctrl OUT)

Channel 3 (magenta /3rd line) - PIN#14 (ACMP0H OUT)

1. Waveform at Vref = 1312 mV, hysteresis is equal to 32 mV

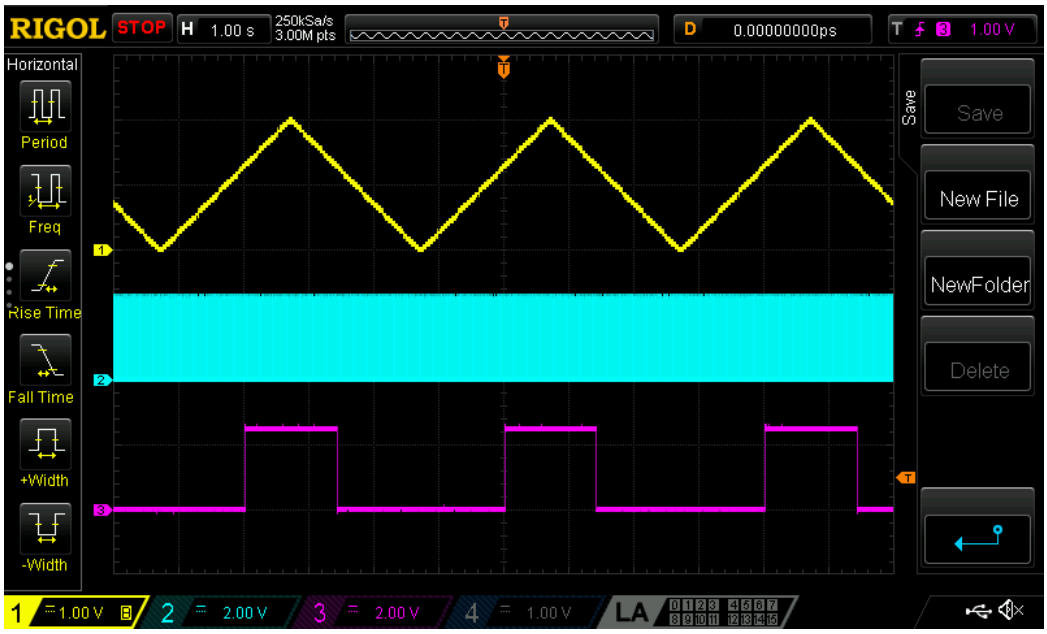

Figure 9: ACMP0H Output during Glitching

2. Waveform at Short wake time mode, Vref = 1312 mV, hysteresis is equal to 32 mV (zoomed rising edge).

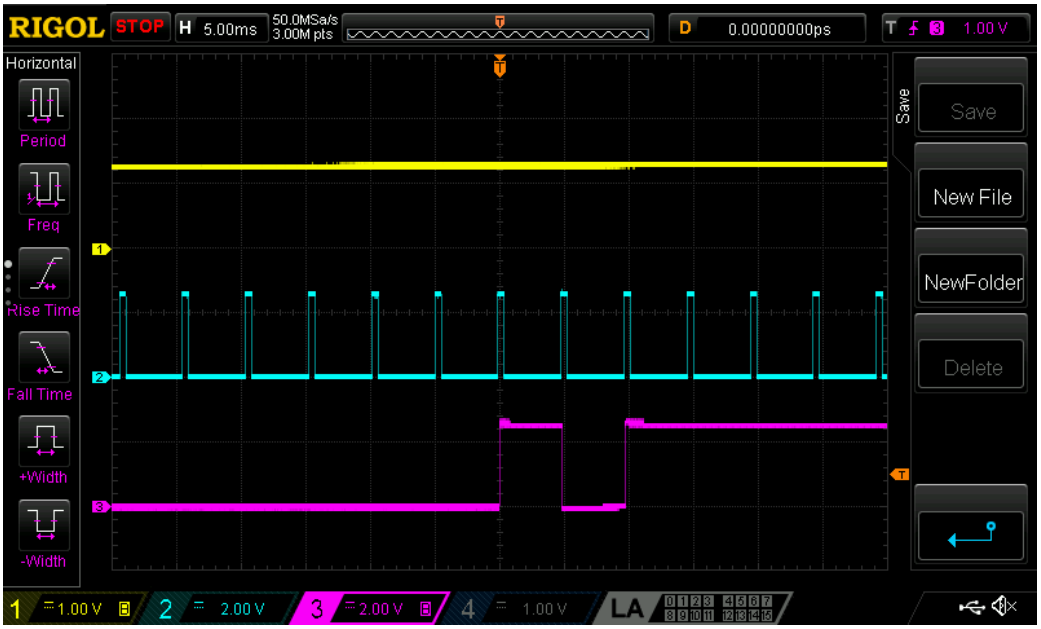

Figure 10: Zoomed ACMP Output during Glitching at Short wake time mode

3. Waveform at Normal wake time mode, Vref = 1312 mV, hysteresis is equal to 32 mV (zoomed rising edge).

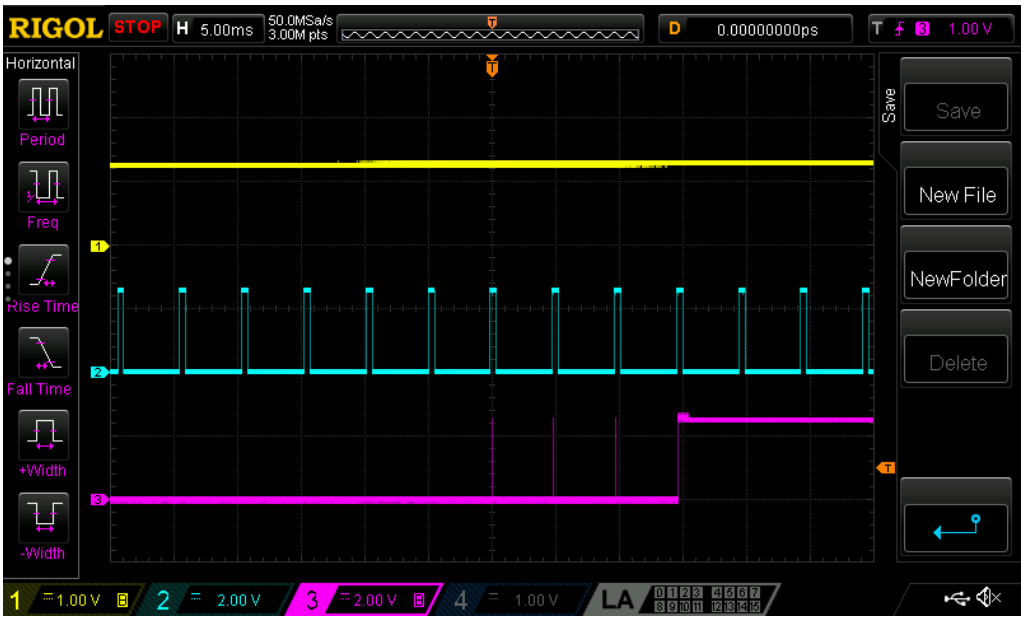

Figure 11: Zoomed ACMP Output during Glitching at Normal wake time mode

3.4.4 Workaround

1. If ACMP is used with WS Ctrl counter, CNT0, avoid conditions described in paragraph 3.4.2.

2. Decrease the reference to avoid conditions described in paragraph 3.4.2 at IN- and add the IN+ gain to keep the needed threshold.

Document Revision History

Revision	Date	Description
1.2	27-Jul-2021	Added issues #3 and #4
1.1	24-Jun-2020	Updated according to new Dialog's format

SLG47105 Errata

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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