Application note

DA14580 Checklist for schematic and PCB layout

AN-B-018

Abstract

This document is a guideline and checklist for DA14580 schematics and PCB layouts.

Contents

1 Terms and definitions

ADC	Analog to Digital Converter
BLE	Bluetooth Low Energy
GPIO	General Purpose Input Output
PCB	Printed Circuit Board
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

2 References

1. DA14580 Datasheet, Dialog Semiconductor
2. AN-B-001: DA14580 Booting from Serial Interfaces, Application note, Dialog Semiconductor
3. AN-B-009: DA14580 Crystal oscillator PCB layout guidelines, Application note, Dialog Semiconductor

3 Checking the schematic and the PCB layout

3.1 GPIO ports

- For UART communication, check that preferably the UART ports P0_4 and P0_5 are used. These are the default ports for the DA14580_01, and these are part of the Boot-Sequence. If not possible, use either one of the other UART pairs: i.e. P0_0/P0_1 or P0_2/P0_3.
- When not using the ADC, make sure the voltage levels at the ports P0_0 thru P0_3 are not higher than Vbat3V in order to prevent that these signals are interfering with internal ADC measurements.
- In case the ADC is being used, check that the voltages at the ADC input ports, P0_0 thru P0_3, are not higher than Vbat3V + 0.2V and never exceeding the maximum level of 3.45 V.
- When an external SPI slave device is used for booting, make sure following ports are being used: P0_0, P0_3, P0_5 and P0_6 for resp. SCK, CS, MISO and MOSI.
  For details, see *"Table 4: Development Mode Peripheral Pin Mapping"* in the datasheet.
- Refer also to Application Note *AN-B-001.pdf.*

3.2 16 MHz crystal oscillator

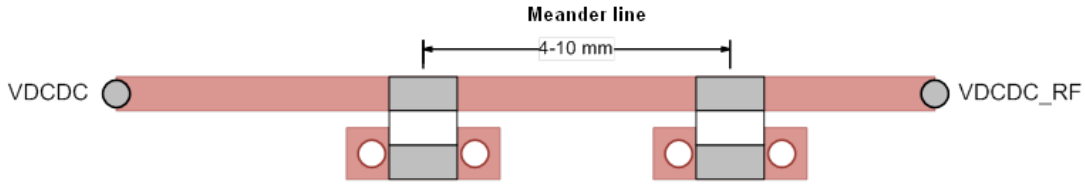
- Select a crystal having a max. ESR lower than 100 Ohm. Higher ESR values will increase the 16 MHz crystal oscillator start-up time. For crystals having 50 to 80 Ohm ESR values, start-up time is about 2 to 2.5 msec, for crystals having ESR of 100 Ohm or higher, it can be as long as 4 or 5 msec. Take this into account. Smaller sized 16 MHz crystal packages (e.g. size 2016) tend to have higher ESR values than larger cans (e.g. size 3225) have.
- No additional load capacitors required, also no capacitor pads foreseen on the PCB.
  The required crystal load capacitors are provided internally. The stray capacitance to the 16 MHz crystal really must be minimised to avoid cross-talk to the 16 MHz oscillator.
- Keep the connections to the 16 MHz crystal as short as possible to minimize picking up interference or noise.
- Keep UART lines, debug lines and other clock lines away from the 16 MHz crystal oscillator. This yields also for traces at the underlying layer, which may be a ground plane. The oscillator is very sensitive and is easily disturbed which may lead to un-stable BLE operation when e.g. clock signals are running by closely.
- Most sensitive ports for the 16MHz crystal oscillator are P1_2 and P1_3; these ports will generate much cross-talk to the 16 MHz oscillator when toggled fast. Make sure these ports are not toggling when the 16 MHz oscillator is active. It is safe to use them for static purposes, though.
- Refer also to Application Note *AN-B-009.pdf.*

3.3 32 kHz crystal oscillator

- If the used 32KHz crystal has required load capacitance in the range of 6 - 7 pF, no additional load capacitors are required. Please, also do not place capacitor pads on the PCB. Only if the required load capacitance is higher than 7 pF, add additional capacitance to the Xtal32K pins. Please note that the maximum allowed load capacitance is 9 pF.
- Although less critical than the 16 MHz crystal oscillator, keep its connections short.
- Port P2_2 of the QFN40 package and port P3_3 of the QFN48 package potentially can disturb the 32KHz crystal oscillator. Don't let traces connected to these ports run close or parallel to the Xtal32Kp side of the Xtal32K oscillator.

3.4 VDCDC and VDCDC_RF filtering and decoupling

- Good filtering and decoupling of the VDCDC output from the VDCDC_RF supply pin is important for a good RF performance. The 1uF decoupling capacitors should be placed as close as possible to the supply pins.
  This is of special importance in a boost mode system, where VBAT1V might be close to VDCDC. In this case the noise at VDCDC is high and RF performance is affected. In this case a higher decoupling capacitor (e.g. 2uF) might be needed.
  In rare cases, where VBAT1V will be close to VBAT3V, placing a 1uF capacitor at VBAT3V and VBAT_RF is recommended.
- **Inductor:** choose a type with a high resonance frequency, preferably higher than 75 MHz. This results in a lower stray capacitance and minimises the HF noise at VDCDC_RF. Its maximum rated current should be at least 80mA for a buck-mode application, preferably 100mA or higher. When the inductor is in saturation, it cannot operate well anymore, resulting in high HF-noise and HF-ripple and worse BLE performance. An inductor value of 2.2 µH is recommended.
- **Capacitors:** use a 1 µF value for both filtering caps at VDCDC and VDCDC_RF, preferably low inductance types or 0201 (0603M) sized ceramic multilayer capacitors, e.g. 1µF, 6.3V, X5R types. For grounding, try to minimize the mounted inductance. Provide either “via in pad” if possible, or if not possible, use double vias as in below picture.
- Use a meander-shaped trace with a length of about 7 mm between the VDCDC pin and the VDCDC_RF pin. This inductance reduces the HF-noise and HF-ripple at the VDCDC_RF pin.



VDCDC_RF filtering and decoupling

3.5 Buck- or Boost-mode

- Check the schematic for correct Buck- or Boost-Mode configuration.

3.6 Debugging interface

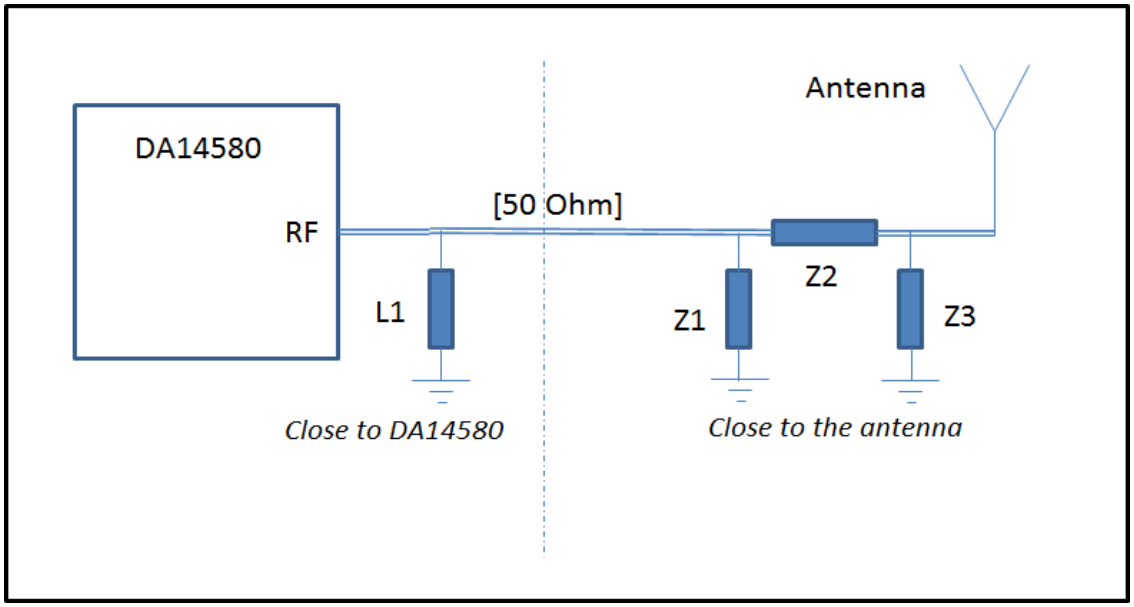
- Check for availability of following signals on e.g. test-points, pins or a header in order to have easy access to them for programming and for debugging:
  JTAG SW_CLK and SWDIO, UART RX, UART TX, VPP, Vbat3V, GND, Reset.

3.7 RF input and output matching

- For optimal matching of the DA14580 to 50 Ohm, make sure to place a shunt inductor as close as possible to the RFIO pin. The value of this shunt inductor depends on the package.
  WL-CSP package: 3.3nH inductor; both QFN packages: 3.9nH inductor.
  This shunt inductor is L1 in below figure in section 3.7.1.
  This matching ensures best RF sensitivity and highest RF output power.
- Further, foresee some matching components for antenna matching; these parts should be close to the antenna. Most universal is a PI matching network, having two shunt components and one series component: Z1, Z3 and Z2. Type and value fully depend on the antenna type, but typically

small pF caps and low nH inductor values are expected here.Maybe not all three parts are required to have a good matching. The connecting PCB trace should have a characteristic impedance of 50 Ohm. See picture in section 3.7.1.
The free Agilent tool 'AppCad' can calculate the characteristic trace impedances when substrate and trace dimensions are known. Also online RF calculators are available.

3.7.1 DA14580 Antenna matching circuit

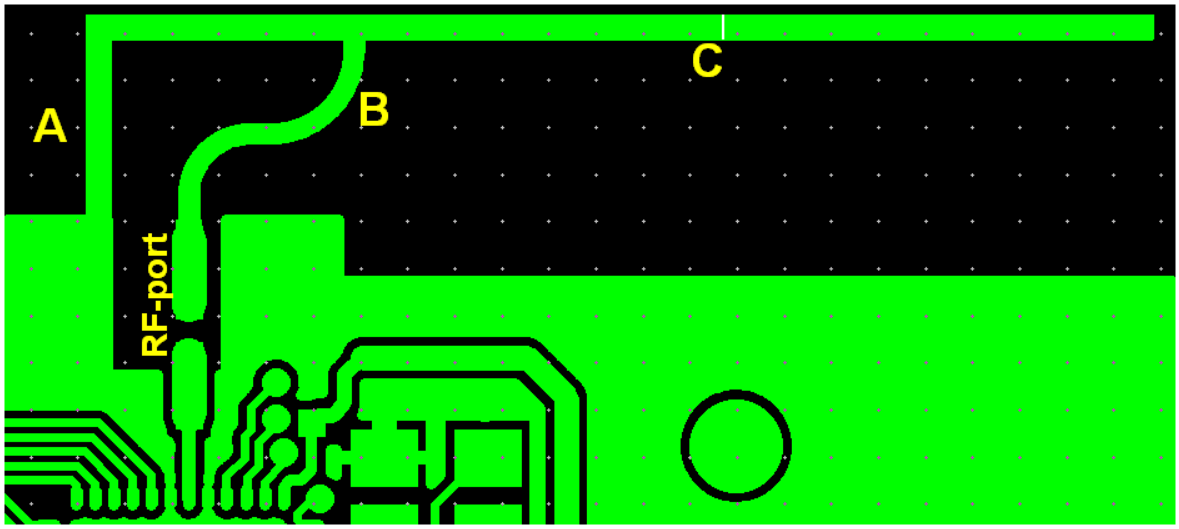


3.7.2 Antenna placement

Whether a PCB printed antenna is being used, or e.g. a ceramic chip antenna, make sure no copper is under the antenna, and no traces are running under the antenna area. The antenna must be able to radiate freely. The ceramic chip antenna mostly requires some copper-free area around it; refer to the antenna manufacturer's antenna layout guide.

3.7.3 Printed antenna example

Below the printed PCB antenna used in the Dialog's Keyboard Reference Design is shown. The design is a so-called inverted F-antenna. One can copy and paste this design on any PCB material. Gerber files and design files can be provided.



PCB Antenna in Keyboard Reference Design

Measures of the shown printed antenna:

A 4 mm long, 0.53 mm wide – this is for the vertical part only

B 5 mm long, 0.40 mm wide – the antenna feed trace

C 23 mm long in total, 0.53 mm wide – the section between A - B is 5.5 mm long

The grid size in above picture is 1 mm

A PI-network for antenna matching components is provided too. Please make sure this matching circuit is present in your design. The antenna free space area should be 25 mm x 6 mm. Under and in this area there should be no ground planes, no traces and no components.

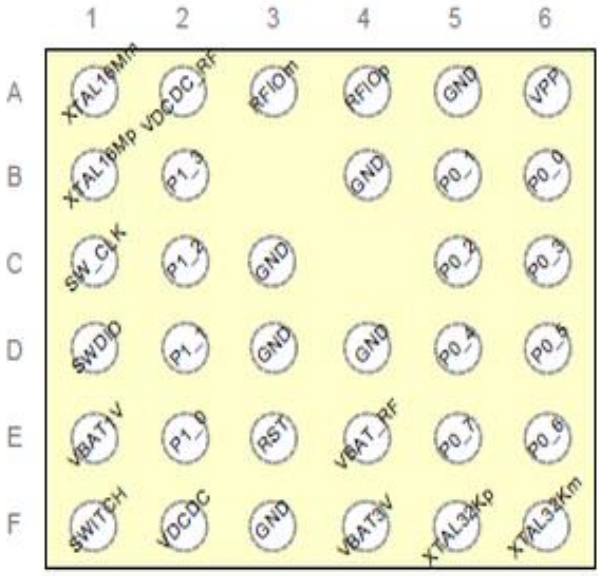
A very similar printed antenna is being used on Dialog's new (2014) evaluation kits.

4 PCB layout examples

4.1 WLCSP package: PCB design examples for 16 MHz crystal

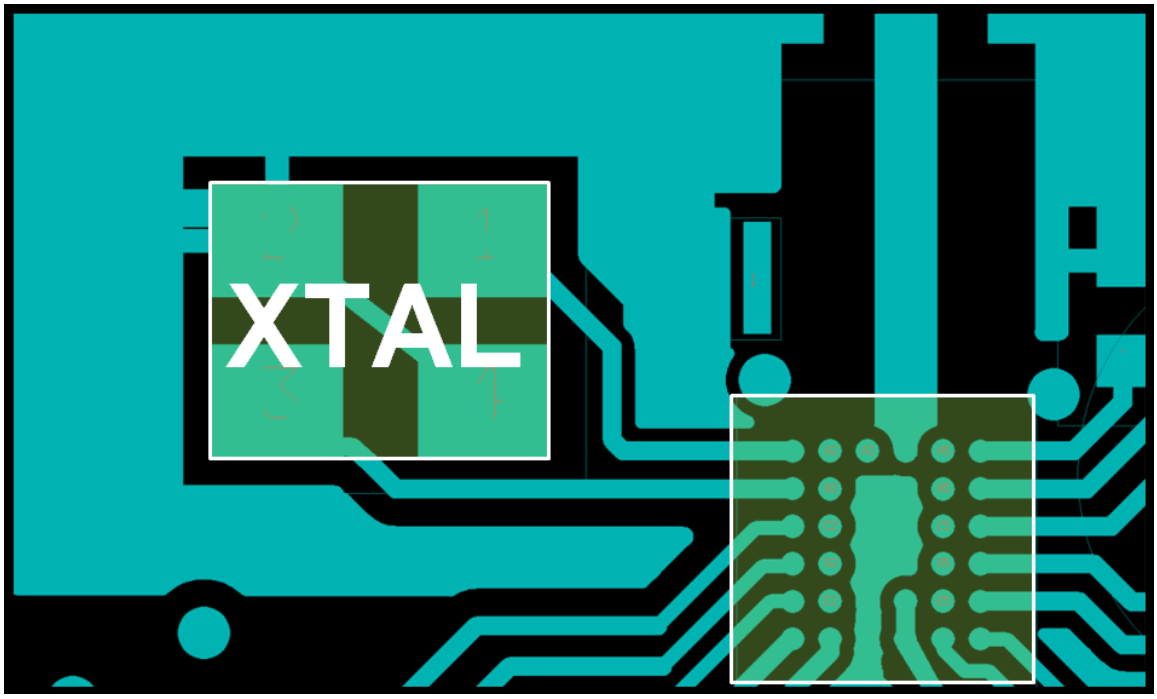
The following paragraphs show some design examples for the DA14580 WLCSP package with different PCB structures. For the WLCSP package the inner ring connections (P1_0, P1_1, P1_2, P1_3, P0_1, P0_2, P0_4 and P0_7) can only be used with a Multi-layer PCB with micro vias. When micro vias are used it is recommended to place the micro vias in the middle of the balls/connections of the device.

4.1.1 DA14580 WLCSP ball pattern



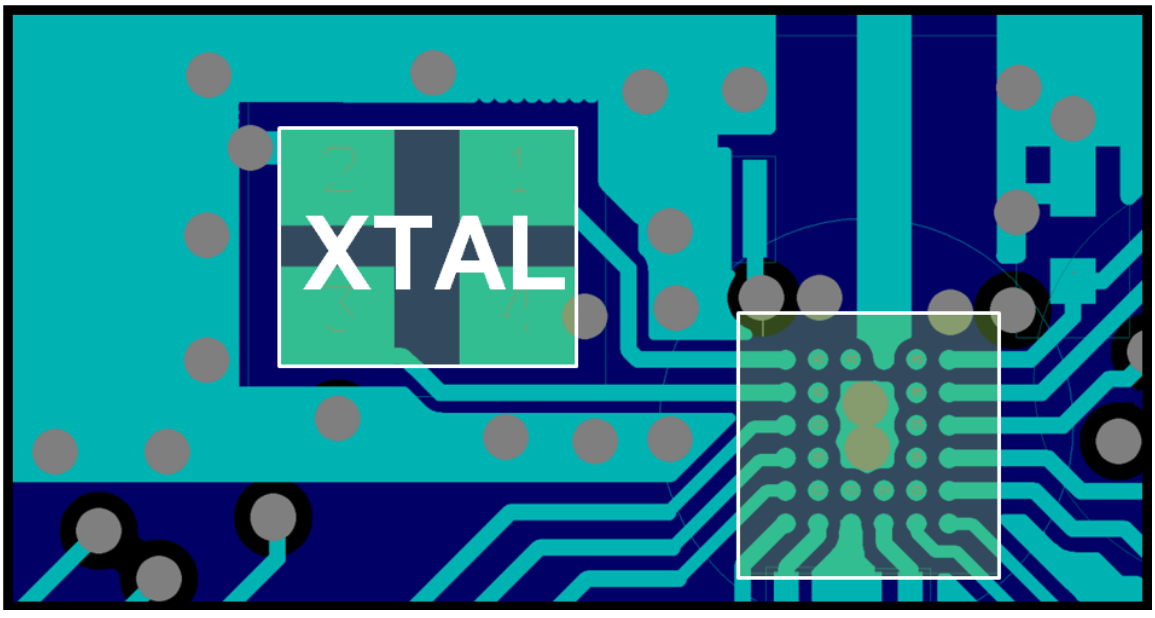
Top View

4.1.2 Single-layer PCB



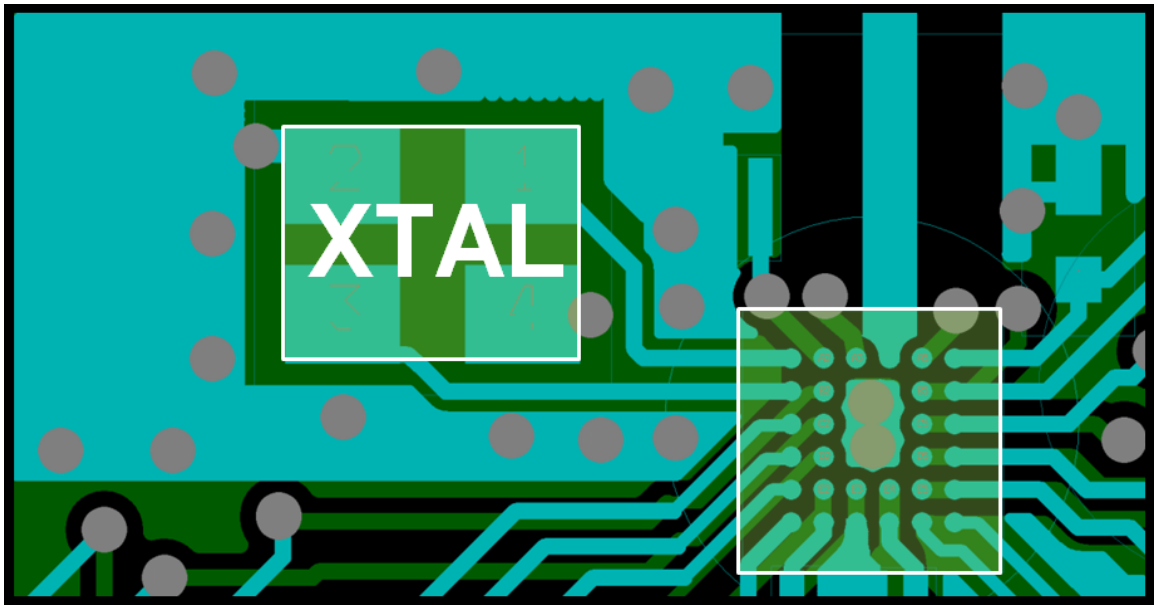
The crystal is surrounded by a guard ring. This guard ring is connected to ground. Both crystal case ground connections are connected to ground. The inner ring of the DA14580 is not used since there is not enough space to route to these pins.

4.1.3 Multi-layer PCB with regular vias



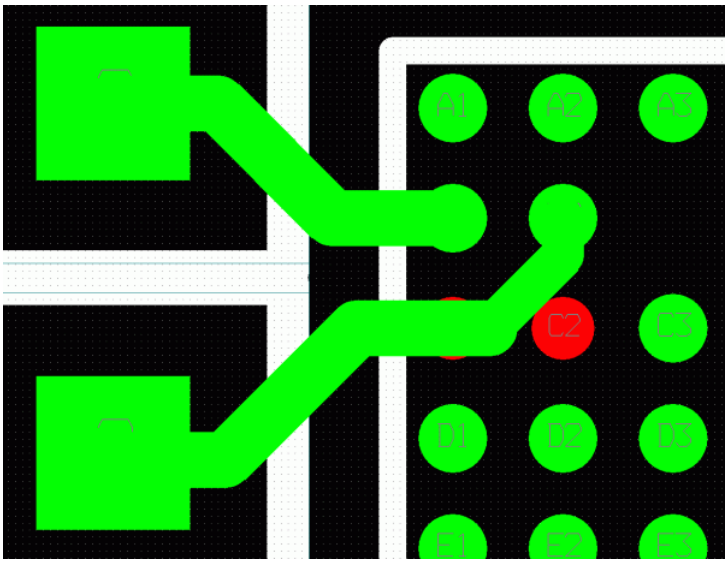
The oscillator circuit is shielded by a ground plane. The crystal is surrounded by a guard ring. This guard ring is connected to the ground plane using vias. Both crystal case ground connections are connected to ground. There should be no wires between the oscillator circuit and the ground plane. The inner ring of the DA14580 is not used since there is not enough space to route to these pins when using regular vias.

4.1.4 Multi-layer PCB with micro vias



The oscillator circuit is shielded by a ground plane. The crystal is surrounded by a guard ring. This guard ring is connected to the ground plane using vias. Both crystal case ground connections are connected to ground. There should be no wires between the oscillator circuit and the ground plane. The micro vias used to connect the inner pins of the DA14580 are located directly under the pads. This makes it possible to route the GPIO lines and e.g. the JTAG lines directly away from the oscillator circuit.

4.2 Single-layer PCB with access to a ball on an inner ring:



An illustration example for having access to ball B2: two pins have to be sacrificed for this, in above example these are pins C1 and C2. This could be used for access to e.g. P0_4 for having UART communication at P0_4/P0_5, either ports P0_2/P0_3 or P0_6/P0_7 have to be sacrificed.

5 Revision history

Revision	Date	Description
0.1	18-Febr-2014	Initial version.
0.2	20-May-2014	Updated for VDCDC decoupling. Template updated to latest version. Back page: contact information updated.
1.0	20-May-2014	Final reviewed version.
1.1	22-Aug-2014	Updated sections 3.3 and 3.6
1.2	25-Apr-2018	Updated section 3.4.

Status definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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RoHS Compliance

Dialog Semiconductor complies to European Directive 2001/95/EC and from 2 January 2013 onwards to European Directive 2011/65/EU concerning Restriction of Hazardous Substances (RoHS/RoHS2).
Dialog Semiconductor's statement on RoHS can be found on the customer portal https://support.diasemi.com/. RoHS certificates from our suppliers are available on request.

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