

Application Note Class-D Audio Amplifier AN-CM-216

Abstract

This application note shows how to create a Class-D Audio Amplifier using GreenPAK™ SLG46140V. This application note comes complete with design files which can be found in the References section.

AN-CM-216



Class-D Audio Amplifier

Contents

Ab	stract	.1
Со	ntents	.2
Fig	ure s	.2
	Terms and Definitions	
2	References	.3
3	Introduction	.4
4	Input and Output Signals	.4
5	GreenPAK Design	.6
6	Results	.9
7	Conclusion	12
Re	vision History	13

Figures

Figure 1: Timing Diagrams for the Different Stages of the Class D Audio Amplifier	4
Figure 2: Circuit Diagram	5
Figure 3: GreenPAK Design	
Figure 4: VREF Properties	6
Figure 5: ACMP0 Properties	7
Figure 6: PWM Output Relative to ADC Value	7
Figure 7: Break-Before-Make Outputs	8
Figure 8: pFET0 and nFET1 are ON	8
Figure 9: pFET1 and nFET0 are ON	9
Figure 10: System Input is a 262 Hz Sine Wave (middle C)	10
Figure 11: 70% Output Duty Cycle, ANALOG_IN ≈ 700 mV	10
Figure 12: 50% Output Duty Cycle, ANALOG IN ≈ 550 mV	11
Figure 13: 30% Output Duty Cycle, ANALOG_IN ≈ 400 mV	
Figure 14: Amplified Output	

AN-CM-216

Class-D Audio Amplifier



1 Terms and Definitions

ACMP	Analog comparator module
ADC	Analog to digital converter
CNT	Counter
DLY	Delay
LC	Inductor and capacitor
PWM	Pulse-width modulation
VREF	Voltage-reference

2 References

For related documents and software, please visit:

https://www.dialog-semiconductor.com/configurable-mixed-signal.

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Dialog Semiconductor provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Dialog IC.

- [1] GreenPAK Designer Software, Software Download and User Guide, Dialog Semiconductor
- [2] AN-CM-216 Class-D Audio Amplifier.gp, GreenPAK Design File, Dialog Semiconductor
- [3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Dialog Semiconductor
- [4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Dialog Semiconductor
- [5] SLG46140V, Datasheet, Dialog Semiconductor

3 Introduction

In this app note, we will use a Dialog GreenPAK[™] SLG46140V to create a Class-D Audio Amplifier. A Class-D amplifier takes an analog audio signal, converts it into a digital PWM signal, and then filters the PWM signal to recapture the analog signal with a greater amplitude for greater volume.

4 Input and Output Signals

Figure 1 shows the input and output signals used in this app note. The analog waves that come out of an iPhone headphone jack are centered around 0 v and have an amplitude of between 1-2 v. We need to process that analog signal through our GreenPAK's ADC (analog to digital converter), but the GreenPAK ADC can only convert positive values from 50 mv to 1200 mv. This means that the first thing we need to do is add a 600 mv DC offset to the input signal. The amplitude of the input signal remains the same, but it is now centered around 600 mv as shown in Step 2 of Figure 1.

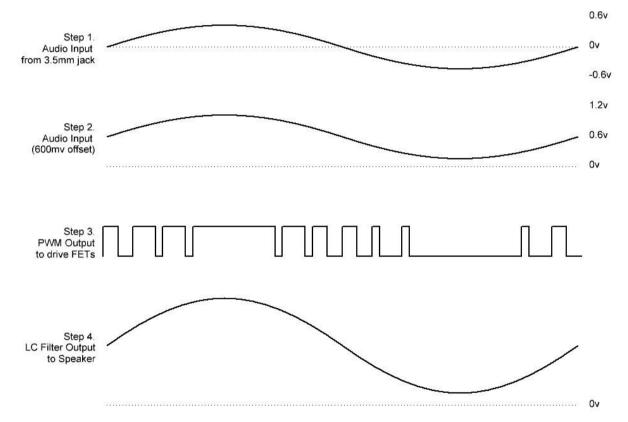


Figure 1: Timing Diagrams for the Different Stages of the Class D Audio Amplifier

We can do that by adding a series capacitor and a resistive divider to our circuit, as shown in Step 2 of Figure 2. The voltage coming out of the GreenPAK's Pin3 is 1.2 v, which means that the waveform that enters Pin6 will be centered around 0.6 v. We'll discuss how to create that 1.2 v rail in the GreenPAK Design section.

The GreenPAK takes the voltage that it receives at Pin6 and converts it into several different PWM signals which are output on Pins 9-12. Those signals are used to control the gates of 4 MOSFETs which are configured as an H-Bridge. In order to maximize the voltage potential across the speaker, pFET0 and nFET1 are turned on at the same time, and pFET1 and nFET0 are turned on at the same time.

Application Note	Revision 1.0	24-Nov-2017



To recreate our analog input signal, we added a pair of LC filters to both sides of the H-Bridge. The outputs of both filters are connected to the speaker terminals.

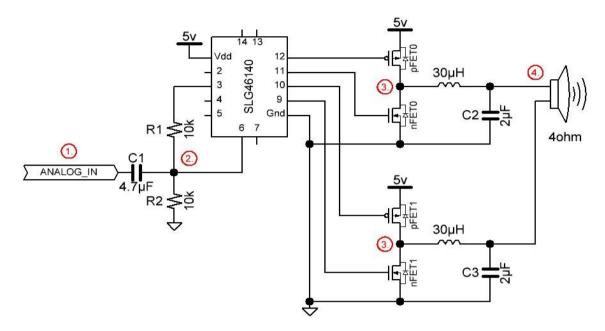


Figure 2: Circuit Diagram

We desired a cutoff frequency of 20kHz, since that is the upper range of human hearing. We measured the speaker impedance at 4Ω , and used those values to calculate the capacitance and inductance needed for our LC filters.

 $L = \frac{Z}{2\pi f_c} = \frac{4}{2\pi * 20000} = 31.8\mu H \approx 30\mu H$ $C = \frac{1}{2\pi f_c Z} = \frac{1}{2\pi * 20000 * 4} = 1.989\mu F \approx 2\mu F$



5 GreenPAK Design

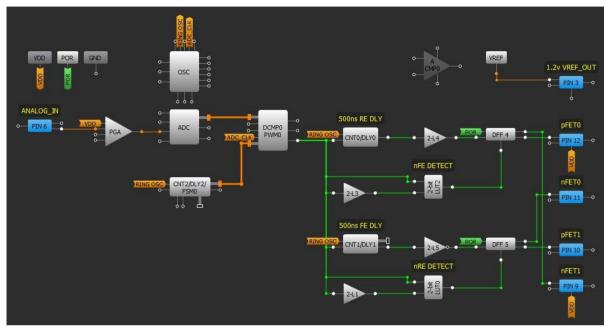


Figure 3: GreenPAK Design

The first thing we needed to do in the GreenPAK design was to create a 1.2 v rail to help add the 600 mV offset to our input signal. We accomplished this by configuring the VREF block so that it outputs the ACMP0 threshold to Pin3. We set ACMP0's threshold to 1200 mV as shown in Figure 5.

Properties		×
	VREF	
Chopper clock frequency:	2 MHz	•
Opamp offset chopper:	Enable	(V)
Source selector:	ACMP0 IN-	*
A CMP0 reference volt.	1200 mV	*
A CMP1 reference volt.	50 mV	¥
Con	nections	
Output	PIN 3	v
Power	ctrl. settings	-

Figure 4: VREF Properties



Properties		×
A	CMP0	
Hysteresis:	Disable	•
Low bandwidth:	Disable	•
Input 100uA current source:	Disable	•
IN+ gain:	Disable	•
Con	inections	
IN+ source:	PIN 10	•
IN- source:	1200 mV	•

Figure 5: ACMP0 Properties

Pin6 receives the analog input signal with the 600 mV offset. The signal is passed through the PGA with a gain of x1, and then is converted into an 8-bit value by the ADC. Meanwhile, CNT2/DLY2 is configured as an 8-bit ripple counter and its clock line is connected to the GreenPAK's 25 MHz RING oscillator. CNT2's count value starts at 255, and every time it is clocked the count value is decremented. When CNT2 has counted 255 clocks, it rolls over to 255 and continues to count down. The DCMP0/PWM0 block is used to generate a PWM output so that when the ADC value is greater than the CNT2 value, the DCP0/PWM0 block outputs HIGH, as shown in Figure 6. This means that when the Analog voltage at Pin6 is higher, the ADC will output a bigger 8-bit number, and the DCMP's output pulse length will be longer.

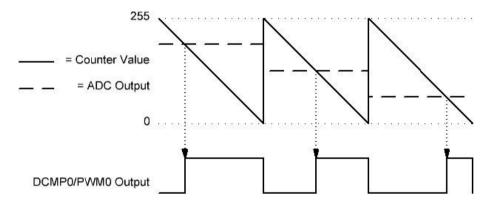


Figure 6: PWM Output Relative to ADC Value

The output of the DCMP0/PWM0 block is sent through some break-before-make circuitry to ensure that our external H-bridge works properly. We want to make sure that pFET0 and nFET0 are never turned on at the same time, which would short our power supply to ground. Likewise, we never want pFET1 and nFET1 to be turned on at the same time.

We used delay blocks, DFFs, and edge detectors to create the break-before-make circuitry. When the output of DCMP0 goes HIGH, the rising edge detector composed of 2-bit LUT1 and 2-bit LUT0 is used to reset DFF5, which turns off both nFET0 and pFET1. 500 ns later, DLY0 clocks POR through DFF4, which will turn on nFET1 and pFET0. The same timing occurs in the inverse when there is a falling edge on the output of DCMP0.

Ann	lication	Noto
Abb	lication	NOLE



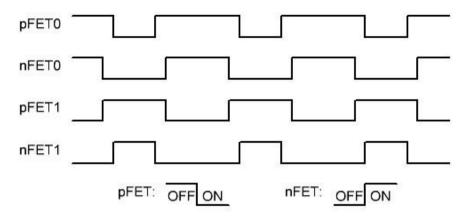


Figure 7: Break-Before-Make Outputs

When opposite sides of the H-Bridge are ON at the same time, the full power supply voltage can be delivered to the speaker.

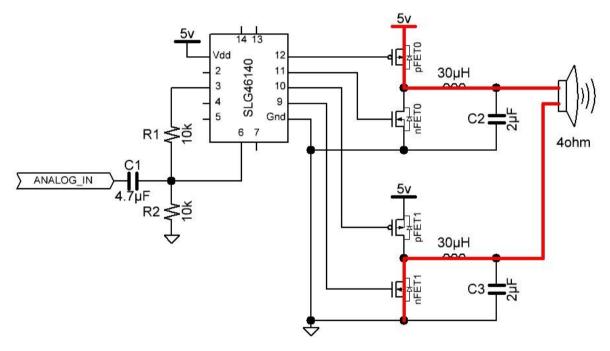


Figure 8: pFET0 and nFET1 are ON



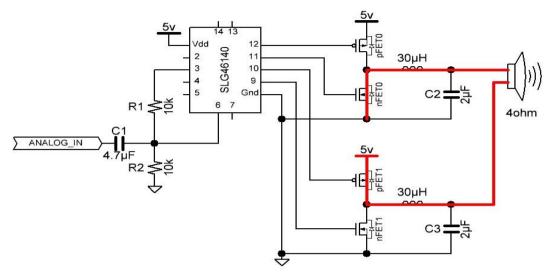


Figure 9: pFET1 and nFET0 are ON

The LC filters smooth out the outputs to create a less choppy signal, thus recreating the original audio waveform.

6 Results

In the following oscilloscope waveforms, the channels were connected to the following signals:

Channel 1 (yellow) – Output from 3.5 mm audio jack

Channel 2 (blue) - Pin6 (ANALOG_IN)

Channel 3 (pink) – Pin9 (nFET1)

Channel 4 (dark blue) – Output of top LC filter

We tested our circuit with a 262 Hz sinewave, which corresponds to the note "Middle C." As you can see in Figure 10, the ANALOG_IN signal has a 600 mV DC offset from the audio jack output. In Figure 10, we disconnected the GreenPAK's Pins 9-12 to reduce switching noise.





Figure 10: System Input is a 262 Hz Sine Wave (middle C)

If we enable Pins 9-12 and zoom in, we can see the duty cycle of Pin9 change at different points in the sinewave. We also encounter some switching noise. This is shown in Figure 11, Figure 12, and Figure 13.



Figure 11: 70% Output Duty Cycle, ANALOG_IN ≈ 700 mV



Figure 12: 50% Output Duty Cycle, ANALOG_IN ≈ 550 mV



Figure 13: 30% Output Duty Cycle, ANALOG_IN ≈ 400 mV

In Figure 14, when we zoom back out you can see that the input waveform has been amplified by our circuit and the output is the same frequency as the input. To hear the amplifier in action, watch the video connected to this app note.



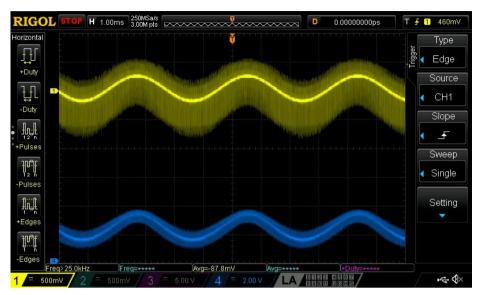


Figure 14: Amplified Output

7 Conclusion

In this app note we created a Class-D amplifier with a Dialog GreenPAK SLG46140V and a few passive external components. We created a DC offset to prepare the input signal to be processed by the GreenPAK's ADC and used an H-Bridge with a pair of LC filters on the output to recreate the input signal.

Since this design only uses about half of the digital logic resources inside the SLG46140V, a designer could use the rest of the logic blocks to add more functionality to the design.



Revision History

Revision	Date	Description
1.0	24-Nov-2017	Initial Version



Status Definitions

Status Definition		
DRAFT	RAFT The content of this document is under review and subject to formal approval, which may result in modifications of additions.	
APPROVED or unmarked	The content of this document has been approved for publication.	

Disclaimer

Information in this document is believed to be accurate and reliable. However, Dialog Semiconductor does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information. Dialog Semiconductor furthermore takes no responsibility whatsoever for the content in this document if provided by any information source outside of Dialog Semiconductor.

Dialog Semiconductor reserves the right to change without notice the information published in this document, including without limitation the specification and the design of the related semiconductor products, software and applications.

Applications, software, and semiconductor products described in this document are for illustrative purposes only. Dialog Semiconductor makes no representation or warranty that such applications, software and semiconductor products will be suitable for the specified use without further testing or modification. Unless otherwise agreed in writing, such testing or modification is the sole responsibility of the customer and Dialog Semiconductor excludes all liability in this respect.

Customer notes that nothing in this document may be construed as a license for customer to use the Dialog Semiconductor products, software and applications referred to in this document. Such license must be separately sought by customer with Dialog Semiconductor.

All use of Dialog Semiconductor products, software and applications referred to in this document are subject to Dialog Semiconductor's Standard Terms and Conditions of Sale, available on the company website (www.dialog-semiconductor.com) unless otherwise stated.

Dialog and the Dialog logo are trademarks of Dialog Semiconductor plc or its subsidiaries. All other product or service names are the property of their respective owners.

© 2018 Dialog Semiconductor. All rights reserved.

Contacting Dialog Semiconductor

United Kingdom (Headquarters)

Dialog Semiconductor (UK) LTD Phone: +44 1793 757700

Germany

Dialog Semiconductor GmbH Phone: +49 7021 805-0

The Netherlands

Dialog Semiconductor B.V. Phone: +31 73 640 8822

Email:

enquiry @diasemi.com

North America

Dialog Semiconductor Inc. Phone: +1 408 845 8500

Japan

Dialog Semiconductor K. K. Phone: +81 3 5769 5100

Taiwan

Dialog Semiconductor Taiwan Phone: +886 281 786 222

Web site: www.dialog-semicond

www.dialog-semiconductor.com

Hong Kong

Dialog Semiconductor Hong Kong Phone: +852 2607 4271

Korea

Dialog Semiconductor Korea Phone: +82 2 3469 8200

China (Shenzhen)

Dialog Semiconductor China Phone: +86 755 2981 3669

China (Shanghai)

Dialog Semiconductor China Phone: +86 21 5424 9058

Application Note

Revision 1.0