Application Note

Over Current Latch with Low Side Sense

AN-CM-223

Abstract

The design in this application note uses a single Dialog GreenPAK™ SLG46110V to realize a low-side sensing over current detection circuit with a latching output used to enable/disable an external high-side PMOS load switch.

This Application Note comes complete with design files which can be found in the References section.

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1 Terms and Definitions

PMOS	P-type metal-oxide-semiconductor logic
PGA	Programmable-gain amplifier

2 References

For related documents and software, please visit:

https://www.dialog-semiconductor.com/configurable-mixed-signal.

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Dialog Semiconductor provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Dialog IC.

[1] GreenPAK Designer Software, Software Download and User Guide, Dialog Semiconductor

[2] AN-CM-223 Over Current Latch with Low Side Sense.gp, GreenPAK Design File, Dialog Semiconductor

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Dialog Semiconductor

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Dialog Semiconductor

[5] SLG46110V, Datasheet, Dialog Semiconductor

[6] Darmawaskita, Hartono, Get Extra Op Amps by Using Spare Comparators, Electronic Design 24 May 2004: n. pag. Web.

Authors: Michael Quinn and David Riedell

3 Introduction

This design uses a single Dialog GreenPAK SLG46110V to realize a low-side sensing over current detection circuit with a latching output used to enable/disable an external high-side PMOS load switch. By configuring one of the onboard comparators (ACMP1) to perform as a non-inverting amplifier with a gain of 22.5 (See attached application note), we can use a very small 0.010 Ω low-side sense resistor to, in this case, detect a 4 A maximum current. Figure 1 shows the full circuit schematic while Figure 2 shows the internal design of the SLG46110V GreenPAK circuit.

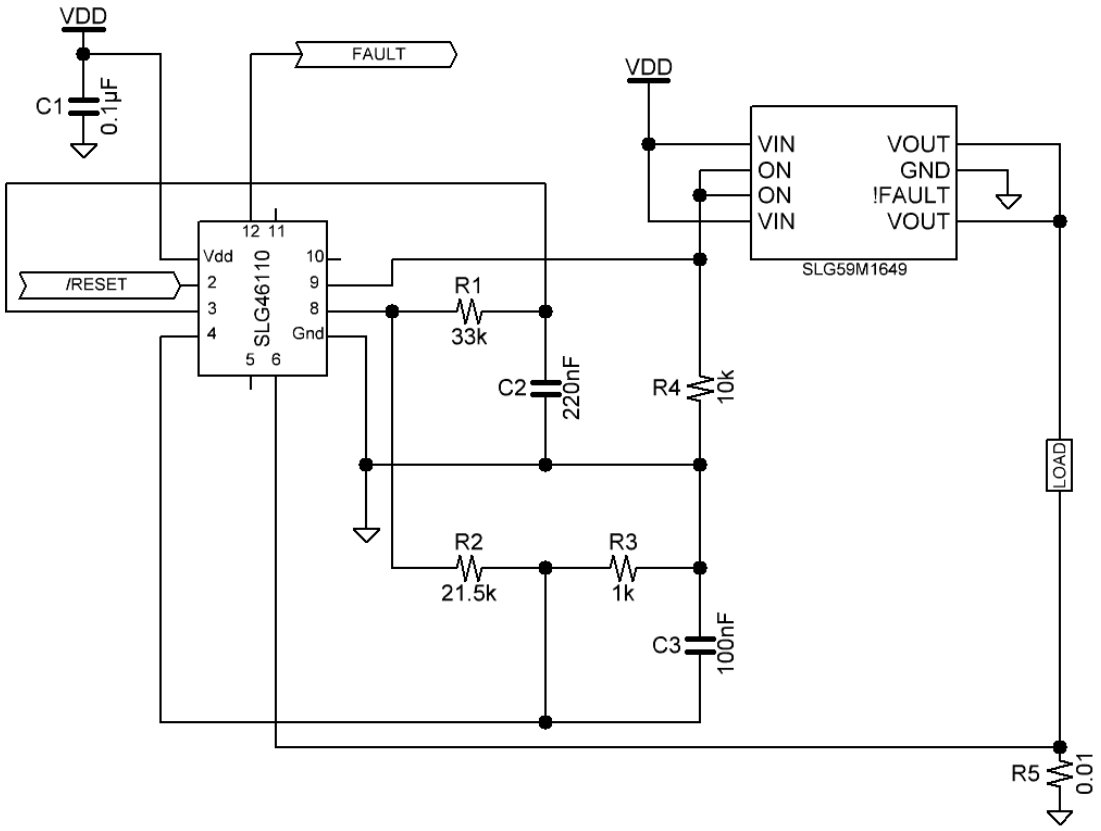

Figure 1: Application Circuit

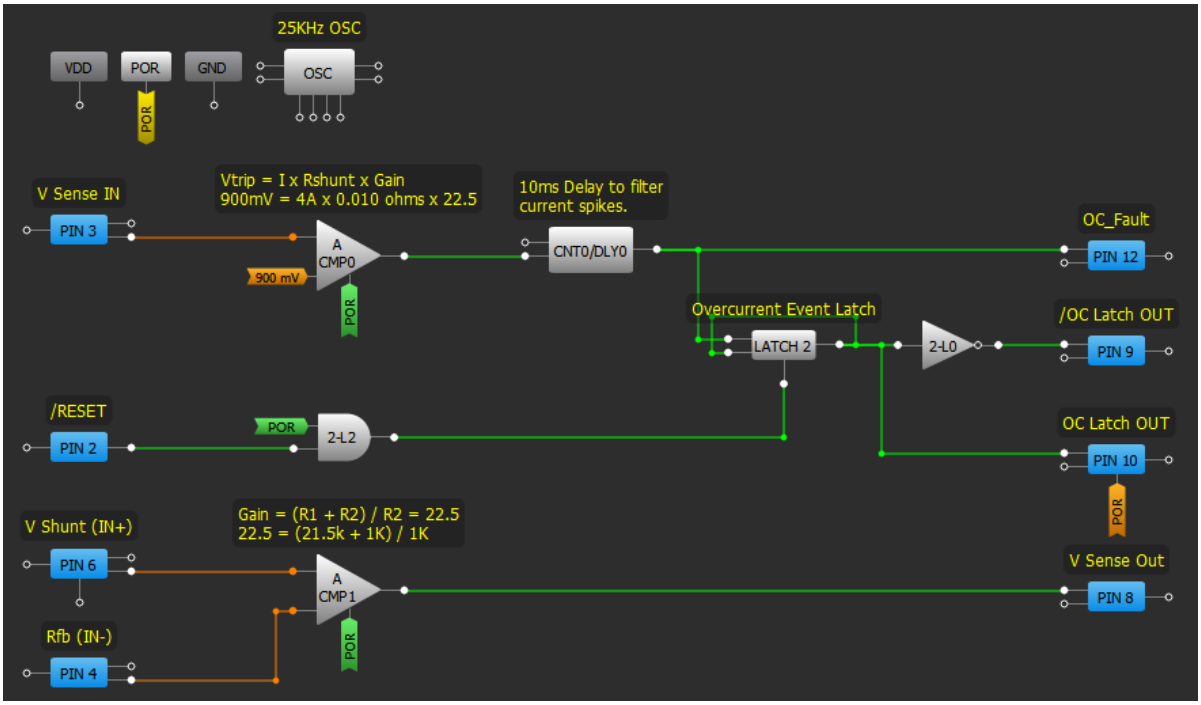

Figure 2: GreenPAK Design

The circuit functions as follows and the associated simulation waveforms are given in Figure 3. Once the 4 A limit is exceeded (shown by the yellow trace), the output of ACMP0 will trip HIGH, setting both the output of Latch 2 and the OC_FAULT output HIGH (shown by the green trace). The /OC_LATCH_OUT and OC_LATCH_OUT outputs are tied to the output of Latch 2, so when the Latch 2 output goes HIGH, the /OC_LATCH_OUT output goes LOW and turns OFF the load switch. Once tripped, the /OC_LATCH_OUT output on Pin 9 will remain LOW, even if the overcurrent event is gone, keeping the external load switch turned OFF. If the overcurrent condition is now cleared, the output of ACMP0 will go LOW, thus the OC_FAULT output will now go LOW, as it follows the output state of ACMP0. However, the /OC_LATCH_OUT output will remain latched LOW. In this event, the micro can now look at the OC_FAULT signal, determine that the over current event has been corrected, and send a LOW going pulse to the /RESET input on Pin 2 (shown by the orange trace). The low going pulse on the /RESET input will then reset the output of Latch 2 to LOW, and thus set the /OC_LATCH _OUT output HIGH, thereby turning on the external switch.

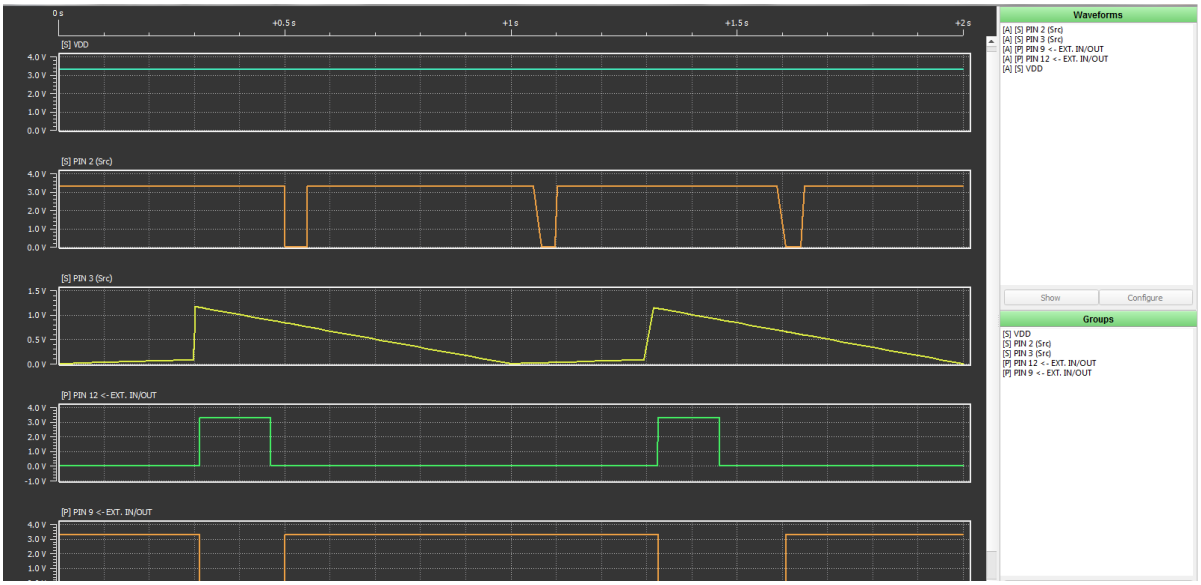

Figure 3: Simulation Waveforms

All essential parameters in the design are customizable to the needs of the application. The gain associated with ACMP1, the voltage trip level associated with ACMP0, signal polarities, load switch and sense resistor can all be configured to match the requirements needed. With the unused resources within the SLG46110V, additional features can also be added to enhance the circuit functionality. One example would be to add an “automatic retry” circuit that would automatically clear the /OC_LATCH_OUT signal after a set period of time. If the continued over current situation caused another immediate trip, the circuit would initiate another retry. It would continue to attempt to clear the /OC_LATCH_OUT signal for a preprogrammed number of times, and if unsuccessful, it would finally latch the /OC_LATCH_OUT signal LOW. At this point the external switch would be latched off until the fault is cleared and a low going pulse is input on Pin 2, /RESET.

This circuit provides a small, configurable, low cost solution for overcurrent safety functions. With the addition of a few properly selected external passive components, this solution can cover a wide range of overcurrent applications needing electronic circuit breaker functions.

4 Configuring GreenPAK Comparators as OpAmps

Often when using a GreenPAK device there is a need to add gain to an input signal in order to bring it into a measurable range for use by the ADC or the comparators. In some GreenPAK devices there is a PGA available to perform this function. The PGA is quite versatile in its configurability but the input voltage range is limited and its gain is limited to a maximum setting of x8. The SLG46110V has no internal Operational Amplifiers (OpAmps). As a result, it would be nice to have a way of incorporating some gain into your GreenPAK design without adding extra OpAmps.

One method to achieve this would be to try and adapt one of the onboard comparators for use as an OpAmp. This is something that has been done for years in highly integrated solutions where cost and size were major factors. With a bit of work and a few external R’s and C’s you can effectively make a low power OpAmp from a spare comparator in your GreenPAK design. This is by no means a high speed, high performance OpAmp solution but for many applications where gain is needed on the input signal from a sensor, we are only looking to amplify a slow-moving DC signal. For many applications such as these where we are measuring temperature or voltage across a shunt resistor, a solution such as this is more than adequate.

In order to configure one of the comparators for use as an OpAmp, we first look at the overall circuit, shown in Figure 4. The comparator is configured as a non-inverting OpAmp with V_{IN} being connected to the non-inverting input of the comparator. The inverting input of the comparator is connected to the center point of the resistive divider made up of R1 and R2, with C1 adding a bit of RC time constant to the feedback signal. The resistor, R3, in combination with C2, will act as a low pass filter, in this case yielding a 24 Hz cutoff. V_{OUT} is then the voltage across C2.

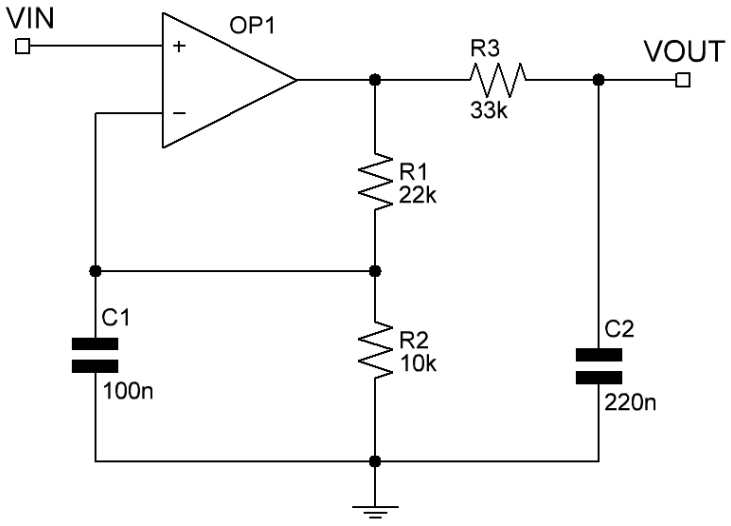

Figure 4: 12 Circuit Configured for Gain of x3.2

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The circuit functions as follows. When the voltage across C1 is less than the input voltage at V_{IN}, the output of the comparator is HIGH. This causes the voltage across C1 to rise. Once the voltage across C1 is greater than V_{IN}, the output of the comparator switches LOW. Now the voltage across C1 begins to fall until it is less than VI_N, at which point the output of the comparator switches HIGH and the cycle begins again. After many cycles the filtered average voltage seen across the output capacitor, C2, is given by the transfer function of the non-inverting amplifier.

$V_{OUT} = V_{IN} (R1 + R2) / R2$

The circuit in Figure 4 was tested and measured yielding results very close to the calculated gain of x3.2. A table of measured data is given in Table 1 along with the associated data plot for V_{OUT} vs. V_{IN} at V_{DD} = 3.3 V.

Table 1: x3.2 Gain

V_{DD} = 3.3 V	
V_{IN} (IN+) (mV)	**V_{OUT} (mV)**
4	13
101	322
201	635
300	947
400	1263
500	1579
599	1891
699	2206
798	2518
898	2835
999	3155
1099	3274

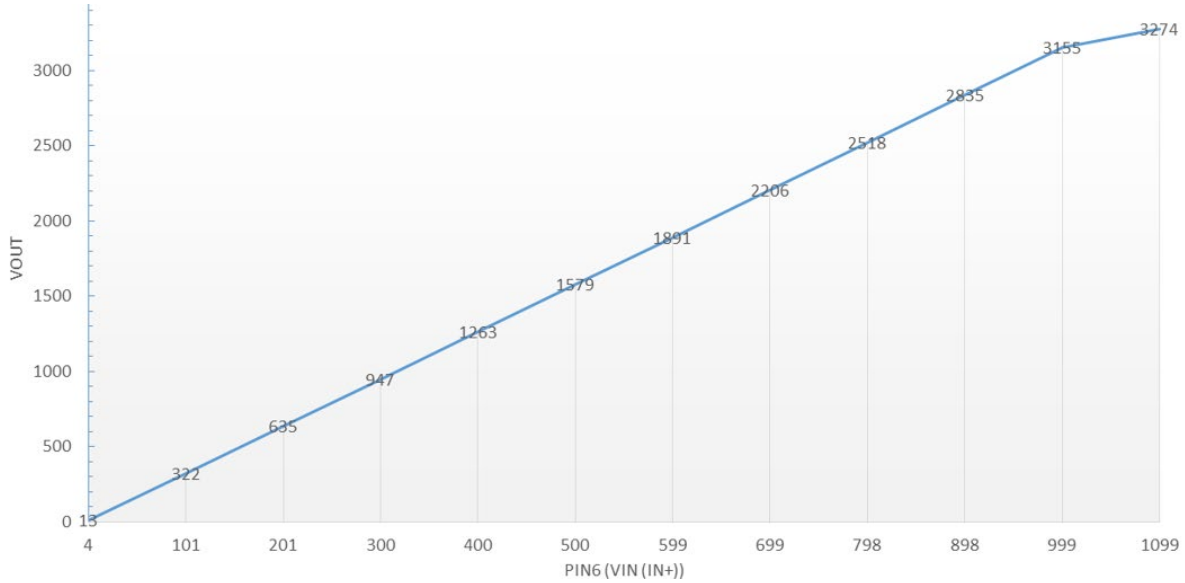

Figure 5: Graph 1. V_{IN} vs V_{OUT} at V_{DD} = 3.3 V with x3.2 Gain

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As shown in Figure 5, there is some error at both extremes of the plot when the input is near 0 V and when the output is near the 3.3 V rail. There is an offset present at the low end of the V_{OUT} vs. V_{IN} plot. This offset can be easily calibrated out of the system, if necessary, but that is not the focus of this application note. Techniques for correcting OpAmp offsets are readily available on the internet. At the high end of the plot, as we get close to the V_{DD} rail, the gain becomes slightly nonlinear. This is to be expected and illustrates the need to allow a bit of headroom below the V_{DD} rail and limit the output swing of the circuit to around V_{DD} – 300 mV or about 3.0 V max. with a V_{DD} of 3.3 V.

One additional limitation of this circuit is the input voltage range. The IN+ node at V_{IN} can normally take a voltage up to V_{DD} but the IN- node is limited to about 1.2 V. For example, a 1.5 V V_{IN} signal with the OpAmp configured for a gain of 2 and V_{DD} = 3.3 V, will cause the circuit to exceed the input voltage range of the IN- node. Once IN- is above 1.3 V, it will cause the output to go to the rail until V_{IN} is brought back down below 1.2 V. So, as a rule, it is recommended to limit the V_{IN} range to 0 < V_{IN} < 1.2 V, max.

Additional V_{IN} vs V_{OUT} data at various gains was taken for both V_{DD} = 3.3 V and V_{DD} = 5 V. That data is listed in Table 2 and plotted in Figure 6 and Figure 7. In all cases the output is very linear within the V_{IN} < 1.1 V and V_{OUT} < V_{DD} – 300 mV constraints.

Table 2: V_{IN} vs V_{OUT} Data for 3 Different Gain Settings at V_{DD} = 3.3 V and 5 V

	V_{DD} = 3.3 V	V_{DD} = 5 V	V_{DD} = 3.3 V	V_{DD} = 5 V	V_{DD} = 3.3 V	V_{DD} = 5 V
	Gain = 2		Gain = 3.2		Gain = 4.3	
V_{IN} (IN+) (mV)	V_{OUT} (mV)		V_{OUT} (mV)		V_{OUT} (mV)	
4	9	10	13	15.2	18.1	19.6
101	204.8	206.2	322	321	429	431
201	406	407	635	636	855	858
300	608	607	947	949	1277	1280
400	810	810	1263	1266	1705	1707
500	1012	1013	1579	1585	2132	2134
599	1212	1213	1891	1899	2556	2556
699	1415	1416	2206	2220	2983	2984
798	1615	1616	2518	2527	3286	3406
898	1818	1820	2835	2845	3286	3839
999	2022	2026	3155	3167	3286	4270
1099	2230	2242	3274	3506	3286	4690
					V_{DD} saturation	

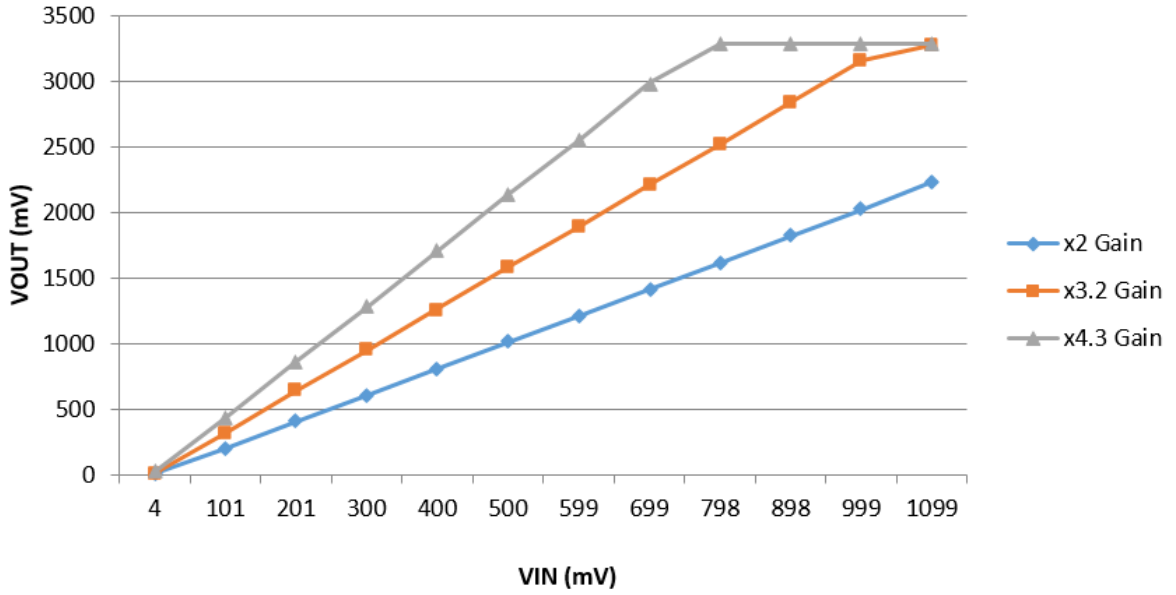

Figure 6: Graph 2. V_{IN} vs V_{OUT} for all Gain Settings at 3.3 V from Table 2 (V_{DD} = 3.3 V)

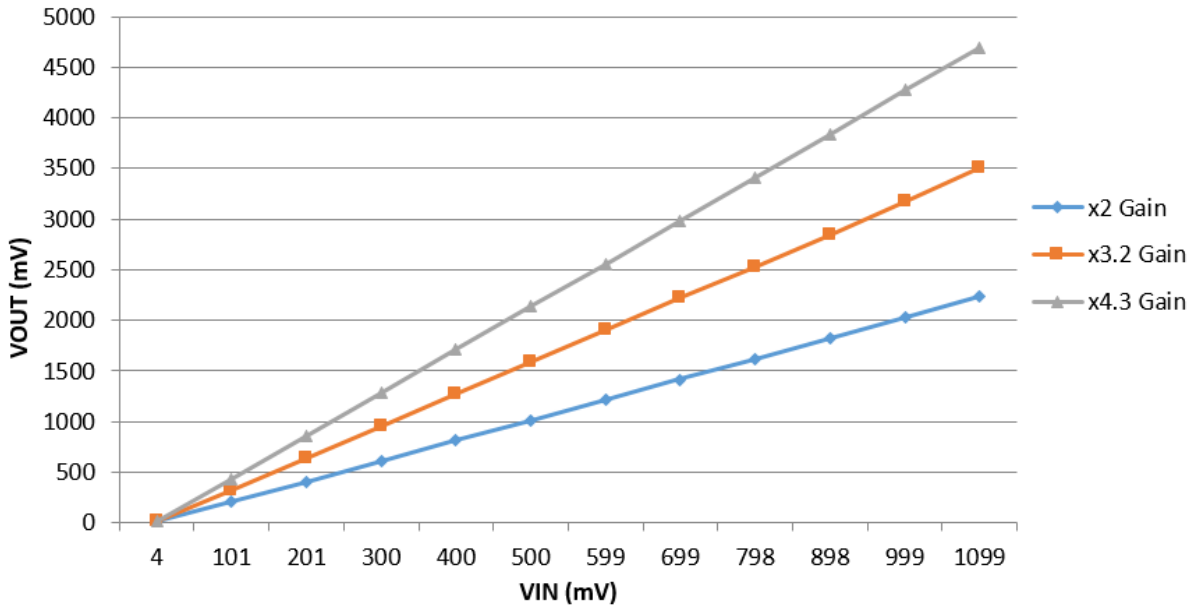

Figure 7: Graph 3. V_{IN} vs V_{OUT} for all Gain Settings at 5 V from Table 2 (V_{DD} = 5 V)

Figure 8 is a screenshot of the circuit designed into an SLG46110V. The figure shows not only the circuit but also the remaining resources and pins that are available to add other features and perform other functions. The actual GreenPAK design program file is attached as well.

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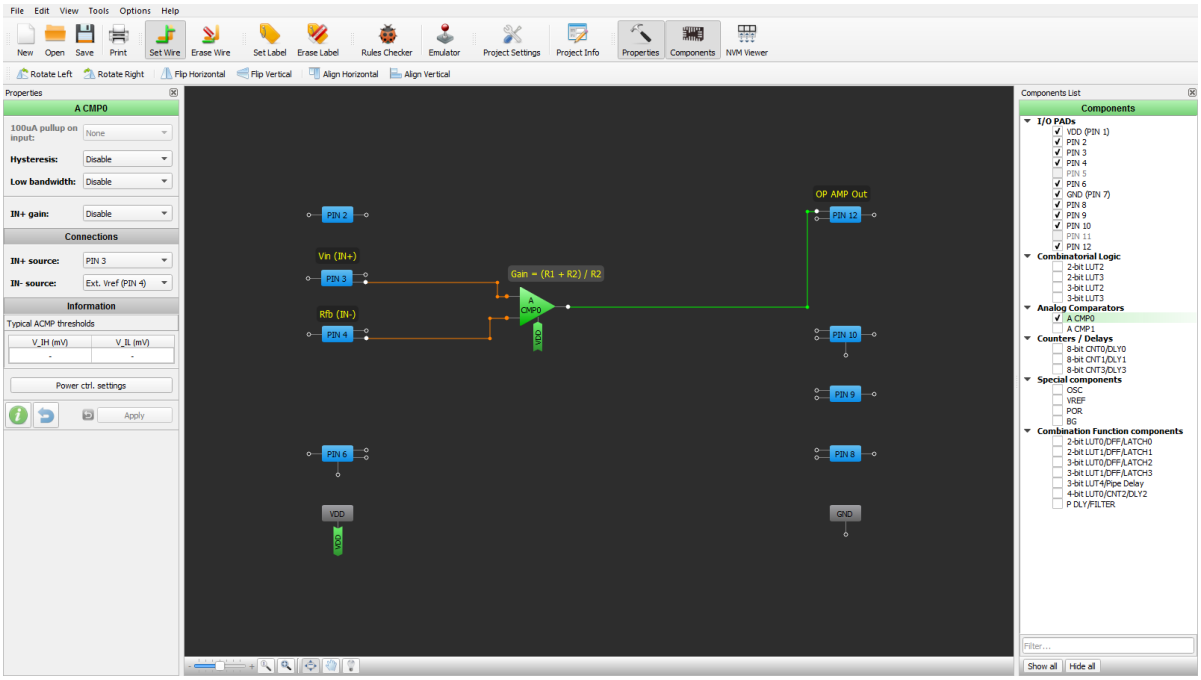

Figure 8: ACMP0 Settings in GreenPAK Design

Based on the analysis given, the circuit operates quite well and as expected. The gain is very linear and accurate for $V_{OUT} < V_{DD}$ - 300 mV and $V_{IN} < 1.1$ V. For many slow varying DC signals this performance is more than acceptable for adding some needed gain and enables the designer to now measure and compare these signal values more accurately and easily without adding additional external OpAmps.

Revision History

Revision	Date	Description
1.0	28-Feb-2018	Initial version.

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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