Application Note

Using Dialog's Integrated Power Switches in Super Capacitor Applications

AN-CM-246

Abstract

This application note describes some common problems caused by powering up on high capacitive loads. Using Dialog Integrated Power Switches it is easy to power up from very small capacitance to relatively high value super capacitors.

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1 Terms and Definitions

ACL	Active Current Limit
IC	Integrated Circuit
IPS	Integrated Power Switch
PCB	Printed Circuit Board

2 References

[1] SLG59M1717V, Datasheet, Dialog Semiconductor.

[2] AN-1068, GFET3 and HFET1 Integrated Power Switch Basics, Application Note, Dialog Semiconductor.

3 Introduction

Capacitance is the ability of a system to store an electric charge (Figure 1). Capacitance value is the ratio of the charge accumulated on conductive plates to the applied voltage:

$$C = \frac{Q}{V}$$

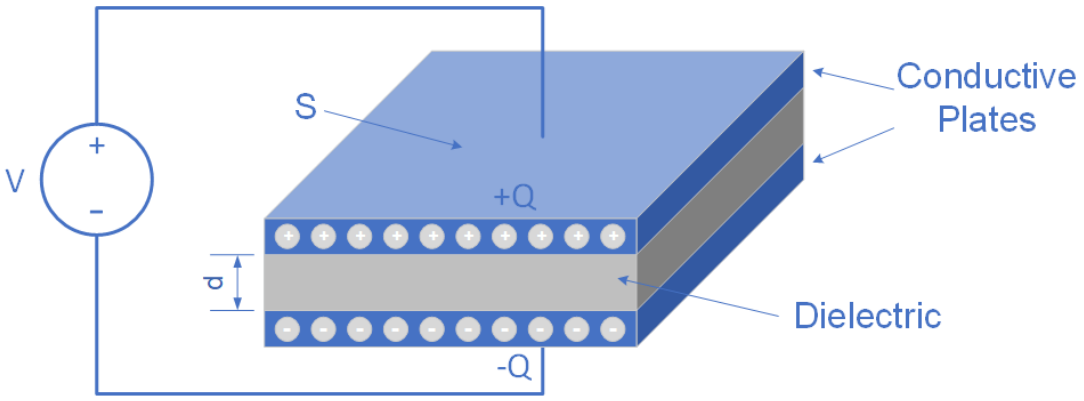

Figure 1: Two Charged Conductive Plates Separated with Dielectric Layer

The capacitance of a parallel plate system is proportional to the plate area *S* and inversely proportional to the distance *d* between these two conductive plates.

$$C = \frac{\varepsilon S}{d} \quad (1)$$

where

ε - an absolute permittivity of the dielectric material;

S - a square of conductive plate;

d - a distance between two conductive plates.

A component designed to store electric charge is called capacitor. In electronic circuits, capacitors can be used in a variety of different ways: coupling and decoupling effects, smoothing output signal of rectifiers, as a timing element, etc.

A capacitor which can store a great amount of charge is called a supercapacitor or ultracapacitor. Supercapacitor's electrodes are made of the materials that have a high surface area. This allows to hold much more charge without increasing capacitor's size.

Supercapacitors have an electrolyte inside and when the electrodes are charged, the electrolyte polarizes according to the charge of the electrodes (Figure 2). This charge separation creates two oppositely charged layers. Such system behaves like two conventional capacitors attached in series. These capacitors have plate separation distances that are a few nanometers thick.

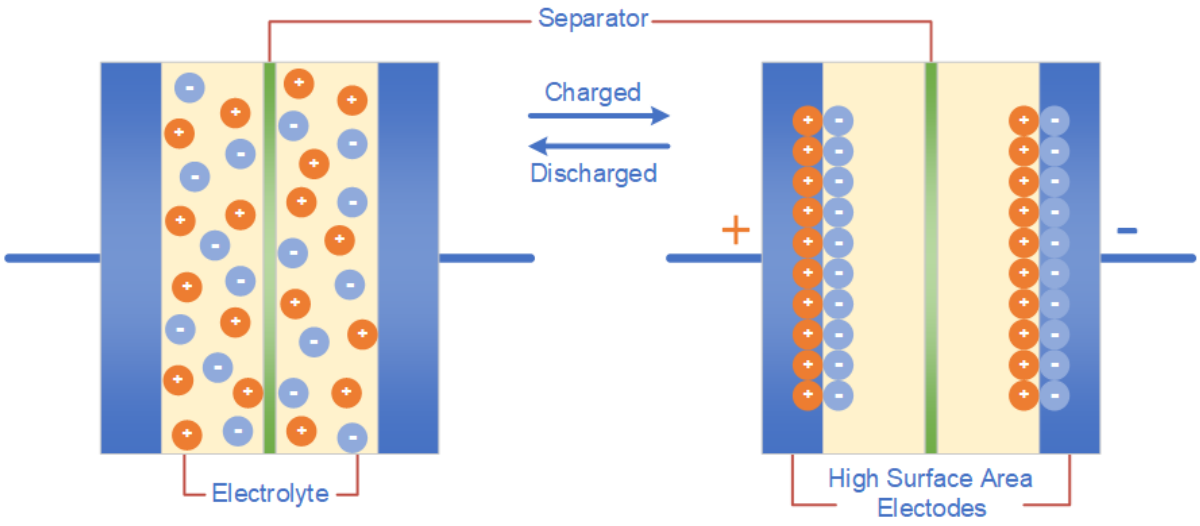

Figure 2: A Supercapacitor Structure and Charge Distribution

The combination of the increased surface area and the small plate separation distance increases the capacitance and the energy stored in the supercapacitor.

4 Design Description

In this application note, we will describe how to apply Dialog's nFET SLG59M1717V IPS to power up into super-capacitor or very high capacitive loads. To implement a very large capacitive load, (3) 5 V, 0.22 F supercapacitors were connected in parallel. The SLG59M1717V is a high-performance, 4 mΩ, 5 A single-channel, feature-rich nFET IPS designed for all 0.8 V to 5.5 V power rail applications. In addition to its world-class RDS_{ON}, the SLG59M1717V incorporates two-stage overcurrent protection: (1) resistor-adjustable Active Current Limit and (2) a fixed 1.6 A Short-circuit Current Limit.

A typical connection of Dialog's SLG59M1717V in capacitive/resistive load applications is illustrated in Figure 3.

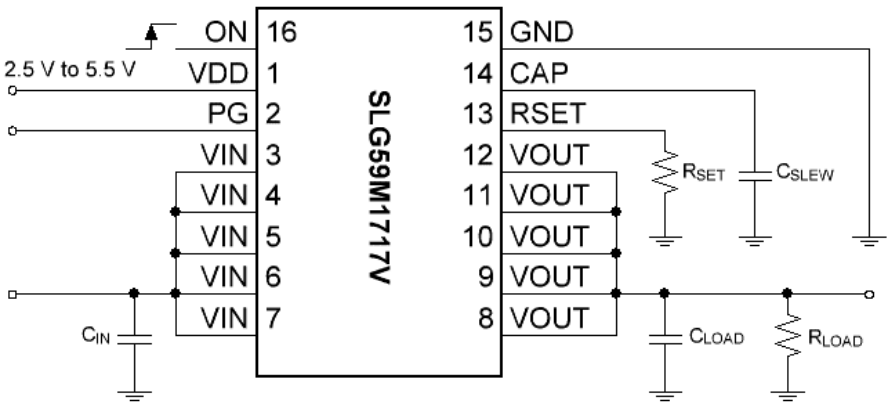

Figure 3: Typical Application Diagram of SLG59M1717V

5 Start-up Inrush Current Considerations

When a voltage is applied to a discharged (or an uncharged) capacitor, a large initial current may flow through an IPS. This current is called inrush current and can be calculated by equation below:

Inrush Current, $I = C\frac{dV}{dt}$

where

C - is the total load capacitance;

$\frac{dV}{dt}$ - the IPS's V_{OUT} slew rate during voltage ramp up.

To reduce inrush current for a given load capacitance, it is necessary to decrease the IPS's V_{OUT} slew rate. An equivalent circuit of the SLG59M1717V's slew rate control loop with capacitors at its VIN and VOUT pins is shown in Figure 4:

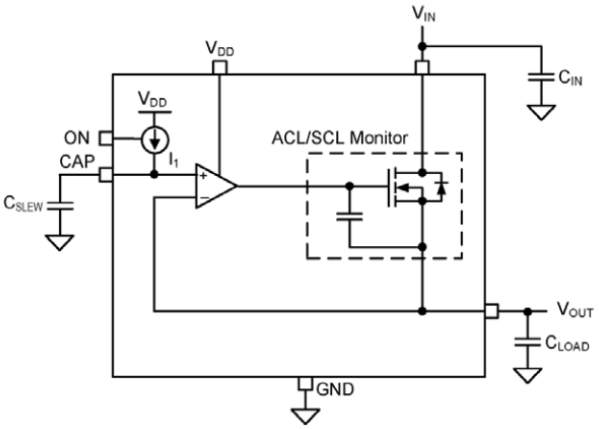

Figure 4: SLG59M1717V's Equivalent Slew-rate Control Loop Circuit

For a desired V_{OUT} slew rate ($V_{OUT(SR)}$), a corresponding C_{SLEW} value is selected. At the VOUT pin and with ON = LOW, the internal FET is OFF, V_{OUT} is initially at 0 V, and there is no stored charge on C_{LOAD}. When a low-to-high transition is applied to the IC's ON pin, an internal current source (I_1) is enabled which, in turn, charges the external slew rate capacitor, C_{SLEW}. The SLG59M1717V's internal micropower op amp sets the circuit's $V_{OUT(SR)}$ based on the slew rate of the nodal voltage at its non-inverting pin (the voltage at the CAP pin).

6 Capacitive Load Operation

In Figure 5, a typical SLG59M1717's power up behavior for resistive and capacitive load is illustrated. As can be observed, output voltage and current through the IPS are changing linearly.

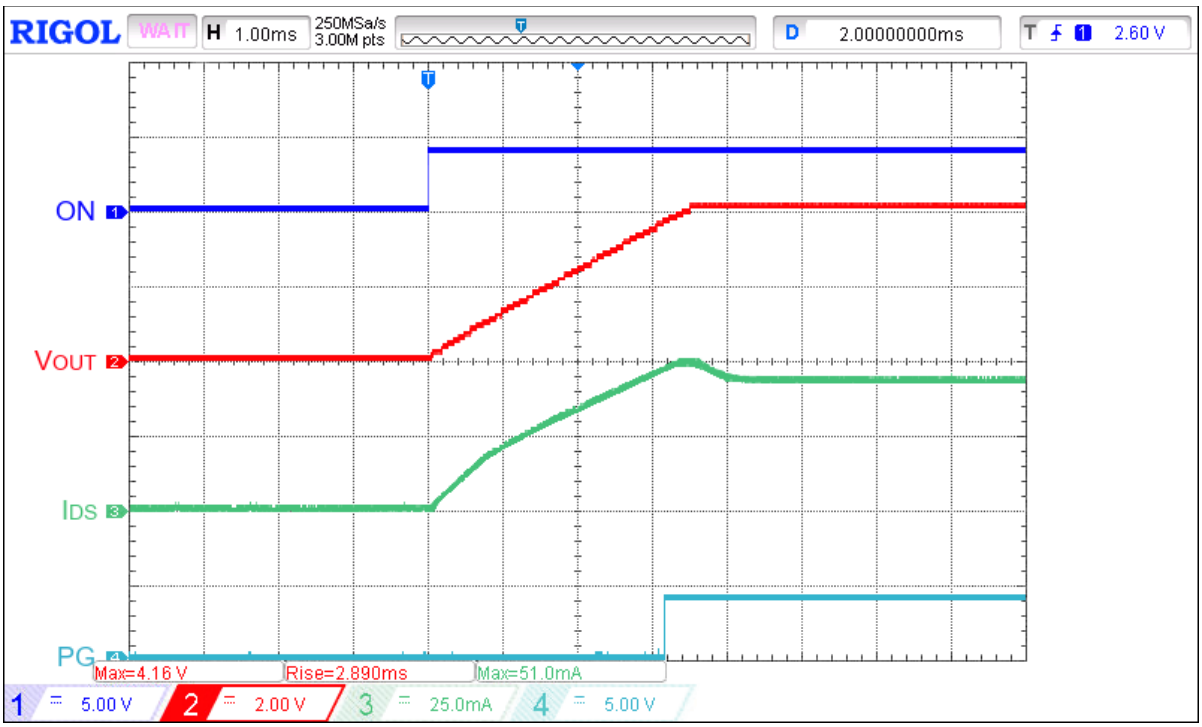

Figure 5: Typical Power up Operation Waveform for V_{DD} = V_{IN} = 4 V, R_{SET} = 40 kΩ, C_{SLEW} = 10 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 10 µF

In this example, a 10 nF C_{SLEW} capacitor sets the slew rate to approximately 1.1 V/ms, thus inrush current is only 11 mA. In using a 0.66F supercapacitor, the resultant inrush current is dramatically increased and a non-linear ramp is observed during power up (see Figure 6). Since the inrush current is higher than the IPS's I_{ACL} threshold (set by external R_{SET} resistor), the IPS's internal overcurrent protection is activated. To keep the load capacitor's charging current from exceeding the IPS's I_{ACL} threshold, the ACL monitor increases the FET resistance. However, if the overload condition persists where the die temperature rises because of the increased FET resistance, the IPS's internal Thermal Shutdown Protection circuit will be activated. If the die temperature exceeds 150 °C the IPS's internal Thermal Shutdown Protection circuit shuts the FET completely OFF, thereby allowing the die to cool. When the die cools to the IPS's lower 130 °C temperature threshold, the FET is automatically turned back on. This process may repeat as long as the output current overload condition persists.

According to the above, charging supercapacitors with high currents leads to continuously switching ON/OFF IPS and a "saw" appears on the V_{OUT} (see Figure 6). To charge up such a large load capacitor, a 2 µF capacitor was chosen for C_{SLEW}. It sets the slew rate to 5.75 V/s and thus limits the inrush current to 3.8 A (see Figure 7).

Even if C_{SLEW} is chosen and protection circuits are not triggered during power up, we recommend to check package-case temperature as well. If during power up, the package case temperature rises higher than 20 °C to 30 °C, we recommend increasing C_{SLEW} value until case temperature rise is less than 30°C (or lower), otherwise frequent overheating cycles may impact the IPS's long-term reliability.

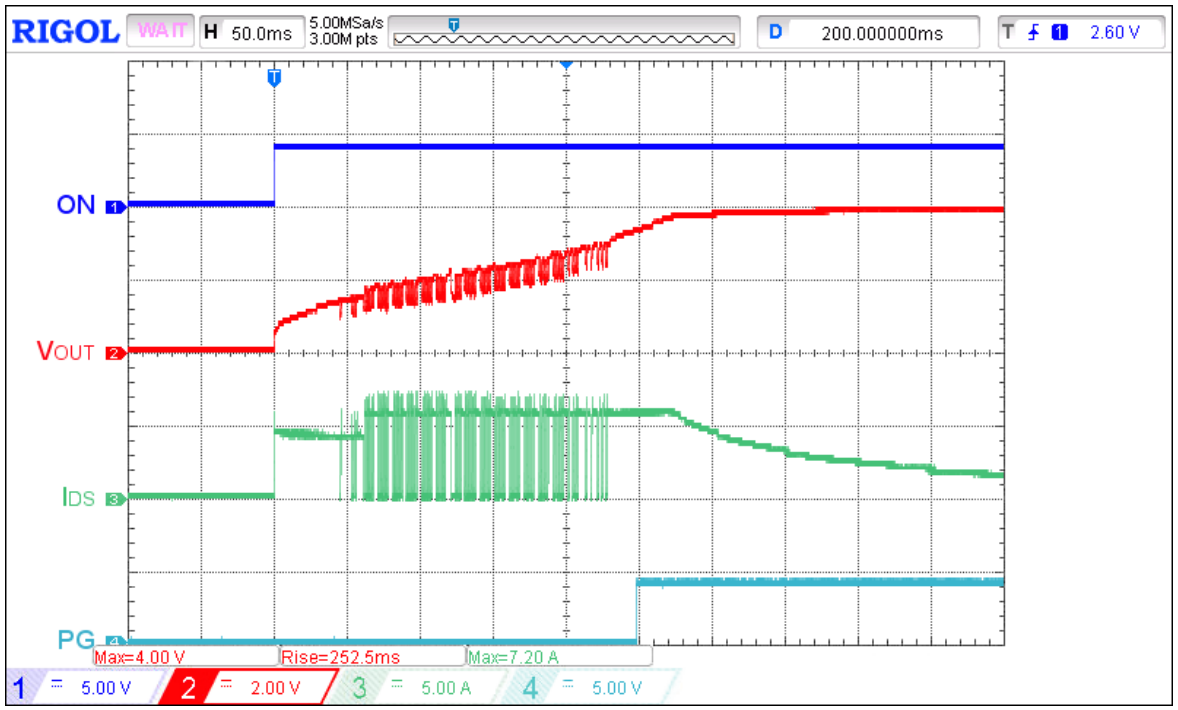

Figure 6: Active Current Limit and Thermal Protection Operation During Power Up on High Capacitive Load Caused by Improper IPS Slew Rate Settings for V_{DD} = V_{IN} = 4 V, I_{ACL} = 5.7 A, R_{SET} = 40 kΩ, C_{SLEW} = 10 nF, C_{LOAD} = 0.66 F, R_{LOAD} = 100 Ω

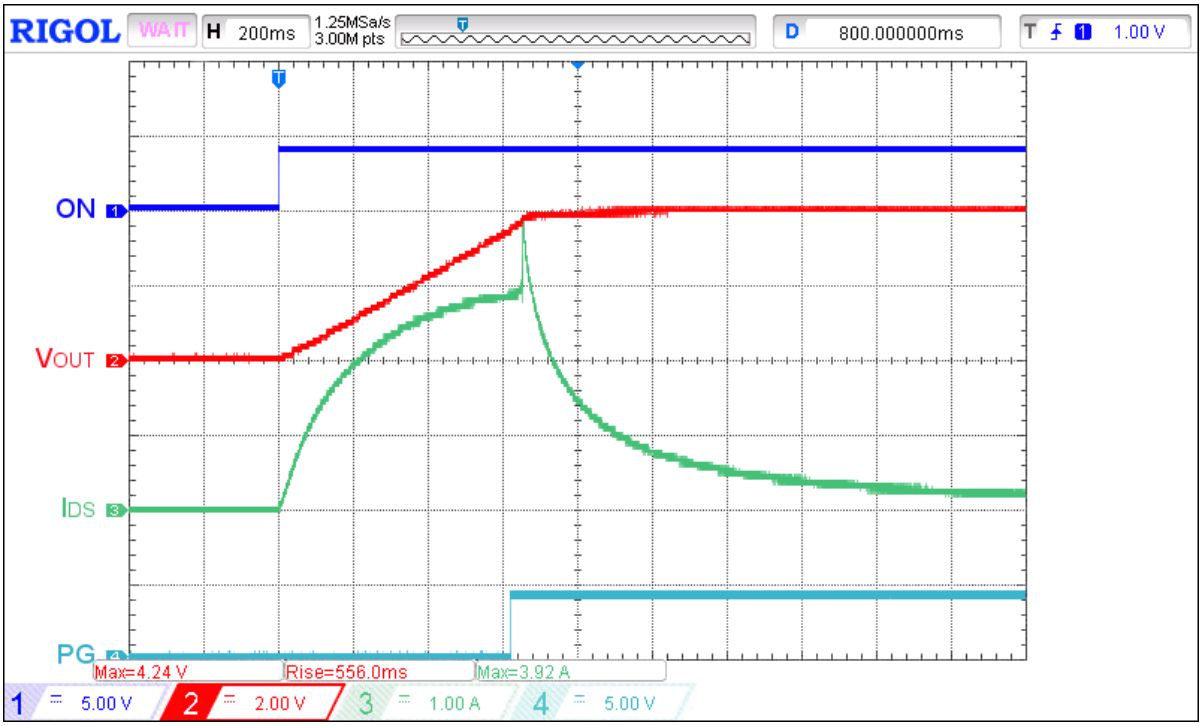

Figure 7: Typical Power Up for High Capacitive Load with Proper IPS Slew Rate Settings for $V_{DD} = V_{IN} = 4$ V, $I_{ACL} = 5.7$ A, $R_{SET} = 40$ kΩ, $C_{SLEW} = 2$ µF, $C_{LOAD} = 0.66$ F, $R_{LOAD} = 100$ Ω

7 Conclusion

Charging high capacitive loads without any control may cause large inrush currents which can severely damage an IPS as well as any circuits downstream of the IPS. In addition, the charging of large capacitive loads may cause frequent over-heating cycles that can affect any IPS's long-term reliability. To solve this problem, Dialog Semiconductor offers a wide range of high-performance nFET integrated power switches with at least one or more protection features like adjustable inrush current control, active current limit, thermal shutdown protection. For more information on Dialog's family of integrated power switches with advanced features, please, visit www.dialog-semiconductor.com

Revision History

Revision	Date	Description
1.0	03-Jul-2018	Initial Version

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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