Application Note

Programmable Limits PWM

AN-CM-265

Abstract

This application note describes how to design PWM with programmable limits using Dialog's GreenPAK IC.
This application note comes complete with design files which can be found in the References section.

Contents

Figures

1 Terms and Definitions

CNT	Counter
DFF	D flip-flop
DLY	Delay
I2C	Serial communication
LUT	Lookup table
OSC	Oscillator
PWM	Pulse width modulation

2 References

For related documents and software, please visit:

https://www.dialog-semiconductor.com/configurable-mixed-signal.

Download our free GreenPAK™ Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Dialog Semiconductor provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Dialog IC.

[1] GreenPAK Designer Software, Software Download and User Guide, Dialog Semiconductor

[2] AN-CM-265 Programmable Limits PWM.gp, GreenPAK Design File, Dialog Semiconductor

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Dialog Semiconductor

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Dialog Semiconductor

3 Introduction

This application note describes three PWM design variants using Dialog Semiconductor's GreenPAK CMIC:

1. "0-100% PWM" is PWM signal generator with the possibility to control the signal's duty cycle from 0 to 100% full range, controlled by external or internal signal (for instance: signal from external pin, I2C signal, from a comparator, etc.).
2. "Programmable Limits PWM" is modification of "0-100% PWM" with settable maximum and minimum limits of the PWM's duty cycle. The limits can be changed by I2C.
3. "Sawtooth modulated" is a PWM generator with settable maximum and minimum limits of PWM's duty cycle and generates a sawtooth PWM modulation.

4 How it works?

Let's start from a simplified design. The following design is just a PWM generator that controls the PWM duty cycle with UP and DOWN buttons.

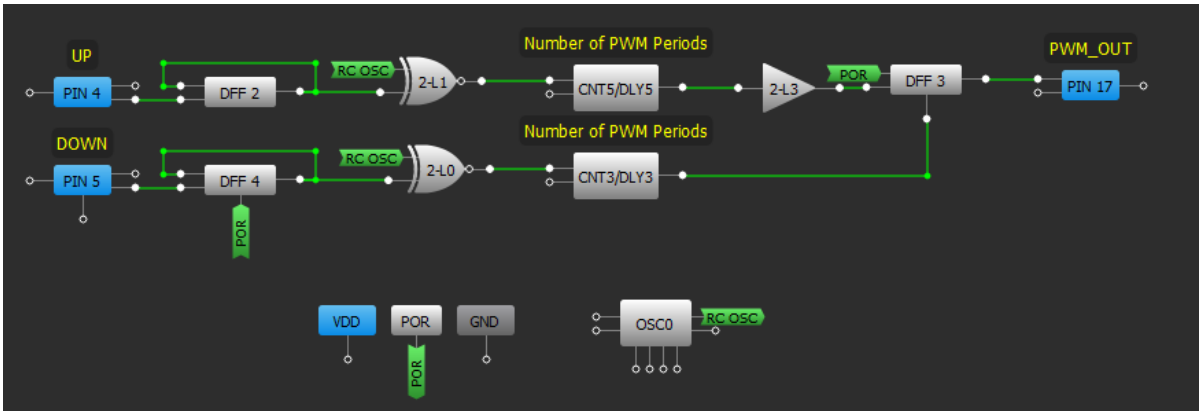


Figure 1: Simplified PWM Design

The PWM's duty cycle is determined by the shift between CNT3 and CNT5 output pulses. CNT3 counter data should equal CNT5 counter data. DFF3 is set by the rising edge of CNT5 pulse and reset by the low pulse of CNT3. CNT3 output is inverted, so active signal is LOW (see Figure 2).

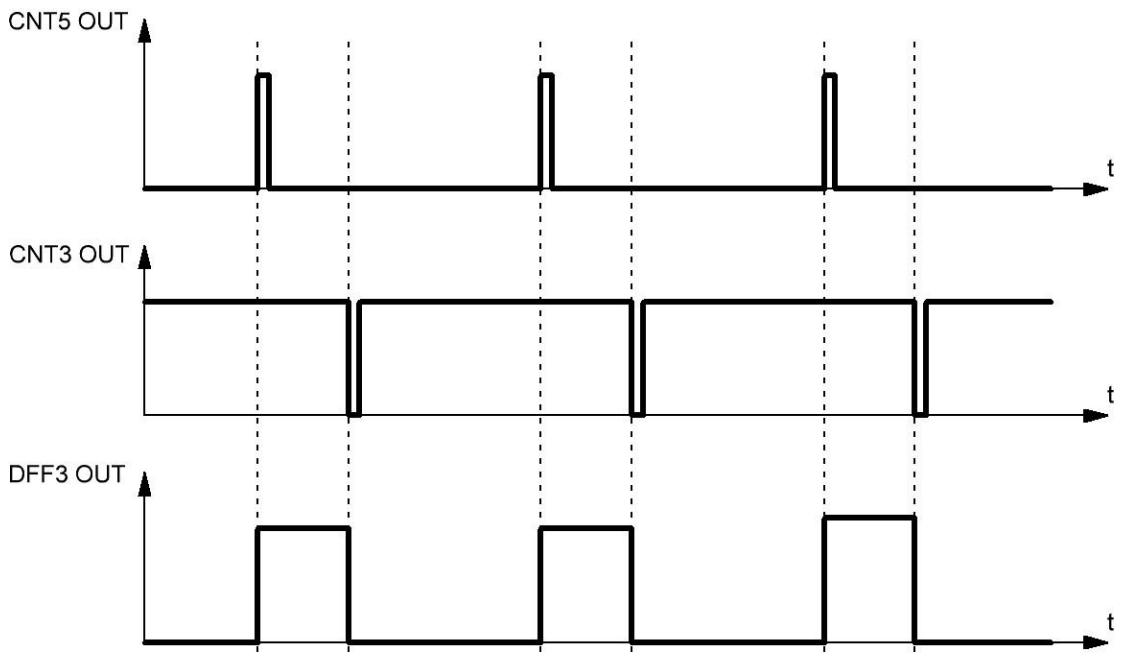


Figure 2: Constant PWM Based on Shift Between Two Clock Signals

To change the value of the PWM duty cycle we need to add one clock to CNT5 (to increase PWM duty cycle) or to CNT3 (to decrease PWM duty cycle). It can be done by external buttons to change the delay between the CNT3, CNT5 outputs. One clock makes 1 step shift (where 1 step shift = (1/(CNT5(or CNT3) counter data + 1)) * 100%). DFF2 and DFF4 are used to avoid an additional clock which can appear when a button generates a logic LOW.

Figure 3 shows the design where a PWM duty cycle changes linearly. Also, there is a possibility to control the rate of the duty cycle change and control the direction of this change.

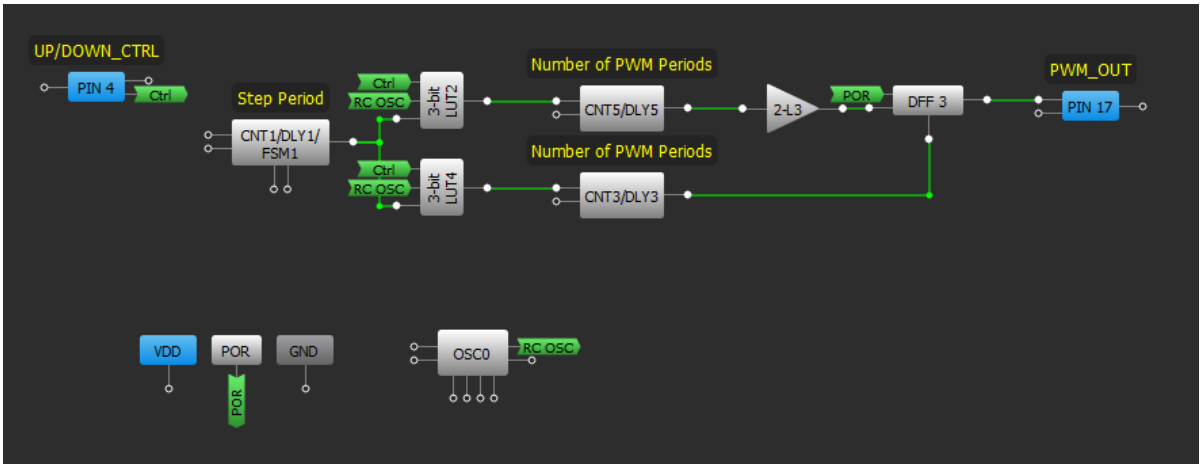
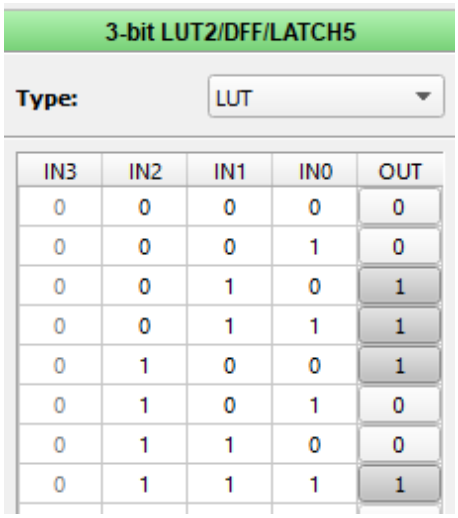


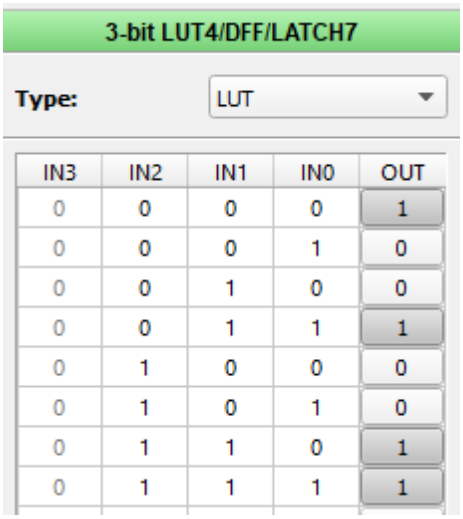
Figure 3: Linearly Changeable PWM

Here, CNT1 generates a clock signal. When “UP/DOWN_CTRL” pin is HIGH, the signal goes to CNT5 CLK input through 3-bit LUT2 (duty cycle increase). When “UP/DOWN_CTRL” pin is LOW, the signal goes to CNT3 CLK input through 3-bit LUT4 (duty cycle decrease).



IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1

Figure 4: Truth Table of 3-bit LUT2



IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1

Figure 5: Truth Table of 3-bit LUT4

2-L3 is just a buffer. This one is used to guarantee 0% duty cycle. In some cases, the design will work with 0% duty cycle without the 2-L3 buffer. However, if the propagation time of CNT5 is less than CNT3, it causes short pulses to appear at the output. So 2-L3 ensures a clean output when the duty cycle should be 0%.

The rate of change of PWM's duty cycle depends on the period of CNT1. PWM full ramp time from 0% to 100% duty cycle can be calculated using following formula:

T_PWM_RAMP = CNT5 Counter Data * CNT1 Period

5 "0-100% PWM"

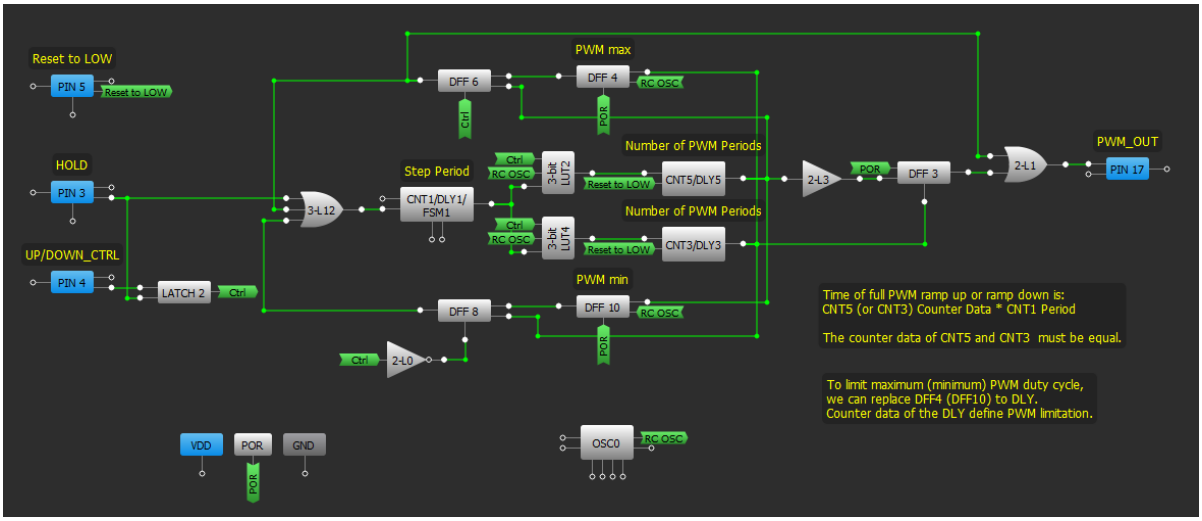


Figure 6: "0-100% PWM"

A part of the "0-100% PWM" design has been described above. This is a linearly changeable PWM, where the duty cycle is changed from 0 to 100%, controlled by an external signal. The rate of duty cycle change can be changed via I2C.

The button “HOLD” is for holding the duty cycle constant. This button just resets CNT1. CNT1 is reset by a HIGH level signal and keeps the output HIGH.

The button “Reset to LOW” is used to reset duty cycle to 0%.

DFF4 and DFF6 provide the upper limit of duty cycle to avoid overflow. These two DFFs measure the shift between two signals, the outputs of CNT3 and CNT5. When the shift is equal to 1.5 clock period of OSC0, these DFFs detect it and reset CNT1. Thus, the duty cycle doesn't change while UP/DOWN_CTRL signal stays HIGH. When CNT1 is reset, its output goes HIGH, generating one more clock signal and RC OSC signal isn’t inverted anymore by 3-bit LUT2. You can see it in Figure 7 and Figure 8. When the shift becomes 1.5 clock period, Maximum duty cycle at output of DFF3 is:

max. Duty cycle = CNT5 counter data/(CNT5 counter data+1).

In our case:

255/256 = 99.6%

Channel 1 (yellow/top line) – DFF3 OUT

D0 – CNT5 OUT

D1 – CNT3 OUT

D2 – CNT1 OUT

D3 – 3-bit LUT2 OUT

D4 – 3-bit LUT4 OUT

D5 – DFF4 OUT

D6 – DFF8 OUT

Figure 7: Duty Cycle Becoming Maximum

Figure 8: A Signal After Duty Cycle Has Become Maximum

DFF8 and DFF10 provide the lower limit of duty cycle to avoid overflow. These two DFFs measure a shift between two signals, CNT3 and CNT5. When the shift is equal to a half clock period of OSC0 these DFFs detect it and reset CNT1. Thus, the duty cycle doesn't change while UP/DOWN_CTRL signal stays LOW. When CNT1 is reset its output goes HIGH, generating one more clock signal and RC OSC signal isn't inverted anymore by 3-bit LUT4. You can see it in Figure 9, Figure 10, Figure 11. Minimum duty cycle is:

min. Duty cycle = 0%.

Channel 1 (yellow/top line) – DFF3 OUT

D0 – CNT5 OUT

D1 – CNT3 OUT

D2 – CNT1 OUT

D3 – 3-bit LUT2 OUT

D4 – 3-bit LUT4 OUT

D5 – DFF4 OUT

D6 – DFF8 OUT

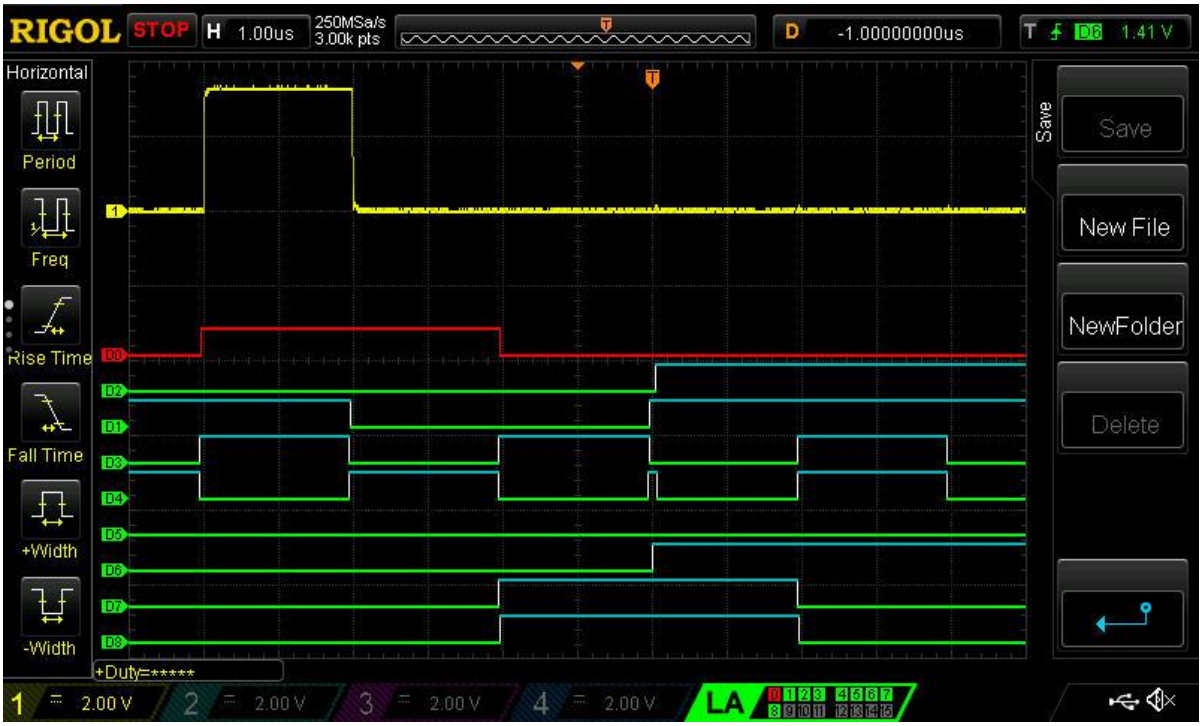


Figure 9: Duty Cycle Becoming Minimum

Figure 10: Zoomed Figure 9

Figure 11: Zoomed Figure 9

2-L1 and LATCH 2 are used to create a 100% duty cycle. When the signal is at maximum duty cycle the output of the DFF6 goes HIGH and the output of 2-L1 goes HIGH as well. So, the duty cycle of the design can change from 0% to 100% duty cycle.

6 "Programmable Limits PWM"

To control the maximum and minimum limits of PWM, DFF4 and DFF10 of the "0-100% PWM" design should be replaced with delay blocks (DLY4 and DLY6).

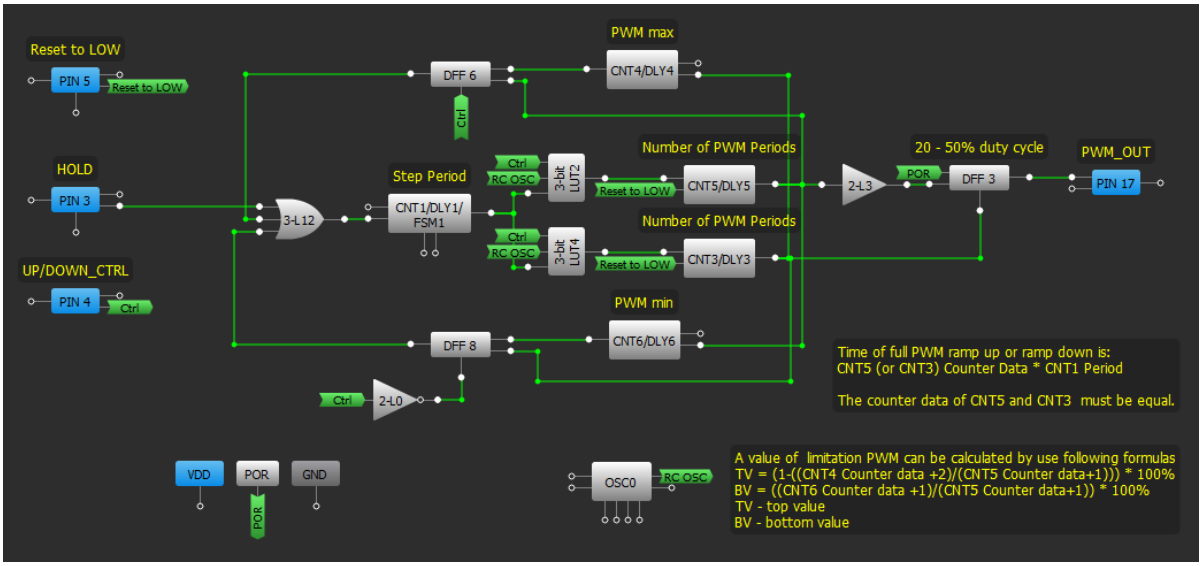


Figure 12: "Programmable Limits PWM"

Programmable Limits PWM

Figure 12 shows the design with the feature of programmable limits of PWM duty cycle. To change the limits of duty cycle you can change DLY4 counter data (for upper limit value of the duty cycle) and DLY6 counter data (for lower limit value of the duty cycle) via I2C. The upper and lower limits of duty cycle can be calculated using the following formulas:

Upper limit = (1-((DLY4 Counter Data +2)/(CNT5 Counter data+1))) * 100%

Lower limit = ((DLY6 Counter Data +1)/(CNT5 Counter data+1)) * 100%

The “Programmable Limits PWM” design file PWM example is set to 20% to 50% duty cycle range.

The minimum possible duty cycle of this design is 0.78% and the maximum possible duty cycle is 98.82%.

Channel 1 (yellow/top line) – PIN#17 (PWM_OUT)

Channel 2 (light blue/2nd line) – PIN#5 (Reset to LOW)

Channel 3 (magenta /3rd line) – PIN#3 (HOLD)

Channel 4 (blue/bottom line) – PIN#4 (UP/DOWN_CTRL)

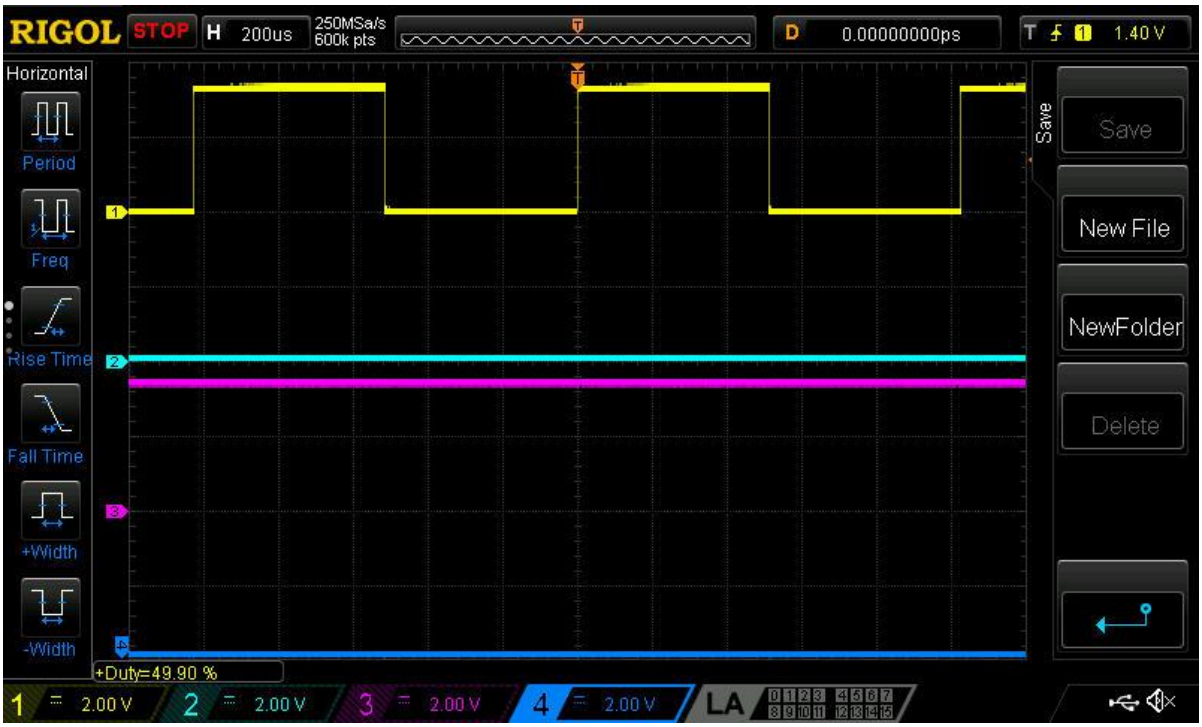


Figure 13: Maximum Limit of PWM Duty Cycle

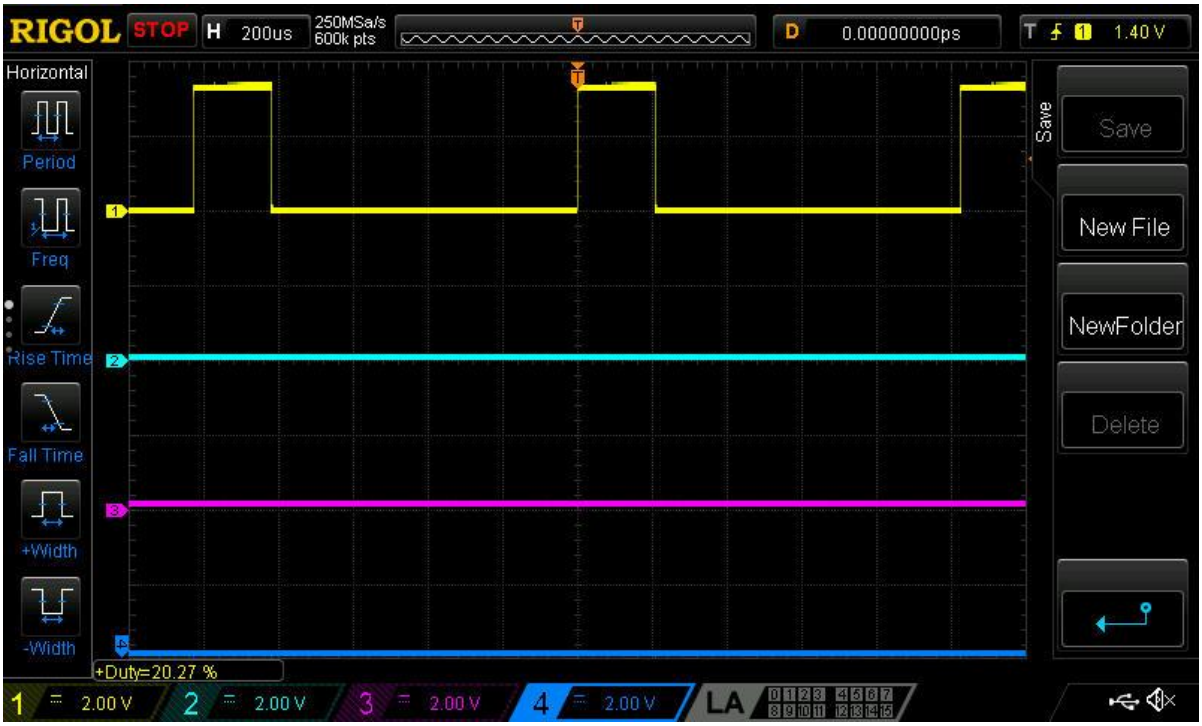


Figure 14: Minimum Limit of PWM Duty Cycle

Therefore, this design can be used as a PWM generator with the possibility to define limits of PWM duty cycle, rate of PWM duty cycle change, and its direction. It can all be done via I2C interface as well. Also, there is the possibility to change the PWM frequency in all designs presented in this application note.

7 “Triangle Modulation”

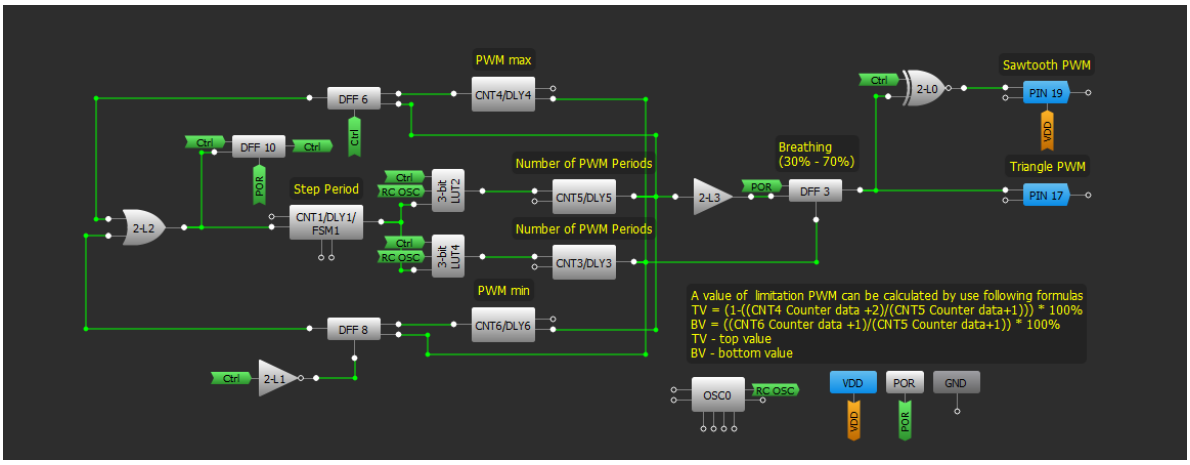


Figure 15: “Triangle Modulation” Design

The “Triangle Modulation” is a design which generates PWM signal with duty cycle changed according to the triangle principle, and with configurable limits of duty cycle (for instance 23-87%, 75-90%, in our case it is 30-70%). Also, the rate of the modulation can be controlled via I2C, same as in the previous designs.

DFF10 is used to change a direction of the duty cycle's change.

There is a possibility to get PWM signal with duty cycle changed according to the sawtooth principle. For this we should set the top limit value and the bottom limit value to be symmetrical to a 50% duty cycle (for example: 20-80%, 35-65%), thus we get a sawtooth PWM at the output of 2-L0 in the set range.

Also, there is a possibility to add a "HOLD" button and "Reset" button to the design.

All other functionality of the design is the same as in the previous design.

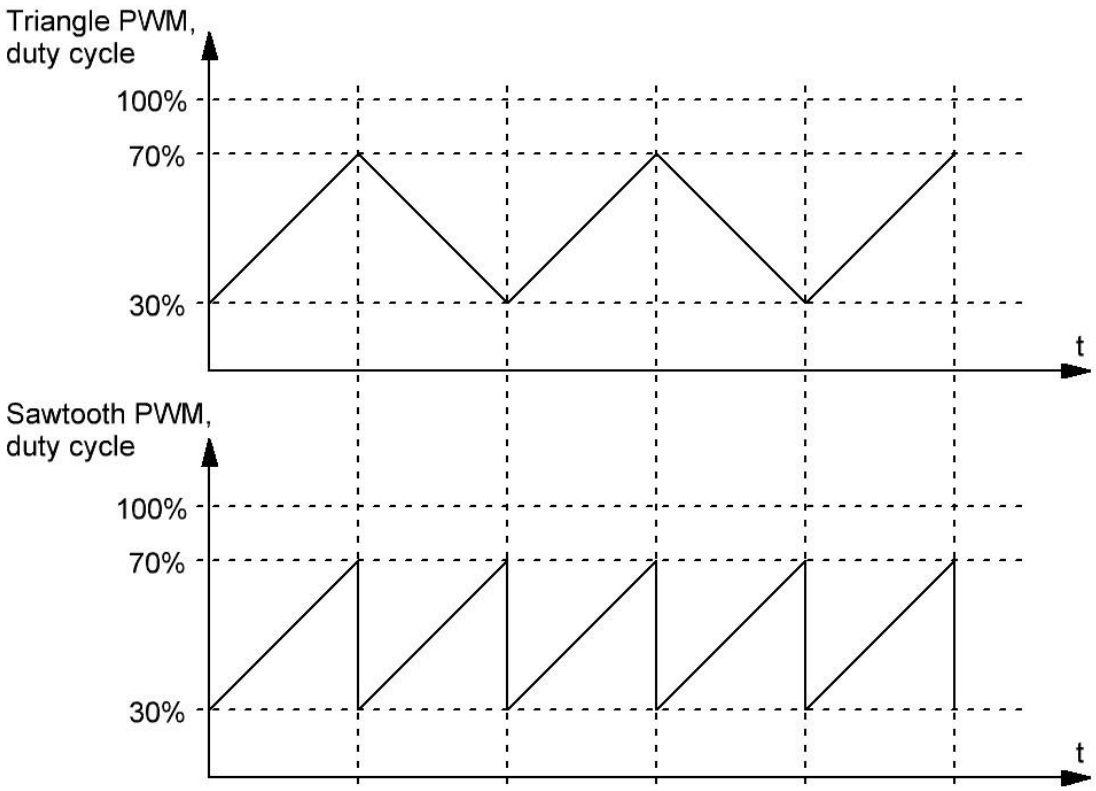


Figure 16: Triangle and Sawtooth Modulation PWM Duty Cycle Principle

8 Conclusions

PWM is commonly used in many electronic devices. The main advantage of PWM is high efficiency, through very low power loss in switching devices. When a switch is off there is practically no current, and when it is on and power is being transferred to the load, there is little voltage drop across a properly selected switch. Power loss, being the product of voltage and current, is close to minimized in both cases.

These designs can be used to control the power supply of electronic devices, especially for inertial loads such as motors, keeping constant rotation speed of brushed motors, solar buttery chargers, driving LEDs, and many other uses.

Revision History

Revision	Date	Description
1.0	13-Dec-2018	Initial Version

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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