

Application Note

PWM Frequency Converter

AN-CM-271

Abstract

This application note describes how to shift the frequency of a PWM signal without changing the duty cycle. A complete design file is included in the References section.

PWM Frequency Converter

Contents

Abstract	1
Contents	2
Figures	2
1 Terms and Definitions	3
2 References	3
3 Introduction	4
4 How it works?	4
5 Conclusions	8
Revision History	9

Figures

Figure 1: PWM Frequency Converter.....	4
Figure 2: Shifting Input Frequency from 100 Hz to 300 Hz.....	5
Figure 3: Shifting Input Frequency from 100 Hz to 25 Hz.....	6
Figure 4: Shifting Input Frequency from 100 Hz to 7.81 kHz.....	6
Figure 5: Zoomed Figure 4.....	7
Figure 6: Shifting Input Frequency from 1 kHz to 4 kHz	7

PWM Frequency Converter

1 Terms and Definitions

PWM	Pulse width modulation
SPI	Serial peripheral interface
FSM	Finite state machine
CNT	Counter
OSC	Oscillator
DCMP	Digital comparator

2 References

For related documents and software, please visit:

<https://www.dialog-semiconductor.com/configurable-mixed-signal>.

Download our free **GreenPAK™** Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the **GreenPAK** development tools [3] to freeze the design into your own customized IC in a matter of minutes. Dialog Semiconductor provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Dialog IC.

- [1] [GreenPAK Designer Software](#), Software Download and User Guide, Dialog Semiconductor
- [2] [AN-CM-271 PWM Frequency Converter.gp](#), [GreenPAK Design File](#), Dialog Semiconductor
- [3] [GreenPAK Development Tools](#), [GreenPAK Development Tools Webpage](#), Dialog Semiconductor
- [4] [GreenPAK Application Notes](#), [GreenPAK Application Notes Webpage](#), Dialog Semiconductor

PWM Frequency Converter

3 Introduction

The following design can convert a PWM signal from one known constant frequency to another constant frequency while retaining the duty cycle. This can be useful in cases where we want transmit the information contained in the duty cycle of a signal, over a carrier of different frequency. An example application is PWM control to analog output by means of RC filter - a low frequency PWM need a very large RC filter, but by converting the PWM to a higher frequency, a smaller RC filter can be used, along with advantages of smaller ripple and faster response.

4 How it works?

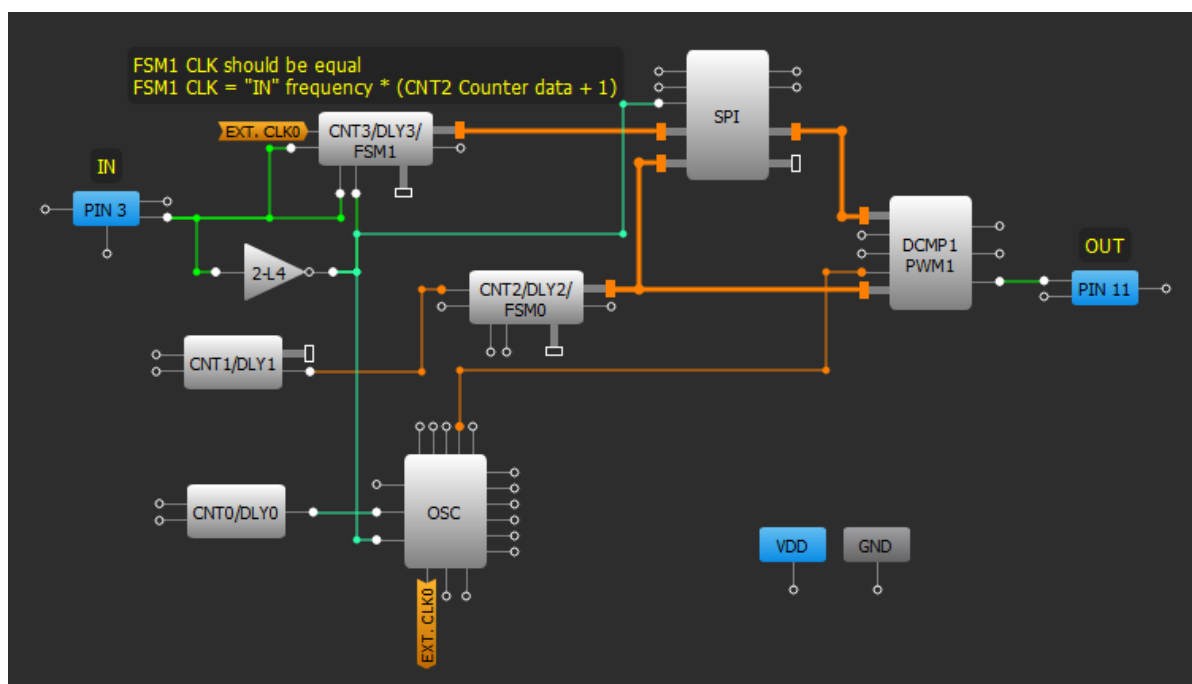


Figure 1: PWM Frequency Converter

Let's see how it works. When PIN#3 (signal input) goes HIGH, FSM1 is reset by the rising edge and starts to count UP, thus measuring the pulse width. Then, when PIN#3 goes LOW, FSM1 stops and the falling edge at PIN#3 through inverter 2-L4 writes FSM1 counter value into SPI buffer. This operation is repeated each period.

At the same time, CNT2 output sets the output frequency, i.e. the frequency at "OUT" is equal to output frequency of CNT2. The PWM of the output is generated as the counter value of CNT2 is constantly compared with SPI buffer's value by DCMP1. To change the "OUT" frequency, the setting of CNT2 as well as any element in the clock source chain (CNT1, osc divider, type) can be changed. The clock source can also be taken directly from OSC or external oscillator if desired.

The input frequency of FSM1 (FSM1 CLK) should be selected using following formula:

$$\text{FSM1 CLK} = \text{"IN" frequency} \times (\text{CNT2 Counter data} + 1)$$

"IN" frequency – frequency at PIN#3

If CNT0 counter data is 255, the formula can be written as:

$$\text{FSM1 CLK} = 256 \times \text{"IN" frequency}$$

PWM Frequency Converter

To change the FSM1 CLK, CNT0 counter data can be changed, oscillator divider can be changed, type of OSC can be changed, also CNT2 counter data can be changed.

Below are shown several scope shots of the design's functionality.

Channel 1 (yellow/top line) – PIN#3 (IN)

Channel 2 (light blue/2nd line) – PIN#11 (OUT)

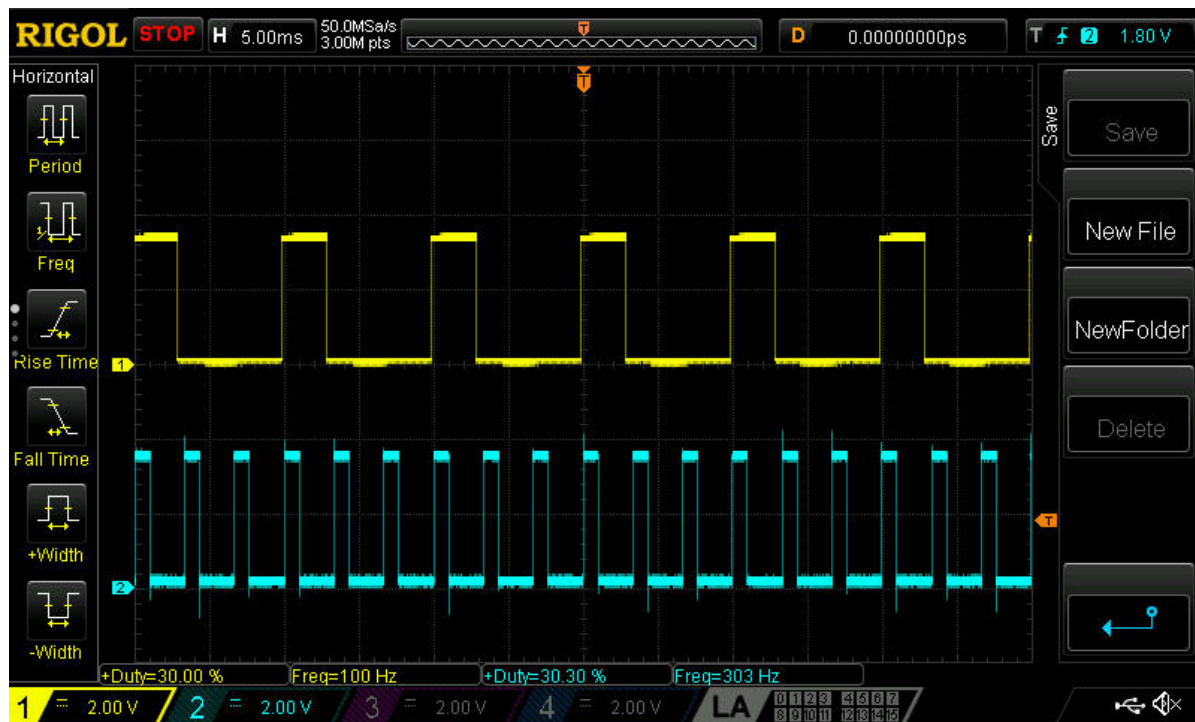


Figure 2: Shifting Input Frequency from 100 Hz to 300 Hz

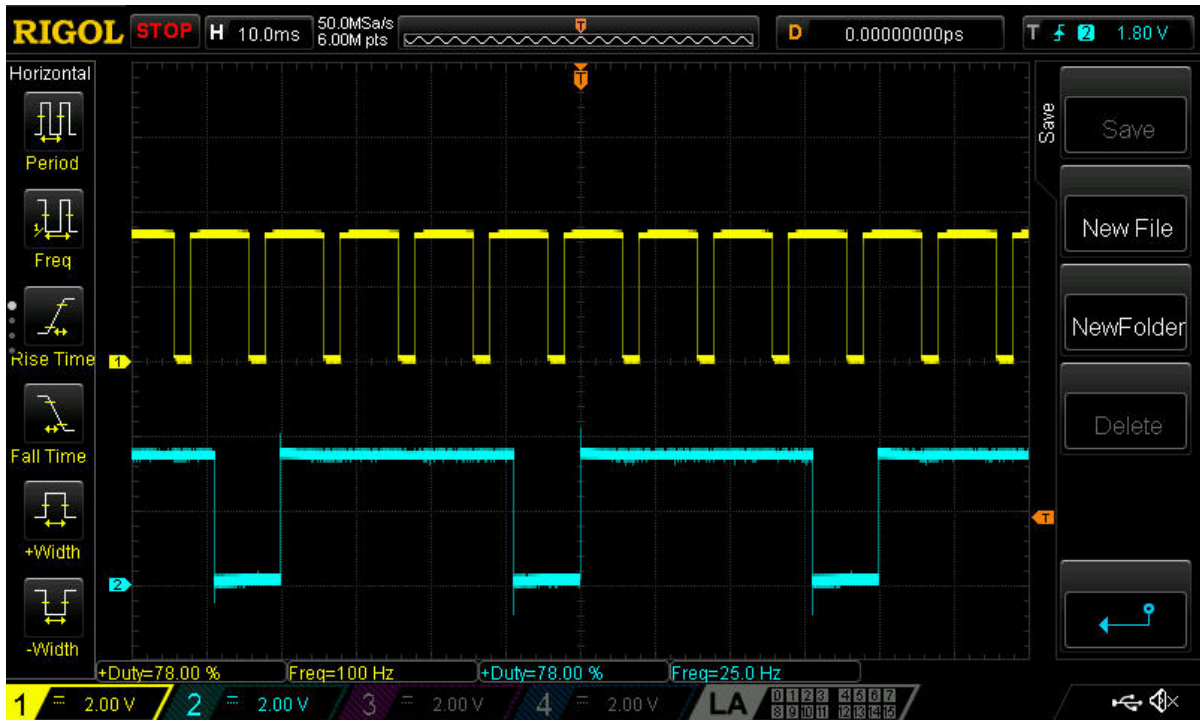


Figure 3: Shifting Input Frequency from 100 Hz to 25 Hz

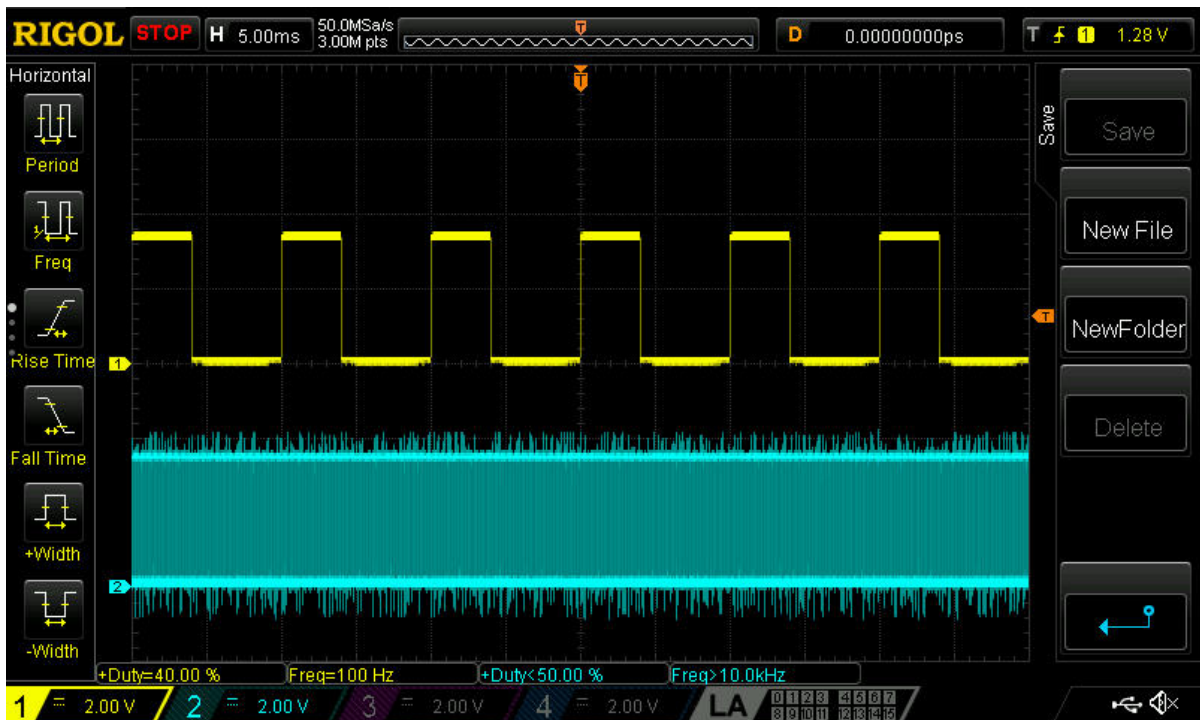


Figure 4: Shifting Input Frequency from 100 Hz to 7.81 kHz

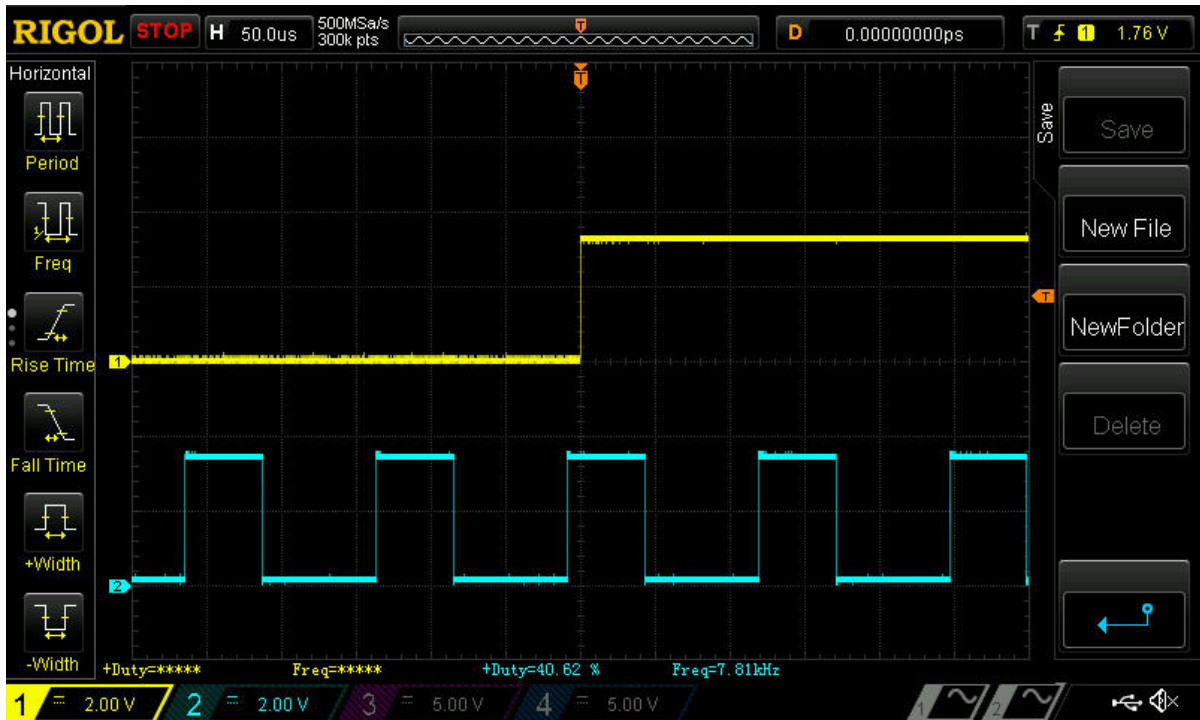


Figure 5: Zoomed Figure 4.

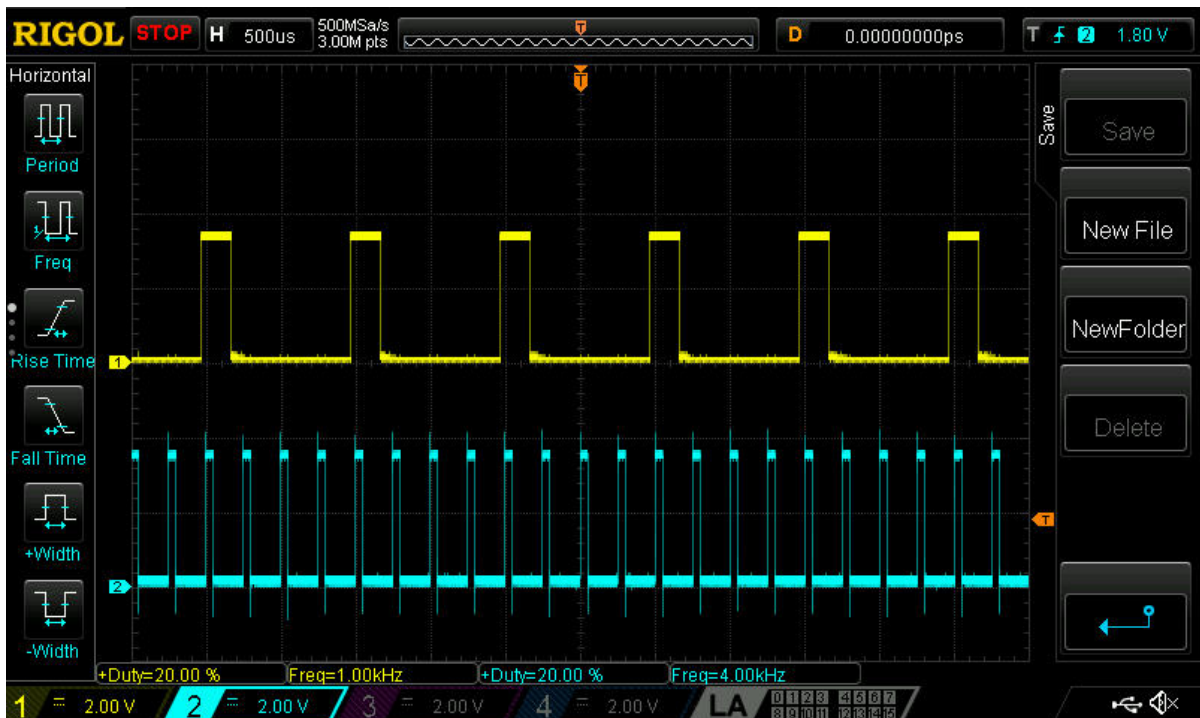


Figure 6: Shifting Input Frequency from 1 kHz to 4 kHz

5 Conclusions

This design can be used in many projects where there is a need to change a PWM constant input frequency without changing the duty cycle, for example LED backlight, motor controller, voltage regulator etc.

PWM Frequency Converter

Revision History

Revision	Date	Description
1.0	21-Jan-2019	Initial Version

PWM Frequency Converter

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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