

# **Application Note**

## Low-Power Button Replacement with Force-Sensitive Resistor

## **AN-CM-311**

### Abstract

This application describes how to create a highly reliable, low-power, temperature-stable button function using an SLG47004 and a force-sensitive resistor that can be used for sealed applications.

The application note comes complete with a design file which can be found in the Reference section.

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## Low-Power Button Replacement with Force-Sensitive Resistor

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### **1** Terms and Definitions

FSR Force-Sensitive Resistor

### 2 References

For related documents and software, please visit:

#### https://www.dialog-semiconductor.com/configurable-mixed-signal.

Download our free GreenPAK<sup>™</sup> Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Dialog Semiconductor provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Dialog IC.

- [1] GreenPAK Designer Software, Software Download and User Guide, Dialog Semiconductor
- [2] AN-CM-311 Low-Power Button Replacement with Force-Sensitive Resistor.gp, GreenPAK Design File, Dialog Semiconductor
- [3] GreenPAK Development Tools, GreenPAK Development Tools Webpage, Dialog Semiconductor
- [4] GreenPAK Application Notes, GreenPAK Application Notes Webpage, Dialog Semiconductor
- [5] SLG47004, Datasheet, Dialog Semiconductor
- [6] Interlink Electronics FSR 400 Series, Datasheet, Interlink Electronics.

Author: Matthew Leonard

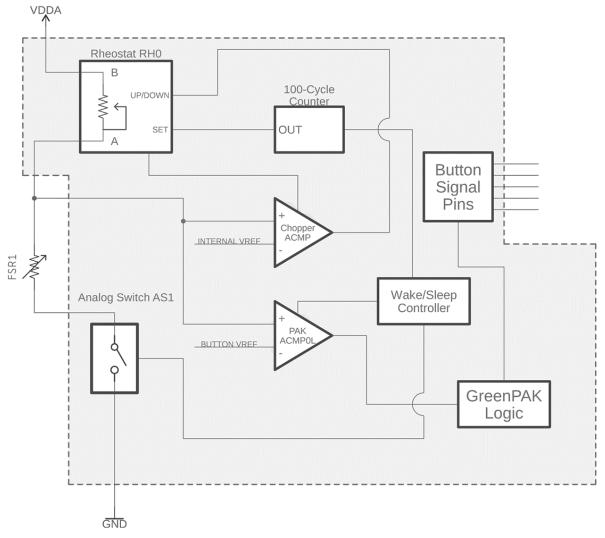
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### 3 Introduction

A common requirement for devices that must be sealed from environmental exposure is to replace all metal contact style push-buttons with functional replacements that do not have those weather-sealing difficulties. This application note describes one such way of creating a contact button replacement using a Force-Sensitive Resistor (FSR) in conjunction with an SLG47004V [5].

### 4 Schematic & Block Diagrams









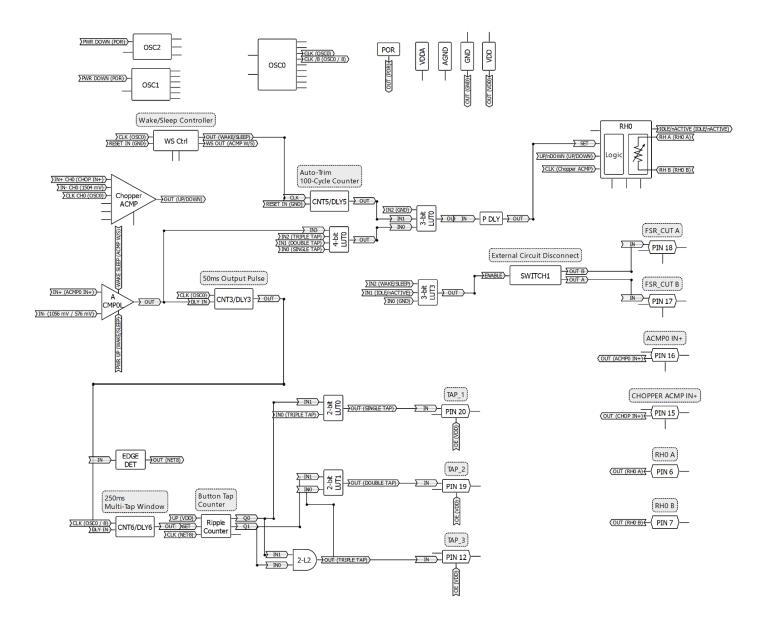
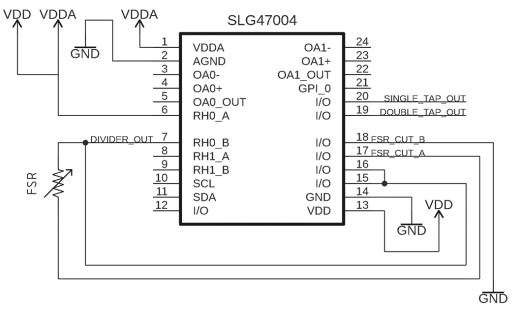


Figure 2: GreenPAK Designer Block Diagram

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VDD = 3.3V





### 5 Design Description

#### 5.1 Overview

The design highlighted above is intended for use as a functional replacement for a metal contact style push-button while featuring ultra-low power consumption. Using an external force-sensitive resistor in series with one of the SLG47004V's internal rheostat modules, a resistor divider network is created which is subsequently sampled by one of the SLG47004V's internal low-power ACMPs. This ACMP determines the state of the button based on the voltage present at the divider output. Once the internal low-power ACMP determines that the button has been pressed, internal GreenPAK logic processes the button press signal to determine whether a single, double, or triple-tap has occurred, and outputs these signals to dedicated pins.

Due to the fact that the force-sensitive resistor present in this design is highly susceptible to variation in resistance due to temperature changes, often as severe as +/-15% at extreme high/low temps, it is imperative that a constant "no-press" reference voltage is maintained throughout a wide range of temperatures. This constant reference voltage is achieved using the SLG47004V's auto-trim functionality, which periodically samples the divider output voltage and adjusts the SLG47004V's internal rheostat resistance, allowing the divider output to return to the specified "no-press" reference voltage. This auto-trim functionality not only allows for accurate operation over a wide range of temperatures, but it also allows the design to accommodate for sensor-to-sensor variations as well as variations in the overall system voltage level.

To attain ultra-low current consumption, the ACMP and external resistor divider network are controlled by the SLG47004V's wake/sleep controller. This wake/sleep controller keeps the ACMP in sleep mode via matrix signal, and the resistor divider circuit in an open state via one of the SLG47004V's internal analog switches, which is placed on the low side of the divider. The Chopper ACMP, which is responsible for the SLG47004V's auto-trim functionality, is also indirectly controlled by the wake/sleep controller using an intermediate counter that triggers an auto-trim cycle once every 100 normal wake/sleep cycles.

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#### Figure 4: A Standard FSR

#### 5.2 Mechanical Pre-Loading of the FSR Sensor (Required)

In order to properly trim the voltage divider circuit to the desired output voltage using the SLG47004V's digital rheostats, a small, consistent amount of force must be permanently applied to the FSR sensor before trimming can occur. This is due to the FSR's very high no-load resistance, which measured over 100 M $\Omega$  in this test and is shown by the graph below, being far too large for the SLG47004V's digital rheostats to compensate for. Pre-loading the FSR with a small mass will lower its base "un-pressed" resistance into a range that will allow the SLG47004V's digital rheostats to properly trim the voltage divider. It is worth noting that this process does not require a specific force value to be applied, so long as the force applied satisfies two requirements:

- 1. The applied force creates a large enough resistance drop within the FSR to allow for proper trimming of the voltage divider.
- 2. The applied force remains constant throughout the lifespan of the application.

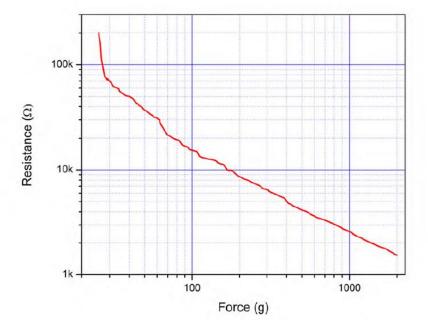


Figure 5: FSR Resistance vs Force Applied

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### 5.3 Auto-Trim Overview

In order to adequately implement an FSR sensor as a button replacement, considerations must be made for its rather large temperature dependency. Ideally, the no-press output voltage of the system would remain constant over temperature, allowing for a detecting ACMP to be tuned to detect button presses at all temperatures. Since the FSR's resistance does not remain constant over temperature, the SLG47004V becomes responsible for maintaining this output voltage.

In this application, the SLG47004V's rheostats are used for their auto-trim capabilities, which adjust their resistance to match an internally generated reference voltage. This auto-trim process occurs whenever a high signal is provided to the rheostat's "SET" pin. When this signal is brought high, either externally or via internal logic, the auto-trim process begins. A waveform of this process is provided at the end of this section, which shows the "SET" signal being brought high, and the voltage divider output voltage changing to match the internally set reference voltage which, in this waveform, is 1.5 V.

This auto-trim process, if implemented to occur periodically during the runtime of the device, will provide a very high level of consistency in the voltage divider's output voltage. This, in turn, allows for one of the SLG47004V's internal ACMPs to be used to detect press signals on the FSR and can be adjusted to detect presses at all temperatures within the range of the device.

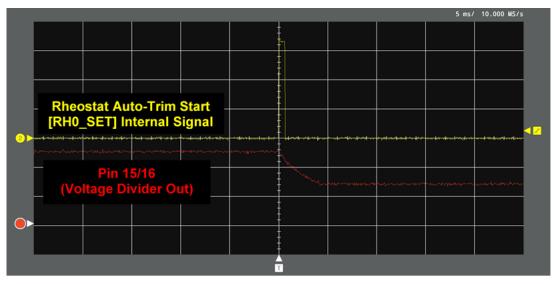


Figure 6: Auto-Trim Procedure

#### Vertical 1 V/div

#### Horizontal 5 ms/div

### 6 Results

Two points of functionality were measured to determine the success of the design. First, the design had to function as a button replacement, triggering the appropriate output signals in response to certain button-press sequences. Second, the device had to consume as little power as possible. Given that this type of design may be valued for its use in wearable technology, a maximum quiescent current of 10 uA was imposed as a design restriction.

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### 6.1 Button-Press Functionality

Waveform captures of various operation conditions of the FSR button setup can be found below with accompanying descriptions and labels. VDDA was, in this test, set to 3.3 V and the FSR was given a small amount of mechanical pre-loading. Additionally, the auto-trim reference voltage was set to 1.5 V, and the rheostat's "SET" signal was configured to be brought high by an internal counter block every 100 ACMP sample-cycles.

TAP_1 Signal (Pin	20)		
	Single Tap		
			auer puud kuungaar mengen daga pananggeun muda karangara
ACMP Threshold			
Voltage Divider Ou	itput (Pin 15/16	<b>5)</b>	

Figure 7: Single-Press Signal

Vertical 1 V/div

Horizontal 50 ms/div



#### Figure 8: Double-Press Signal

Vertical 1 V/div

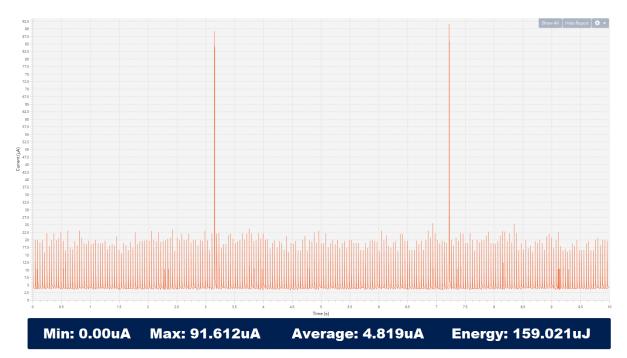
Horizontal 50 ms/div

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### 6.2 Current Consumption

Testing of quiescent current took place primarily at a sample rate of 25 Hz, as this is the lowest sample rate which seemed to provide an adequately responsive button design. A DC power monitor was used to capture the average Iq of the device, with external circuity included, over a period of ten seconds, and the sample rate of said power monitor was set to 50 kHz for these tests. Below is the capture window of said DC power monitor:



**Figure 9: Current Consumption Graph** 

The two spikes present in the capture represent the auto-trim windows of the design, which are responsible for modifying the SLG47004V's internal rheostat value to allow the voltage divider in the above schematic to match a reference voltage. Since the device has already been properly auto-trimmed at this point, the SLG47004V's internal chopper ACMP responsible for the auto-trim functionality is immediately turned off, thus resulting in a short spike. Each of the smaller spikes in the capture represents the SLG47004V's internal low-power ACMP being powered up to check if this reference voltage has dropped below a certain threshold, which would signal a button press has occurred.

The main testing parameter that prevents a higher level of precision when conducting this test is the fact that the force-sensitive resistor used in this design must be given a certain amount of mechanical "pre-loading" force in order for the resistance of the sensor to fall within a range that the SLG47004V can effectively auto-trim. This sensor is very sensitive to not only the amount of force on the sensor but to the exact position of the force on said sensor. Since the sensor is too small for various reference weights to be used, the average active current measurements can be observed to fluctuate between 4 uA and 5 uA from test-to-test.

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### 7 Conclusions

This design was tested at a number of sample rates, ranging from 10 Hz to 1 kHz. Of these sample rates, it was determined that to provide both adequate button performance and low power consumption, 25 Hz seemed to be the ideal ACMP sampling frequency. Under all tested conditions, however, the combination of SLG47004V and FSR proved to be a stable and well-performing button replacement solution.

## **Appendix A**

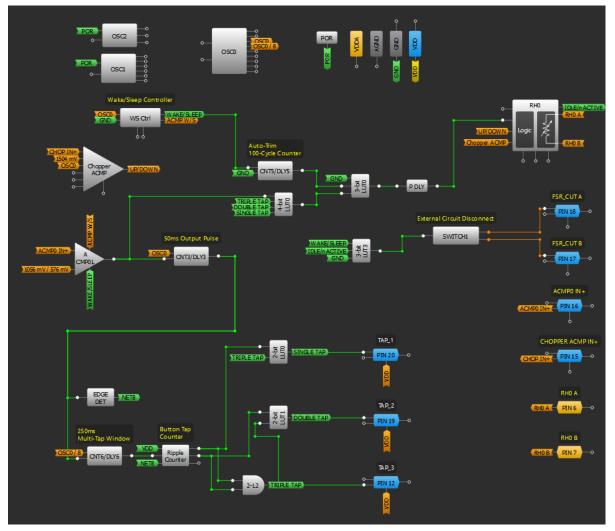


Figure 10: View in GreenPAK Designer

Applic	ation	Note





## **Revision History**

Revision	Date	Description
1.0	1-Jan-2021	Initial version



#### **Status Definitions**

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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