Application note

Suspend and Resume

AN-PM-007

Abstract

This document describes how to achieve suspend and resume behaviour with Dialog DA9052,DA9053, DA9021 and DA9022 PMIC devices.

Suspend and Resume

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1 Terms and definitions

DA905x	For this document this will be used to represent DA9021, DA9022, DA9052, DA9053 and DA9057
OTP	One Time Programmable: The type of memory used to store the configuration of the PMIC
PMIC	Power Management Integrated Circuit

2 References

[1] Power Commander User Guide, Dialog Semiconductor

3 Introduction

In many applications the system is required to enter a low power suspend or standby state, where at least some of the system configuration is maintained to allow the system to wake quickly and resume normal activity. This application note describes how this can be achieved with most members of the DA905x family. This note assumes that the system has already been configured so that it can achieve the normal active state. For the examples in this document, a DA9053 was used with the OTP programmed with the Dialog 3F configuration. For this document, the low power state will be referred to as Suspend.

4 Definition of SUSPEND

SUSPEND is a low power state that differs from POWERDOWN or OFF state in that a minimum number of supply rails are left on to allow the system to maintain a level of configuration so that normal operation can be resumed without the requirement to follow the normal boot sequence.

5 Preparation for SUSPEND

There is some basic information that is required to prepare the system to enter the SUSPEND state.

1. How will the system enter the SUSPEND state? Is it a hardware signal or an I^2C/SPI command?

   There are two possible triggers for the PMIC to enter the SUSPEND state. The first is a register write to the SYS_EN bit of the CONTROL_A register (bit 0 of address 0x0E). Clearing the SYS_EN bit causes the sequencer to step down from its current state to the POWERDOWN state. The alternative to the register write is to configure GPIO8 as a hardware SYS_EN. A transition on this hardware signal then triggers the sequencer.

2. What retention voltages are required to maintain the required system information/configuration?

   For this example it is assumed that the required regulators to be left on are:

   - BUCKCORE 0.85 V
   - BUCKPRO 0.95 V
   - LDO7 1.2 V
   - LDO10 1.2 V

   The nRESET signal should not trigger a reset of the processor during SUSPEND. Set NRES_MODE,,bit 0 of the ID_0_1 Register (R29) to ‘0’ to prevent the assertion of NRESET in SUSPEND.

3. What will trigger the system to Resume?

   There are multiple options to wake up the system from the SUSPEND state:

   - nONKEY
   - The hardware signal SYS_EN
   - A valid charger
   - An RTC alarm
   - An alternative signal, such as a GPIO

   Each of these events can be generated on the DA905x. The descriptions below show how each one can be implemented.

4. The SYS_PRE control, Bit 2 of the ID_0_1 register (R29), can be used to change the behaviour of the SYS_UP signal during SUSPEND. For correct SUSPEND functionality, Dialog recommend that SYS_PRE is set to ‘1’ so that the SYS_UP signal will go low during SUSPEND.

6 The SUSPEND RESUME sequence

This section describes the sequence of actions and events during one suspend resume cycle. The system is assumed to be booted up in the ACTIVE state.

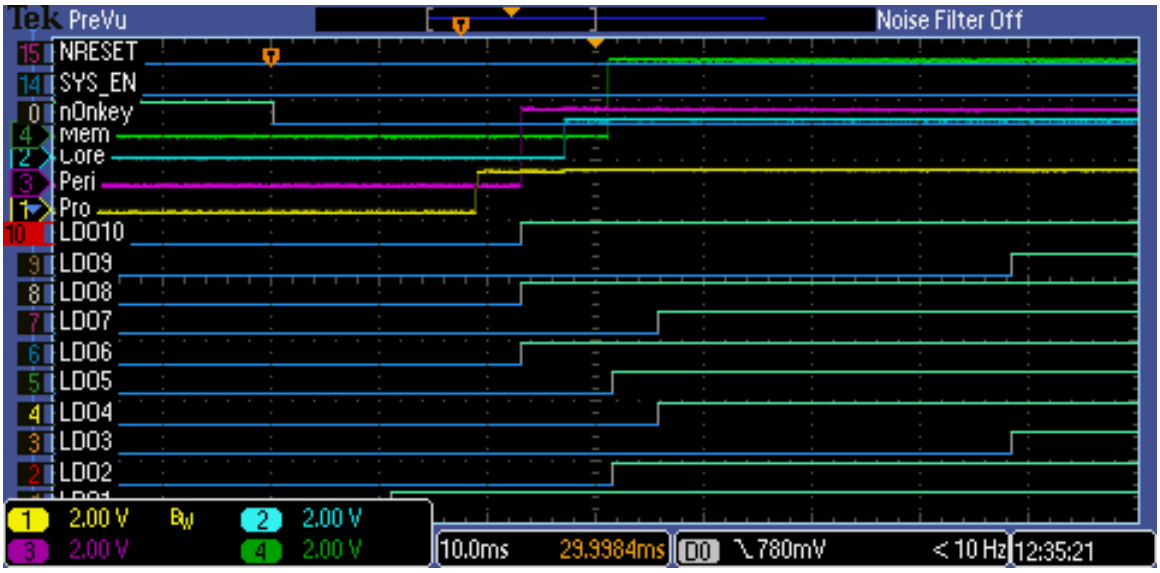

Figure 1: Normal start-up

Note that in Figure 1 nRESET goes high just after the period captured. Also note that the LDOs were connected to digital channels on the oscilloscope. The plot therefore indicates whether the LDO is on or off, but not the actual LDO voltage level.

6.1 Configure the PMIC for SUSPEND

Set NRES_MODE to ‘0’ in R29	// nRESET must not be asserted during SUSPEND
Set DEF_SUPPLY to ‘0’ in R29	// This must be cleared to allow the pre-set voltage mode to function
Set SEQ_TIMER (R43) to 0x00	// This sets the sequence time to minimum, for a fast in and fast out of SUSPEND.
Set R46 to 0x8E	// Set the CONF bit and the pre-set voltage of BUCKCORE to 0.85 V
Set R47 to 0xD2	// Set the CONF bit and the pre-set voltage of BUCKPRO to 0.95 V
Set R56 to 0xC0	// Set the CONF bit and the pre-set voltage of LDO_7 to 1.2 V
Set R59 to 0xC0	// Set the CONF bit and the pre-set voltage of LDO_10 to 1.2 V

The NRES_MODE bit (bit 0 of R29) defines whether the nRESET signal is asserted when the PMIC enters the POWERDOWN state with regulators left enabled via the CONF bits. With NRES_MODE set to ‘0’, nRESET is not asserted. With NRES_MODE set to ‘1’, nRESET is asserted when powering down.

The CONF bit, which is the MSB of each of the LDO and buck registers, sets the regulator into pre-configure mode. With the CONF bit set, the voltage can then be configured without immediately changing the voltage of the regulator. The new voltage is applied when the sequence pointer next reaches the active slot for that particular regulator. For the CONF bits to function correctly, DEF_SUPPLY (bit 1 of R29) must be set to ‘0’.

6.2 SUSPEND

Clear the SYS_EN bit in the CONTROL_A register to go to the SUSPEND state.

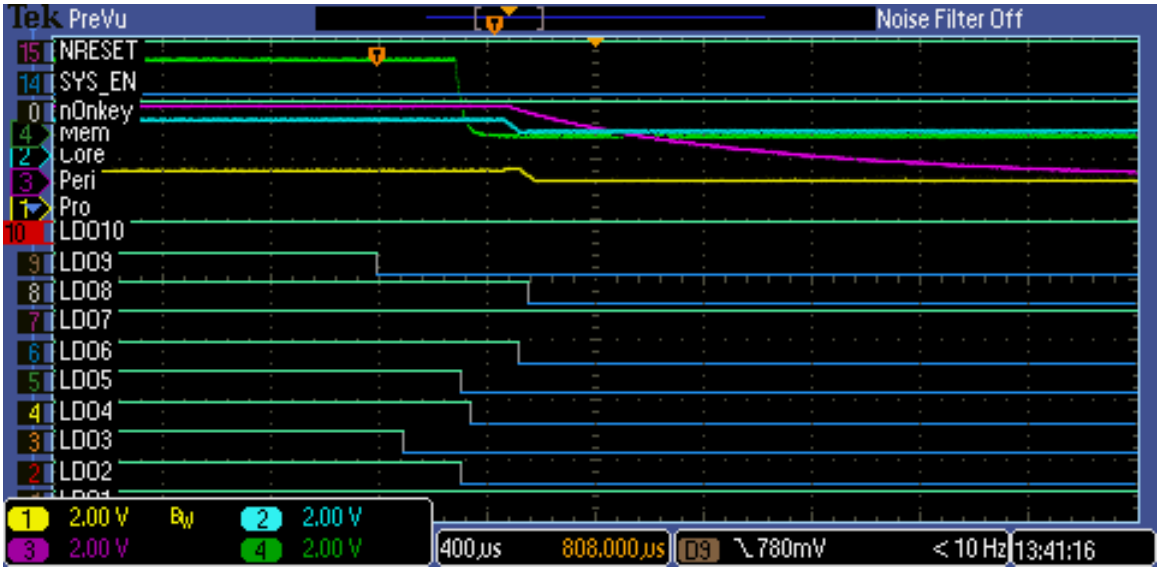

Figure 2: SUSPEND triggered by SW SYS_EN

BUCKCORE and BUCKPRO can be seen to change their voltage but remain active, as do LDOs 1, 7 and 10. All other supplies are disabled.

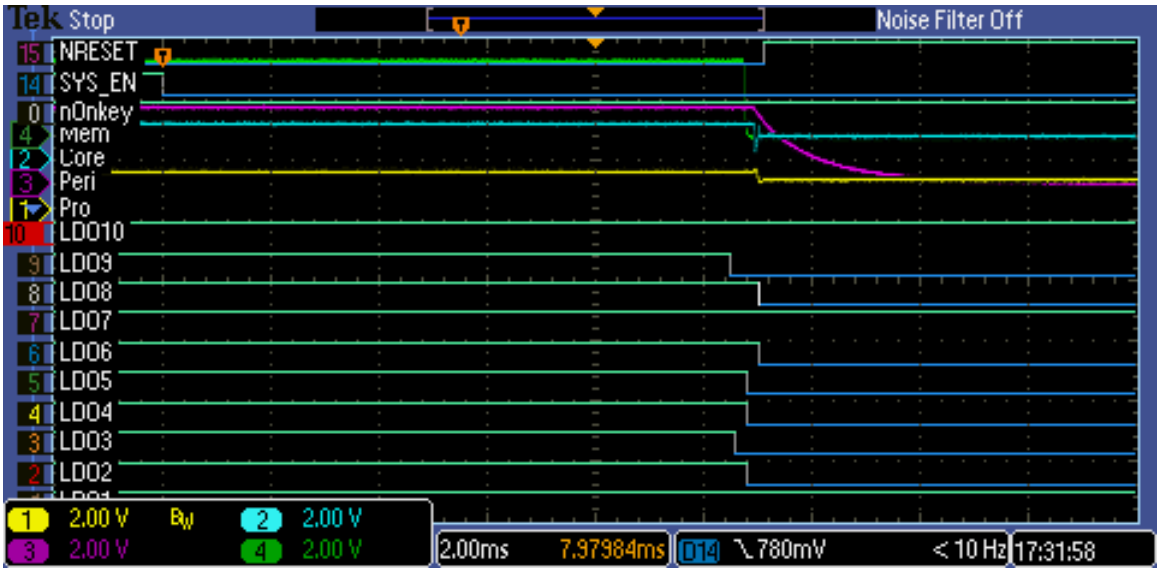

Figure 3: SUSPEND triggered by hardware SYS_EN low

To permit the hardware SYS_EN signal to trigger the SUSPEND state, GPIO8 must be configured to be hardware SYS_EN. SYS_EN can be configured as active high or low. The GPIO is configured via R25.

6.3 RESUME

When the RESUME event occurs, the supplies revert to their OTP programmed values. For this to happen correctly, the OTPREAD_EN (bit 3) of register CONTROL_B (R15) must be set. This bit triggers a partial OTP read on leaving the POWERDOWN state of the sequencer. The partial OTP read will read the buck and LDO registers to reset the regulator voltages to the original OTP programmed values. The CONTROL_A register is also read during this partial read: this can be used to reconfigure the SYS_EN bit to allow the sequencer to continue.

The figures below show the RESUME triggered by the various options.

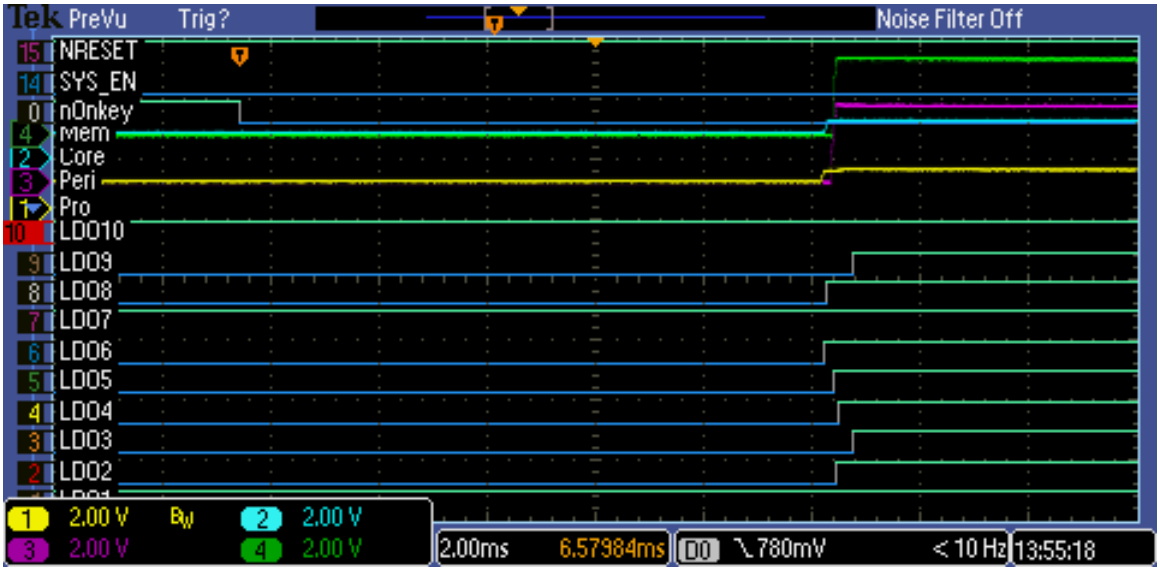

Figure 4: RESUME triggered by nONKEY

Figure 5: Expanded view of RESUME triggered by nONKEY

Figure 5 illustrates only slight increases in voltage on BUCKPRO (yellow trace) and BUCKCORE (blue trace), rising from 0.95 V and 0.85 V, respectively; BUCKMEM (green trace) and BUCKPERI (magenta trace) resume from the OFF state.

Suspend and Resume

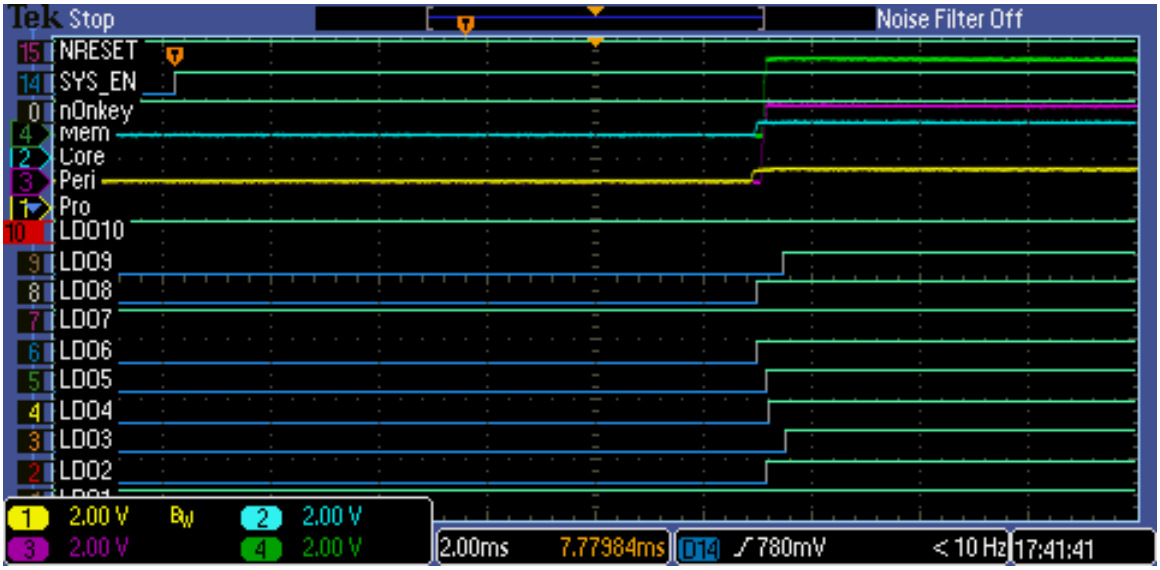

Figure 6: RESUME triggered by rising SYS_EN

To permit the hardware SYS_EN pin to trigger a resume, R25 should be configured with GPIO8 set as hardware SYS_EN and debounce enabled.

The value for the lower four bits of GPIO_8-9 (R25) should be 0xC for an active high SYS_EN and 0x8 for an active low SYS_EN.

Figure 7: RESUME triggered by charger

The wake-up may be triggered by a valid charger detection on either VBUS or DCIN. In Figure 7 the charger is connected to VBUS and it is shown that the resume sequence starts 10 ms after the charger is detected. The 10 ms delay is due to the debounce on the charger detect.

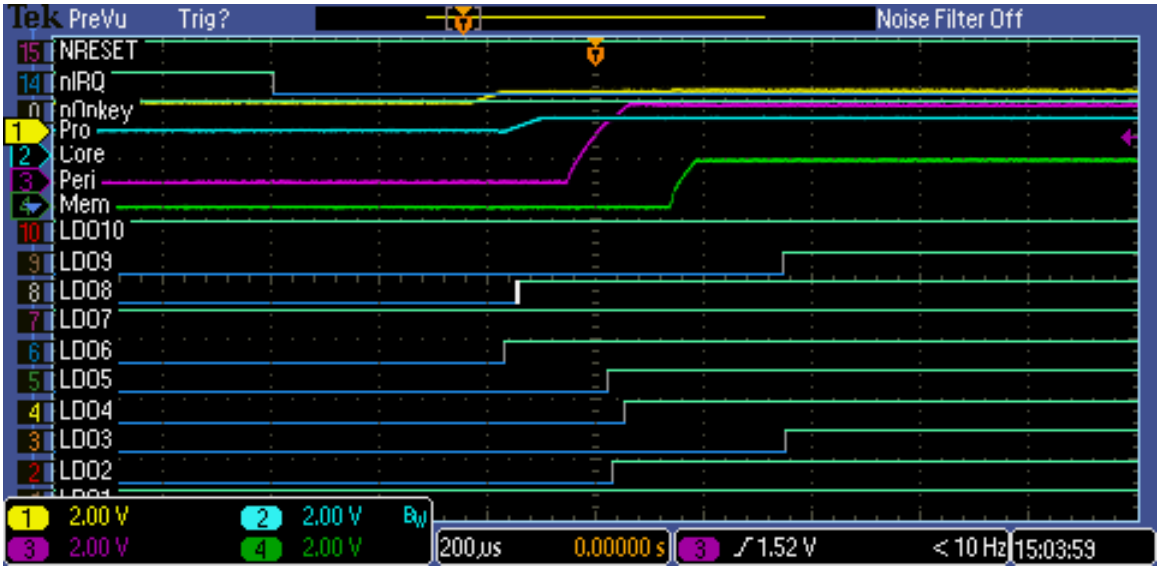

Figure 8: RESUME triggered by RTC Alarm

Figure 8 shows the RESUME triggered by an alarm from the RTC. In this case the trigger event is seen as the interrupt (nIRQ). The RTC wakeup can either be the RTC alarm or the RTC tick function.

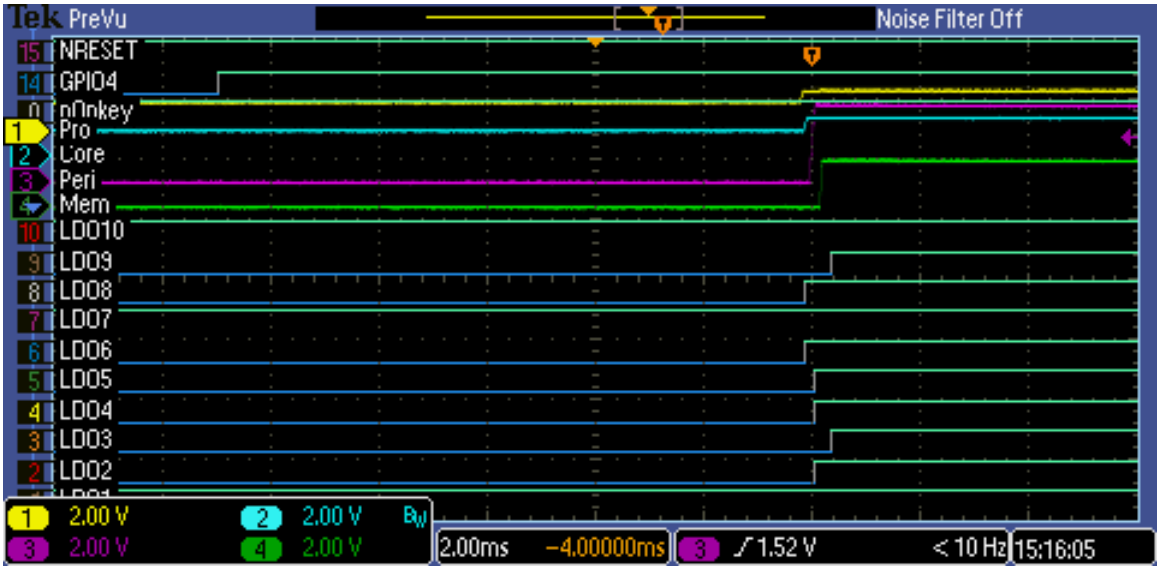

Figure 9: RESUME Triggered by GPIO4 rising edge.

Figure 9 shows the RESUME triggered by a rising edge on GPIO4. To use a GPIO, it must be programmed as a GPI and debounce must be enabled to trigger the wake-up.

7 System Power Off

While SUSPEND and RESUME are used to reduce power consumption during the normal operation of the system, the system will at some time be powered off.

When a system is using SUSPEND and RESUME, it is important that NRES_MODE (bit 0 of R29) is set back to ‘1’ before the system is shutdown. This ensures nRESET is correctly asserted when the device is fully powered down. This can safely be performed as part of the system shutdown procedure.

Appendix A Power Commander script

While performing the above tests, a simple Power Commander script was used to configure the part.

To use the script, cut and paste the text below into a text file and save into the data directory under the Power Commander installation.

The script can then be executed using the ‘File Operations’ option in the Power Commander GUI. See the Power Commander User Guide for further information on using scripts.

```
//Configure the PMIC for SUSPEND using hardware SYS_EN

PMIC     0x1D      0x00
PMIC     0x2B      0x00
PMIC     0x2E      0xCE
PMIC     0x2F      0xD2
PMIC     0x38      0xC0
PMIC     0x3B      0xC0
PMIC     0x19      0x7C
```

Revision history

Revision	Date	Description
1.0	22-Mar-2012	Initial version.
1.1	02-Jun-2015	Updated to use new template.
1.2	10-Jul-2015	Minor corrections following review.
1.3	26-Jan-2016	Expanded DA905x to list of relevant parts in abstract.

Suspend and Resume

Status definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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RoHS Compliance

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