# Application Note

## DA9063 Voltage Monitoring

### AN-PM-024


## Abstract

*This application note supplements the DA9063 datasheet with further detail of the monitoring feature for the input voltage (VSYS) and output voltages (LDOs, bucks), and also describes manual monitoring of rails*

# Contents



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# 1 Terms and Definitions

| | |
|---|---|
| LDO | Low DropOut voltage regulator. Used in battery operated systems, where the output voltage is typically lower than the input voltage. |
| PMIC | Power Management Integrated Circuits. Integrated circuits for managing power requirements of the host system. |

# 2 References

[1] DA9063, Datasheet, Dialog Semiconductor.

 

# 3 Introduction

The monitoring of input and output voltages on a PMIC is valuable for most applications. The range of signals and internal events described in this document allows Dialog's DA9063 to provide many opportunities to indicate and handle input/output out-of-range conditions.

# 4 Signals and Registers Overview

DA9063 provides several signals and internal events to help monitor input voltage VSYS and output voltages (bucks and LDOs).

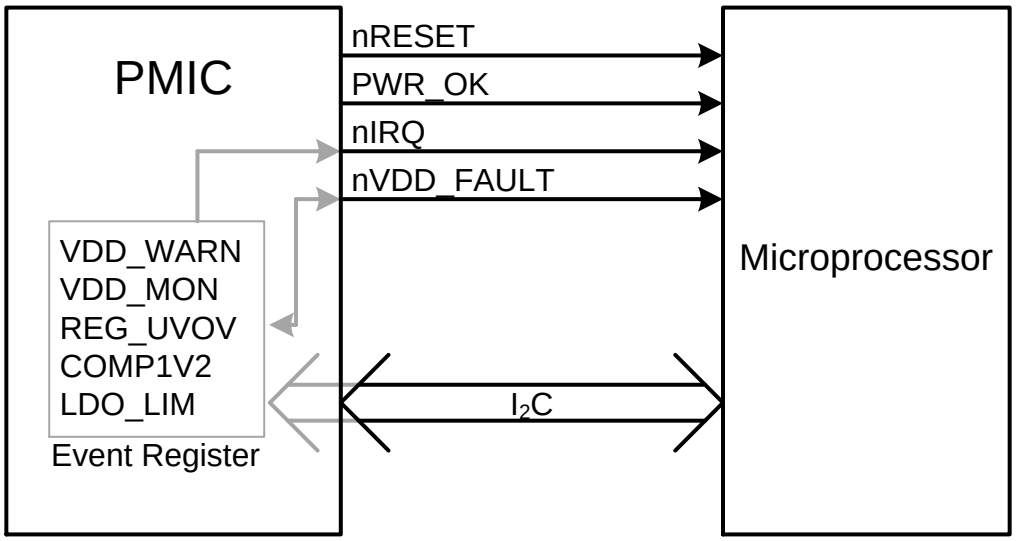


**Figure 1: Signals and Registers used for Voltage Monitoring**

**Table 1: Signal Descriptions**

| Signal | Description |
|---|---|
| PWR_OK | Out-of-range output detection via ADC (LDOs and bucks). |
| nIRQ | Indicates that an interrupt event has occurred and that event information is available in the related registers. |
| nVDD_FAULT | Indicates a supply voltage (VSYS) low status. |
| nRESET | Asserted if microprocessor enters the RESET state. |

**Table 2: Event Descriptions**

| Event | Description |
|---|---|
| VDD_WARN | VSYS dropped below VDD_FAULT_UPPER threshold. |
| VDD_MON | VSYS crossed VSYS_MON threshold. |
| REG_UVOV | Regulator output underflow or overflow. |
| COMP1V2 | 1.2 V comparator (ADC channel 2) state changed. |
| LDO_LIM | LDO3, 4, 7, 8 or 11 current limit exceeded for more than 10 ms |

# 5 VSYS Monitoring

The system supply voltage, VSYS, is monitored with two comparators as shown in Figure 2.

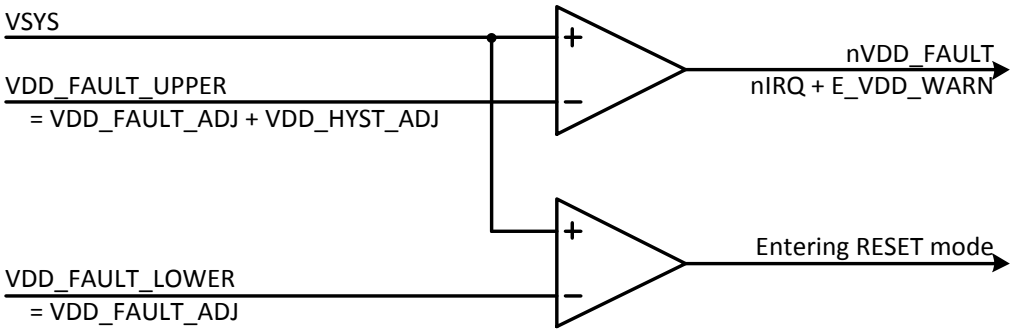


**Figure 2: VSYS Monitoring**

## 5.1 VSYS Under-Voltage, E_VDD_WARN, nIRQ and nVDD_FAULT

The first comparator monitors the higher voltage threshold, VDD_FAULT_UPPER. Whenever VSYS voltage goes below VDD_FAULT_UPPER, the system issues the warning E_VDD_WARN and sets nIRQ low (unless it is masked), so the system can run safety routines, backup data and power-down securely. Simultaneously, nVDD_FAULT (available on GPIO12) goes low. E_VDD_WARN and nIRQ output can be de-asserted at any time during the under-voltage condition. The nVDD_FAULT output is strictly driven by the comparator. Its type is push-pull only and active level is selected by GPIO12_MODE: active-low (0) or active-high (1). The nIRQ output is either active-low push-pull (PM_O_TYPE = 0) or active-low open-drain (PM_O_TYPE = 1) and can be supplied from either VDD_IO1 (PM_O_V = 0) or VDD_IO2 (PM_O_V = 1).

The second comparator monitors the lower voltage threshold, VDD_FAULT_LOWER. Whenever VSYS voltage goes below VDD_FAULT_LOWER, the PMIC enters RESET mode.

Both thresholds (VDD_FAULT_UPPER and VDD_FAULT_LOWER) are adjustable by OTP configurable register CONFIG_B. VDD_FAULT_LOWER is set directly by VDD_FAULT_ADJ in the register from 2.5 V to 3.25 V in 50 mV steps. VDD_FAULT_UPPER is set indirectly by VDD_HYST_ADJ (VDD_FAULT_UPPER = VDD_FAULT_ADJ + VDD_HYST_ADJ).

VDD_HYST_ADJ hysteresis is adjustable from 100 mV to 450 mV in 50 mV steps.

## 5.2 VDD_MON, nIRQ

The VDD_MON event is detected based on a comparison of the supply voltage VSYS and the VSYS_MON threshold as shown in Figure 3.

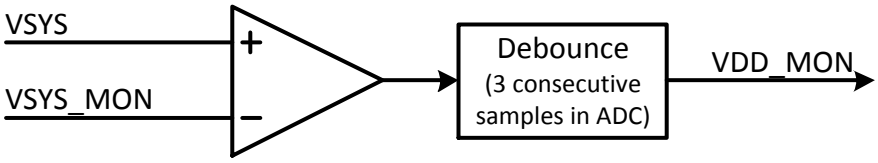


**Figure 3: VDD_MON Event**

VDD_MON is asserted whenever the VSYS voltage value in ADC exceeds or drops below the adjustable threshold VSYS_MON for three consecutive samples, see Figure 4. nIRQ is asserted simultaneously with VDD_MON (unless it is masked). This provides a ‘power good’ signal to trigger boot activity on the microprocessor.

After the nIRQ assertion, the automatic measurement of channel VSYS is paused for reading. The event causing the voltage value is kept inside the result register, VSYS_RES. The host has to clear the VDD_MON flag to re-enable the supervision of VSYS.

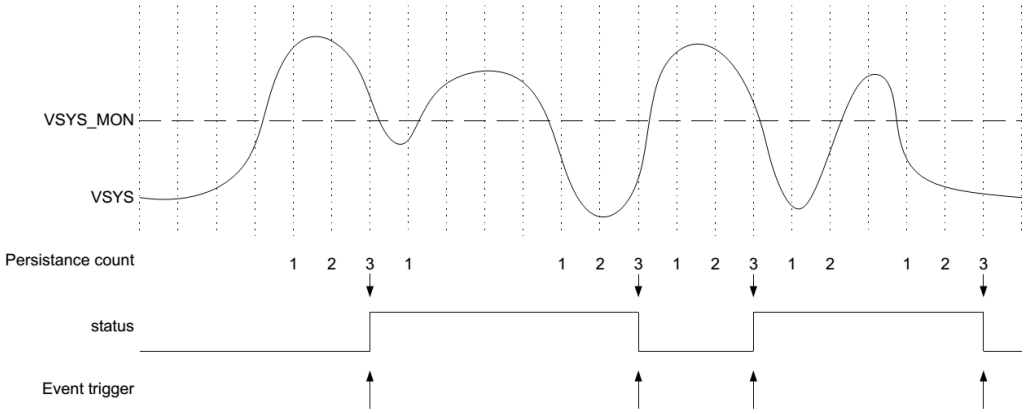


**Figure 4: VDD_MON Debouncing**

VSYS_MON threshold can be adjusted by setting the VSYS_MON register, the range is from 2.5 V (VSYS_MON = 0x00h) to 5.5 V (VSYS_MON = 0xFFh). VSYS auto measurements must be enabled (AUTO_VSYS_EN = 1).

VDD_MON output is push-pull type and can be either active low (GPIO12_MODE = 0) or active high (GPIO12_MODE = 1).

The nIRQ output is either active-low push-pull (PM_O_TYPE = 0) or active-low open-drain (PM_O_TYPE = 1) and can be supplied from either VDD_IO1 (PM_O_V = 0) or VDD_IO2 (PM_O_V = 1).

### 5.2.1 VDD_MON Example Settings

Before proceeding, clear all interrupt events (ensure the nIRQ output is high).

**Table 3: Example Settings for VDD_MON Voltage Detection**

| Setting | Description |
|---|---|
| AUTO_VSYS_EN = 1 | VSYS auto measurements enabled. |
| VSYS_MON = 0x44h | VSYS_MON threshold is set to 3.3 V. |
| GPIO12_PIN = 0x02h | Output is controlled by the state of VSYS monitor. |
| GPIO12_MODE = 0 | Output is active-low push-pull type. |

A VDD_MON event is asserted as soon as three consecutive samples under or over VDD_MON thresholds are recognized. The nIRQ output is asserted simultaneously with VDD_MON (unless it is masked). The voltage value that triggered the event is stored in the result register, VSYS_RES (VSYS_RES = 0x00h is equal to VSYS = 2.5 V; VSYS_RES = 0xFFh is equal to VSYS = 5.5 V).

## 5.3 VSYS Power-up

VSYS monitoring contains additional mechanisms to prevent an application starting from a weak power supply, example voltages are shown in Figure 5.

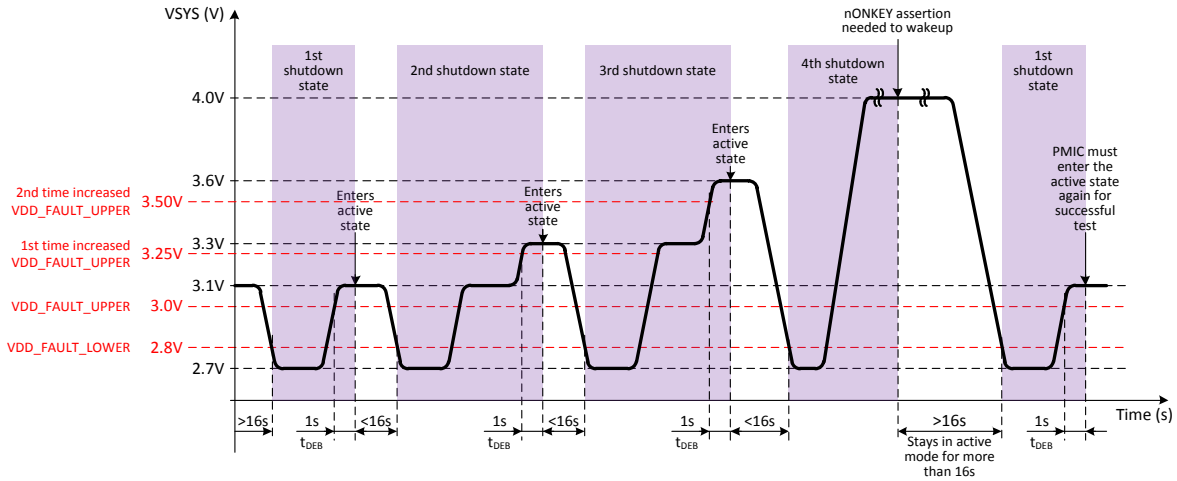


**Figure 5: VSYS Power-up**

If DA9063 is started and the VSYS voltage drops below the VDD_FAULT_LOWER threshold (possibly because of a high load), it enters SHUTDOWN state. Next time it starts, VSYS has to go above VDD_FAULT_UPPER + 0.25 V in order to enter the ACTIVE state. If VSYS drops below VDD_FAULT_LOWER again, the next time it has to cross VDD_FAULT_UPPER + 0.50 V. The VDD_FAULT_UPPER threshold is not further increased. The timeout for voltage drop is 16 s (the voltage has to drop within 16 s) so the VDD_FAULT_UPPER threshold is increased after the next start up. DA9063 also cannot enter an ACTIVE state before $t_{DEB}$ debounce time expires (typically 1 s) after crossing the appropriate threshold, see Figure 5.

# 6 Monitoring Output Voltages

## 6.1 PWR_OK

PWR_OK becomes active if none of the selected regulators are out-of-range. It is available through the GP_FB2 pin, when PM_FB2_PIN = 0 and the REG_UVOV interrupt is masked (M_REG_UVOV = 1). Monitored regulator outputs must be enabled, otherwise the out-of-range condition is detected. In the case where at least one of the supervised regulators is out-of-range or a monitored regulator output is disabled, the PWR_OK signal becomes inactive. There are also five special cases for the PWR_OK:

- If the supply monitoring is disabled, so that none of the supplies are monitored, the PWR_OK becomes inactive.
- The output voltage monitoring is not available for BUCKPRO in the DDR memory termination mode.
- When BUCKCORE1, BUCKCORE2 and BUCKMEM, BUCKIO are configured in merged mode only the master buck should be monitored. BUCKCORE1 and BUCKMEM are the master bucks.
- The GPIO4 pin should be configured as the remote feedback for BUCKCORE1 and BUCKCORE2 in merged mode because the GP_FB2 pin is needed for PWR_OK.
- If any of the monitored LDOs are configured in bypass mode, the PWR_OK becomes inactive.

If any regulator is out-of-range, its ID is stored in MON_A8_IDX, MON_A9_IDX, or MON_A10_IDX, see Table 4. The last voltage measurement from the MON_A8_IDX group is stored in MON1_RES, from the MON_A9_IDX group in MON2_RES and from the MON_A10_IDX group in MON3_RES.

**Table 4: Assignment of Regulators for Voltage Monitoring**

| Register Address | Bit | Type | Label | Default | Description |
|---|---|---|---|---|---|
| 0x118 MON_REG_5 | 7 | R | Reserved | 0 | |
| | 6:4 | R | MON_A9_IDX | 000 | Latest measurement at channel A9 was:<br>000: none<br>001: BUCKIO<br>010: BUCKMEM<br>011: BUCKPERI<br>100: LDO1<br>101: LDO2<br>101: LDO5<br>> 110: reserved |
| | 3 | R | Reserved | 0 | |
| | 2:0 | R/W | MON_A8_IDX | 000 | Latest measurement at channel A8 was:<br>000: none<br>001: BUCKCORE1<br>010: BUCKCORE2<br>011: BUCKPRO<br>100: LDO3<br>101: LDO4<br>110: LDO11<br>> 110: reserved |
| 0x119 MON_REG_6 | 7 | R | Reserved | 0 | |
| | 6:4 | R | Reserved | 000 | |
| | 3 | R | Reserved | 0 | |

| Register Address | Bit | Type | Label | Default | Description |
|---|---|---|---|---|---|
| | 2:0 | R | MON_A10_IDX | 000 | Latest measurement at channel A10 was:<br>000: none<br>001: LDO6<br>010: LDO7<br>011: LDO8<br>100: LDO9<br>101: LD10<br>> 101: reserved |

PWR_OK is either active-low push-pull (GP_FB2_TYPE = 0) or active-high open-drain (GP_FB2_TYPE = 1). The active-low push-pull is chosen to avoid permanently draining current through a pull resistor while the system is active.

### 6.1.1 PWR_OK Example Settings

Before proceeding, clear all interrupt events (ensure the nIRQ output is high).

**Table 5: Example Settings for LDO1 and IO Buck Output Monitoring**

| Setting | Description |
|---|---|
| M_REG_UVOV = 1 | Mask bit for REG_UVOV must be set to enable PWR_OK functionality. |
| PM_FB2_PIN = 0 | GP_FB2 output has PWR_OK functionality. |
| GP_FB2_TYPE = 0 | Active-low output. GP_FB2 is low if outputs are within range. GP_FB2 is high if any output is out-of-range. |
| MON_MODE = 0x00h | UV/OV event when out-of-range |
| MON_DEB = 1 | Debouncing on |
| MON_THRES = 0x00h | Monitored output threshold accuracy is ±25 %. |
| VLDO1_A = 0x14h | LDO1_A voltage is 1.0 V. |
| VLDO1_SEL = 0 | LDO1_A voltage is on LDO1 output. |
| LDO1_EN = 1 | LDO1 output enabled. |
| VBIO_A = 0x0Ah | BIO_A voltage is 1.0 V. |
| VBIO_SEL = 0 | BIO_A voltage is on BIO output. |
| BIO_EN = 1 | BUCKIO output enabled. |
| LDO1_MON_EN = 1 | Monitoring of LDO1 output voltage enabled. |
| BIO_MON_EN = 1 | Monitoring of BUCKIO output voltage enabled. |

Both LDO1 and VBIO voltages are monitored for minimum voltage 0.75 V (1.0 V – 25 % = 1.0 V * 0.75) and maximum voltage 1.25 V (1.0 V + 25 % = 1.0 V * 1.25). If any of these thresholds are exceeded, PWR_OK output is de-asserted.

If LDO1 exceeds the upper limit (1.25 V), the settings in Table 6 are performed.

**Table 6: LDO1 Exceeding the Upper Limit**

| Setting | Description |
|---|---|
| E_REG_UVOV = 1 | PMIC detected under-voltage or over-voltage condition. |
| LDO1_EN = 1 | LDO1 output **stays** enabled. |
| MON_A9_IDX = 0x04h | Out-of-range condition detected on LDO2. |
| MON2_RES = 0x42h | Last output voltage before out-of-range detection. It should be higher than 0x3Fh (1.25 V). 0x00h corresponds to 0.0 V and 0xFFh corresponds to 5.0 V. |

### 6.1.2 Interrupt Asserted by PWR_OK and nIRQ

If the configuration for PWR_OK output is used, the REG_UVOV mask bit must be set (M_REG_UVOV = 1) and nIRQ is not asserted if an out-of-range condition is detected. If the interrupt should still be detected, it is possible to set both outputs (nIRQ and PWR_OK) as open-drain and connect them together, see Figure 6.

Open-drain settings:

GP_FB2_TYPE = 1 PWR_OK is active-high open-drain output type.

PM_O_TYPE = 1 nIRQ is active-low open-drain output type.

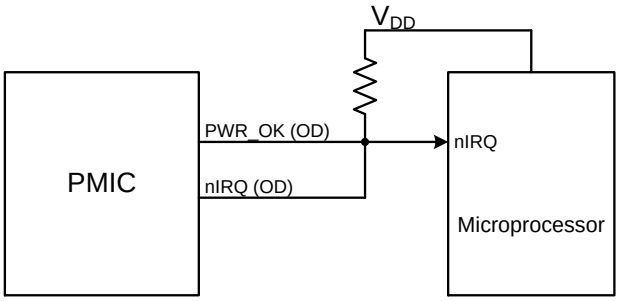


**Figure 6: Interrupt Asserted by PWR_OK and nIRQ**

## 6.2 nRESET

nRESET is asserted to force the microprocessor to enter the RESET state. In order to activate assertion of nRESET during an out-of-range condition, both MON_RES and M_REG_UVOV mask bits must be set high. Minimum assertion time is 1 ms.

nRESET is always asserted at the beginning of a DA9063 cold start from NO POWER / DELIVERY / RTC mode. It is asserted in ACTIVE mode before DA9063 starts powering down to RESET mode (triggered from user, host, or an error condition).

The nRESET signal is de-asserted following the expiry of the RESET_TIMER. The trigger for the RESET_TIMER is programmable by the OTP from EXT_WAKEUP, SYS_UP, PWR_UP, or leaving PMIC RESET state. The duration of the RESET_TIMER is programmable from 1 ms to 1 s. This flexibility allows the RESET functionality to be optimized for any host system.

nRESET can be asserted directly by setting FORCE_RESET signal (FORCE_RESET = 1).

The nRESET output is either active-low push-pull (PM_O_TYPE = 0) or active-low open-drain (PM_O_TYPE = 1). The nRESET can be supplied either from VDD_IO1 (PM_O_V = 0) or from VDD_IO2 (PM_O_V = 1).

### 6.2.1 nRESET Example Settings

**Table 7: Example Settings for LDO3 Output Monitoring**

| Setting | Description |
|---|---|
| M_REG_UVOV = 1 | Mask bit for REG_UVOV must be set to enable PWR_OK functionality. |
| MON_MODE = 0x00h | UV/OV event when out-of-range. |
| MON_DEB = 1 | Debouncing on. |
| MON_RES = 1 | nRESET output asserted if out-of-range condition is detected. The following registers **must** be set M_REG_UVOV = 1 and MON_MODE = 0x00h. |
| MON_THRES = 0x00h | Monitored output threshold accuracy is ±25 %. |
| VLDO3_A = 0x05h | LDO3_A voltage is 1.0 V. |
| VLDO3_SEL = 0 | LDO3_A voltage is on LDO3 output. |

| Setting | Description |
|---|---|
| LDO3_EN = 1 | LDO3 output enabled. |
| LDO3_MON_EN = 1 | Monitoring of LDO3 output voltage enabled. |

LDO3 output is monitored for minimum voltage 0.75 V (1.0 V – 25 % = 1.0 V * 0.75) and maximum voltage 1.25 V (1.0 V + 25 % = 1.0 V * 1.25). If any of these thresholds are exceeded, the nRESET output is asserted.

If LDO3 exceeds the upper limit (1.25 V), the settings in Table 8 are performed.

**Table 8: LDO3 Exceeding the Upper Limit**

| Setting | Description |
|---|---|
| E_REG_UVOV = 1 | PMIC detected under-voltage or over-voltage condition. |
| LDO3_EN = 1 | LDO3 output **stays** enabled. |
| MON_A8_IDX = 0x04h | Out-of-range condition detected on LDO3. |
| MON2_RES = 0x42h | Last output voltage before out-of-range detection. It should be higher than 0x3Fh (1.25 V). 0x00 corresponds to 0.0 V and 0xFF corresponds to 5.0 V. |

## 6.3 REG_UVOV, nIRQ

If any regulator is out-of-range, the REG_UVOV event is asserted. Its ID is stored in MON_A8_IDX / MON_A9_IDX / MON_A10_IDX and the last voltage measurements are stored in MON1_RES / MON2_RES / MON3_RES, see Table 4. At the same time as the REG_UVOV event, the nIRQ output is asserted.

Out-of-range can be adjusted in MON_THRES ranging from 3.125 % to 25 %.

The nIRQ output is either active-low push-pull (PM_O_TYPE = 0) or active-low open-drain (PM_O_TYPE = 1) and can be supplied from either VDD_IO1 (PM_O_V = 0) or VDD_IO2 (PM_O_V = 1).

### 6.3.1 REG_UVOV, nIRQ Example Settings

Clear all interrupt events (nIRQ output is high).

**Table 9: Example Settings for LDO2 and CORE1 Buck Output Monitoring**

| Setting | Description |
|---|---|
| M_UVOV_MASK = 0 | Mask bit for REG_UVOV must be set to enable PWR_OK functionality. |
| PM_O_TYPE = 0 | nIRQ output is active-low push-pull type. |
| PM_O_V = 0 | nIRQ is supplied from VDD_IO1. |
| MON_MODE = 0x00h | UV/OV event when out-of-range. |
| MON_DEB = 1 | Debouncing on. |
| MON_THRES = 0x00h | Monitored output threshold accuracy is ±25 %. |
| VLDO2_A = 0x14h | LDO2_A voltage is 1.0 V. |
| VLDO2_SEL = 0 | LDO2_A voltage is on LDO2 output. |
| LDO2_EN = 1 | LDO2 output enabled. |
| VBCORE2_A = 0x46h | BCORE2_A voltage is 1.0 V. |
| VBCORE2_SEL = 0 | BCORE2_A voltage is on BIO output. |
| BCORE2_EN = 1 | BCORE2 buck output enabled. |
| LDO2_MON_EN = 1 | Monitoring of LDO2 output voltage enabled. |

| Setting | Description |
|---|---|
| BCORE2_MON_EN = 1 | Monitoring of BCORE2 buck output voltage enabled. |

Both LDO2 and VBCORE2 voltages are monitored for minimum voltage 0.75 V (1.0 V – 25 % = 1.0 V * 0.75) and maximum voltage 1.25 V (1.0 V + 25 % = 1.0 V * 1.25). If any of these thresholds are exceeded, E_REG_UVOV event bit is set and the nIRQ output is asserted. Also the regulator output, which exceeded the limit, is disabled.

If LDO2 exceeds the upper limit (1.25 V), the settings in Table 10 are performed.

**Table 10: LDO2 Exceeding the Upper Limit**

| Setting | Description |
|---|---|
| E_REG_UVOV = 1 | PMIC detected under-voltage or over-voltage condition. |
| LDO2_EN = 0 | LDO2 output disabled. |
| MON_A9_IDX = 0x05h | Out-of-range condition detected on LDO2. |
| MON2_RES = 0x42h | Last output voltage before out-of-range detection. It should be higher than 0x3Fh (1.25 V). 0x00h corresponds to 0.0 V and 0xFFh corresponds to 5.0 V. |

nIRQ output is asserted (goes low).

## 6.4 Manual Measurement of Regulator Output Voltages

In addition to the automatic output voltage monitoring, the DA9063 also provides functionality to allow the host to make a manual measurement of the output voltage, of any of the enabled regulators, using the integrated ADC.

The key to all manual measurements using the DA9063 ADC is that the results are always returned in the ADC_RES registers ADC_RES_H, (0x38) and ADC_RES_L (0x37). ADC_RES_H contains the upper eight bits of the 10 bit result. ADC_RES_L bits 7:6 contain the two LSBs.

The 17 regulator outputs are split between three channels of the ADC. For the channel allocation, see Table 11.

To perform a manual measurement, both the ADC channel and the individual regulator index must be specified. The regulator index is written to the MON_Ax_IDX value in register MON_REG_5 (0x11E) or MON_REG_6 (0x11F). The ADC channel is selected by setting the ADX_MUX value, ADC_MAN[3:0].

Once both the ADC channel and the regulator index have been specified the manual measurement is triggered by writing a '1' to bit 4 of ADC_MAN,(0x34).

Note that bit 4 of ADC_MAN is a self-clearing bit and is cleared to indicate that the measurement is complete. Event E_ADC_RDY in register EVENT_A,(0x06) is also asserted to indicate that the measurement is compete and that the result is available to be read.

For more information about the ADC functionality, see the DA9063 datasheet [1].

The REG_RANGE ADC channels have a range of 0 V to 5 V. For the 10 bit manual measurements each LSB represents 4.883 mV.

**Table 11: ADC Channel Addressing**

| ADC Channel | Select Register | Regulator | Index |
|---|---|---|---|
| REG_RANGE1<br>ADX_MUX[3:0] = 0x1000 | MON_A8_IDX | BUCKCORE1 | 1 |
| | | BUCKCORE2 | 2 |
| | | BUCKPRO | 3 |

| ADC Channel | Select Register | Regulator | Index |
|---|---|---|---|
| | | LDO3 | 4 |
| | | LDO4 | 5 |
| | | LDO11 | 6 |
| REG_RANGE2<br>ADX_MUX[3:0] = 0x1001 | MON_A9_IDX | BUCKIO | 1 |
| | | BUCKMEM | 2 |
| | | BUCKPERI | 3 |
| | | LDO1 | 4 |
| | | LDO2 | 5 |
| | | LDO5 | 6 |
| REG_RANGE3<br>ADX_MUX[3:0] = 0x1010 | MON_A9_IDX | LDO6 | 1 |
| | | LDO7 | 2 |
| | | LDO8 | 3 |
| | | LDO9 | 4 |
| | | LDO10 | 5 |

### 6.4.1 Example of Manual Voltage Read

This section provides the details of how to perform the manual read.

For this example, BUCKCORE1 is set to 0.9 V and LDO3 is set to 1.2 V, and both regulators are already enabled.

Both BUCKCORE1 and LDO3 are assigned to ADC channel REG_RANGE1. The REG_RANGE1 select register is MON_REG_5:MON_A8_IDX.

BUCKCORE1 is index 1 on channel REG_RANGE1.

LDO3 is index 4 on channel REG_RANGE1.

**Table 12: Read BUCKCORE1 Voltage**

| Setting | Description |
|---|---|
| ADC_MUX[3:0]= 8h | Select ADC channel REG_RANGE1 |
| MON_A8_IDX = 0h | Select BUCKCORE1 |
| ADC_MAN = 1 | Trigger the manual conversion |
| | Read the result from ADC_RES_H & ADC_RES_L |

ADC_RES_H = 0x2E

ADC_RES_L=0x40

This results in a 10 bit value of 0010111001b =0x0B9 = 185dec.

The measured voltage is 185 * 4.883 mV = 0.903 V.

**Table 13: Read LDO3 Voltage**

| Setting | Description |
|---|---|
| ADC_MUX[3:0]= 0x8 | Select ADC channel REG_RANGE1 |
| MON_A8_IDX = 0x4 | Select LDO3 |
| ADC_MAN = 1 | Trigger the manual conversion |
| | Read the result from ADC_RES_H & ADC_RES_L |

ADC_RES_H = 0x3D

ADC_RES_L=0x80

This results in a 10 bit value of 0011110110b =0x0F6 = 246dec.

The measured voltage is 246 * 4.883 mV = 1.201 V.

# 7 Monitoring External Voltages

## 7.1 COMP1V2, nIRQ

A comparator with a threshold of 1.2 V is connected to the input of ADC channel 2, see Figure 7. The comparator is asserted whenever the input voltage exceeds or falls below 1.2 V for at least 10 ms (debouncing) after being enabled in COMP1V2_ENA. Status flag COMP1V2 is indicating the actual state and a maskable interrupt request E_COMP1V2 is generated at falling and rising edge state transitions. The user can disable the comparator in COMP1V2_EN when auto measurements with high resolution are executed on ADCIN2.

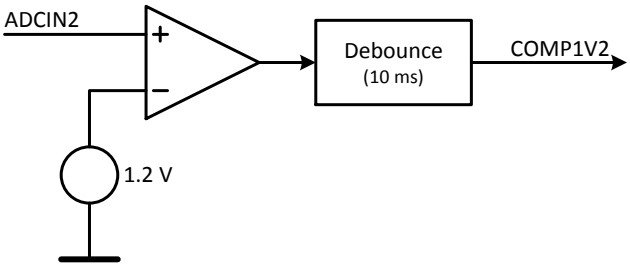


**Figure 7: COMP1V2 Comparator**

### 7.1.1 COMP1V2 Example Settings

Before proceeding clear all interrupt events (ensure the nIRQ output is high).

**Table 14: Example Settings for COMP1V2 Comparator**

| Setting | Description |
|---|---|
| GPIO1_PIN=0x00h | GPIO1 is used as an input of ADC channel 2. |
| COMP1V2_EN=1 | COMP1V2 comparator is enabled. |

Whenever the voltage on ADCIN2 input goes above or below 1.2 V for at least 10 ms, COMP1V2 event is detected and the nIRQ output is asserted (unless it is masked).

## Status Definitions

| Status | Definition |
|---|---|
| DRAFT | The content of this document is under review and subject to formal approval, which may result in modifications or additions. |
| APPROVED or unmarked | The content of this document has been approved for publication. |

## Disclaimer



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