Application Note

Testing DA906x with a Slowly Ramping Supply

AN-PM-056

Abstract

The Dialog DA906x family of power management ICs (DA9061, DA9062, DA9063) includes versatile supply voltage supervision to achieve reliable system design. Within a system development environment, an application might be tested with a slowing increasing supply voltage. In such a scenario, the device behavior may not be as expected. To enable such testing to proceed, a workaround is to set the M_VDD_WARN mask bit until the system is powered up.

Contents

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1 Terms and Definitions

PMIC	Power Management Integrated Circuit
DA906x	DA9061, DA9062, DA9063

2 References

[1] DA9063, Datasheet, Dialog Semiconductor

[2] DA9061, Datasheet, Dialog Semiconductor

[3] DA9062, Datasheet, Dialog Semiconductor

3 Introduction

The Dialog DA906x family of PMICs (DA9061, DA9062, DA9063) includes versatile supply voltage supervision that enables reliable system design. The PMIC monitors the voltage available on the VSYS supply and how it varies over time. This allows for clean start-up and shutdown of the system in all typical real system use cases.

A real system may power the PMIC VSYS main supply using a battery. This will produce a slowly decaying supply voltage. The DA906x PMICs monitor this decay, providing interrupts and event flags to allow software to manage the system response. When developing an application, the system designer may simulate this slowly decaying battery by using an external programmable power supply. However, in the lab it is possible to invert the ramp direction of the programmable supply to produce a slowing increasing voltage. With this development scenario, the Dialog DA906x may not respond as expected. This application note explains the behavior and provides a workaround.

4 Device Response to a Slowing Rising V_{SYS}

When starting the DA906x PMIC from NO POWER mode (V_{SYS} < 2.4 V) with a supply ramp rate of less than ~10 Vs^{-1}, the following occurs within the device:

1. When the V_{SYS} supply voltage is above 2.4 V (the typical Power On Reset level, V_POR_UPPER) and below VDD_FAULT_UPPER[1], the device is starting up and its internal voltage supervision comparators are enabled.
2. The voltage supervision circuit starts to check the supply voltage after a 100 ms debounce period. This period is intended to allow a V_{SYS} supply to reach its final level before monitoring begins.
3. If, after the 100 ms debounce, the supply is below the VDD_FAULT_UPPER reference, a VDD_WARN event is generated. (This would normally be indicative of a dropping supply voltage.)
4. The VDD_WARN event generates a system wakeup (to allow software to handle the event). The DA906x therefore begins to progress through the power-up sequence towards the ACTIVE state. As the device moves through the sequence, regulators may be turned on.
5. After a further 100 ms, if the supply is still below VDD_FAULT_LOWER[2], the device begins to shut down. Any regulators that had turned on will now turn off.
6. If the voltage rises again above VDD_FAULT_UPPER then, after a 1.0 s debounce, the DA906x will power up.

The above behavior is illustrated by comparing Figure 1 and Figure 2. A normal power-up is shown at (a) with the supply attaining its final voltage in much less than 100 ms. With a slowly discharging supply such as a battery, a VDD_WARN event is generated at (b) when V_{SYS} falls below VDD_FAULT_UPPER. When the supply falls below VDD_FAULT_LOWER at (c), a VDD_FAULT event is generated and the device powers down. With a slowly increasing V_{SYS} ramp, Figure 2 shows, 100 ms after starting upon reaching V_POR_UPPER, a VDD_WARN event is generated at (d) because V_{SYS} remains below VDD_FAULT_UPPER. The wakeup causes sequenced regulator(s) to turn on, but after only 100 ms the device powers down again because V_{SYS} remains below VDD_FAULT_LOWER.

[1] typically 2.95 V (programmable)
[2] typically 2.80 V (programmable)

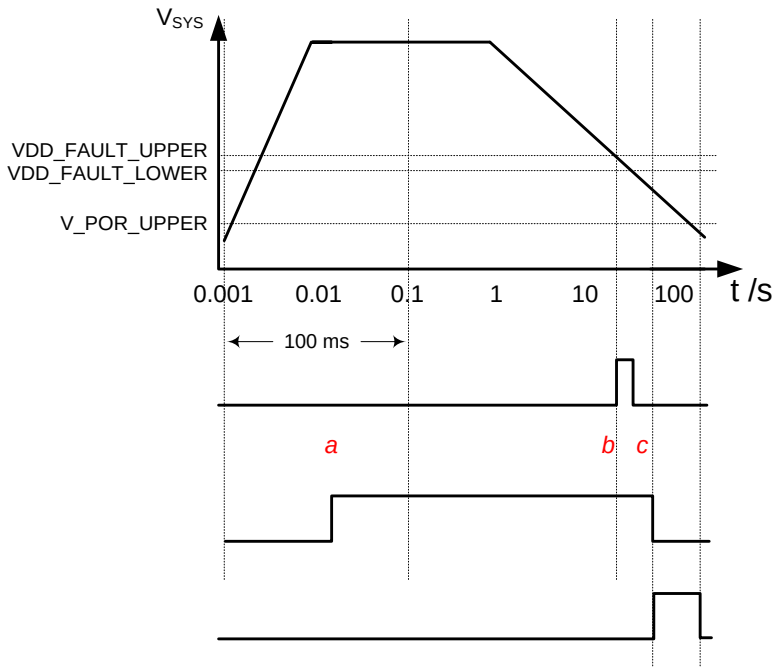

Figure 1: Normal V_{SYS} application: (a) normal power-up; (b) VDD_WARN event; (c) VDD_FAULT shutdown.

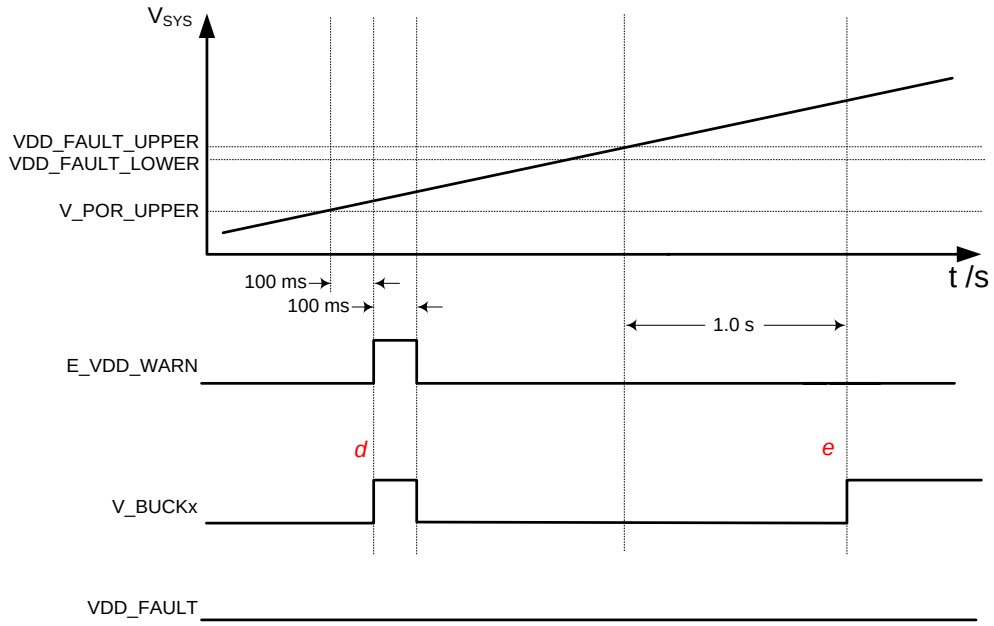

Figure 2: Slow V_{SYS} ramp: (d) wakeup attempt 100 ms after rising about V_POR_UPPER; (e) final power-up after V_{SYS} > VDD_FAULT_UPPER.

5 Workaround for Testing a Slowing Rising V_{SYS}

When using a programmable power supply with slowing rising V_{SYS}, the undesirable wakeup and VDD_WARN event can be eliminated by setting the M_VDD_WARN mask bit in register IRQ_MASK_B. This setting must be programmed into the device OTP so that it is present during the V_{SYS} ramp.

After the V_{SYS} ramp test is complete, with V_{SYS} at its nominal value and the system started, software can then clear the M_VDD_WARN mask to return the PMIC to a standard configuration.

6 Conclusion

When powering up a DA906x PMIC with a slowly ramping supply, expected behavior can be observed by using a programmed device OTP which includes register bit M_VDD_WARN set to ‘1’. This workaround is not required for normal system operation.

Revision History

Revision	Date	Description
1.2	07-Dec-2016	Corrected Figure 2 to show 1.0 s debounce starting when V_{SYS} rises above VDD_FAULT_UPPER.
1.1	13-Oct-2015	List of relevant products updated.
1.0	27-May-2015	Initial version

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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