Application Note

DA9061/2 Developers' Guide

AN-PM-060

Abstract

The DA9061 and DA9062 are PMICs optimized for supplying single- and dual-core systems. This application note is provided for system developers and offers guidance to supplement the datasheet specifications. It provides expanded descriptions of device functionality, application information such as PCB layout, and definitions for thermal design and parameter measurement.

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1 Terms and Definitions

Bandgap	The main internal voltage reference for the PMIC
GUI	Graphical User Interface
OTP	One-Time Programmable (memory). In this document, OTP refers specifically to the PMIC's non-volatile configuration memory.
PCB	Printed Circuit Board
PMIC	Power Management IC
Power Commander	User interface software (a GUI) to control the DA9061/2
PSRR	Power Supply Rejection Ratio
QFN	Quad Flat No-leads
RF	Radio Frequency
TDMA	Time Division Multiple Access

2 References

[1] DA9061, Datasheet, Dialog Semiconductor, 2018

[2] DA9062, Datasheet, Dialog Semiconductor, 2018

[3] AN-PM-063, DA9061/2/3 Configuration of nSHUTDOWN / nRESETREQ and nOFF, Dialog Semiconductor, 2015

[4] AN-PM-029, DDR3/DDR3L SDRAM complete power solution with the DA9063 including VTT terminations and VTTR reference, Dialog Semiconductor, 2015

[5] DA9061/2 GUI User Manual, Power Commander Software (Help Menu), Dialog Semiconductor, 2015

[6] AN-PM-010, PCB Layout Guidelines, Dialog Semiconductor, 2015

[7] AN-PM-024, Voltage Monitoring, Dialog Semiconductor, 2013

[8] AN-PM-080, In-Circuit Programming of DA9061/2/3, Dialog Semiconductor, 2018

3 Introduction

This guide provides system developers with information to supplement the DA9061 and DA9062 datasheet specifications. It principally addresses frequently asked questions (FAQs) relating to PMIC function and practical applications.

The flexibility of Dialog Semiconductor power management products allows configurations to suit most applications. Your Dialog support representative can assist in configuring DA9061/2 to meet your system requirements.

To understand the DA9061/2 and explore its comprehensive set of features, Dialog recommends using the SmartCanvas software (GUI). This provides a visual interface to help users understand the function of each control. Used in conjunction with the DA9061/2 Evaluation Kit (available to order), the GUI simplifies the development process for custom device configurations.

Many of the sections in this guide are written with respect to DA9062, but are applicable also to DA9061.

4 Detailed Functional Descriptions

The following information supplements the Functional Description section of the datasheets.

4.1 Power States and Sequencer Pointer

The device state and sequencer pointers have different names. Broadly, they align as listed in Table 1. For example, when the sequencer processes the slot containing POWER_END, the device

will generally enter the ACTIVE state. When the sequencer processes the slot containing MAX_COUNT, the device will enter the POWER1 state.

Table 1: Device States and Sequencer Power Domains

Sequencer Pointer	State (Power Domains)
Slot 0	POWERDOWN
PART_DOWN	STANDBY
SYSTEM_END	SYSTEM
POWER_END	ACTIVE
MAX_COUNT	POWER1

More detailed information regarding device state is provided in the following section.

4.2 Device Power Modes

The DA9061/2 power mode diagrams in the datasheets have been simplified to provide clear specifications. However, a more detailed version of the state diagram is presented in Figure 1. When developing a system with the Dialog Evaluation Kit and software (GUI), the state and its number (given in the figure within brackets) are also shown by the GUI.

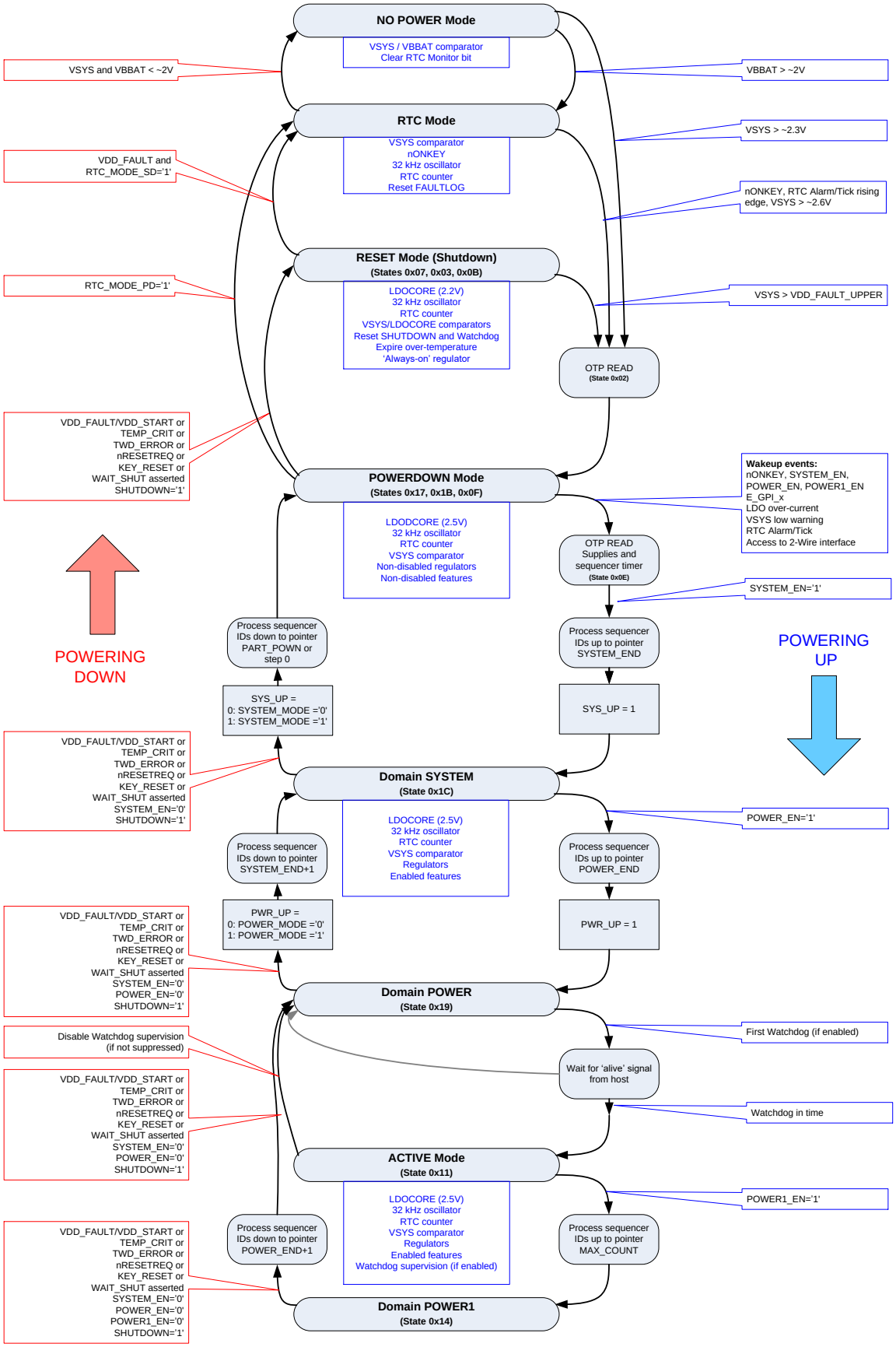

Figure 1: Power Mode Transitions

4.2.1 NO-POWER and RESET Mode

The DA9061/2 has an internal Power-On-Reset (POR) signal to control the PMIC start-up when a supply is first applied. The PMIC must be able to power its own internal core before it can function, otherwise it is held in an off state (NO-POWER mode). The PMIC only exits NO-POWER mode when the system can supply the internal logic supply VDDCORE at a voltage greater than a threshold V_{POR_UPPER}.

Similarly, there is an additional supply voltage threshold, $V_{DD\_FAULT\_UPPER}$, which must be crossed to allow the PMIC to power up into the POWERDOWN state. The device is held in RESET mode if V_{SYS} fails to rise above $V_{DD\_FAULT\_UPPER}$. In this state, the device is referred to as being in shutdown. The DA9061/2 datasheet power mode diagrams show this as a V_{SYS} error.

4.2.2 Exiting RESET Mode

The DA9061/2 progresses out of RESET mode into POWERDOWN mode. From POWERDOWN mode, the DA9061/2 continues through the power-up sequence if either:

- the power domain SYSTEM was enabled via GPIO4 configured as a SYS_EN input, or,
- the power domain SYSTEM and the AUTO_BOOT bit were both set in OTP.

With the AUTO_BOOT bit disabled and the power domain SYSTEM enabled in OTP settings (SYSTEM_EN bit set), a non-suppressed wake-up event allows the DA9061/2 to continue through the power-up sequence.

4.2.3 Masking the Domain Register Bits

CONTROL_A register is not only used as a control register, but is also used as a status register. The register bits SYSTEM_EN, POWER_EN and POWER1_EN have associated write mask bits M_SYSTEM_EN, M_POWER_EN and M_POWER1_EN. This allows writing to individual control bits without disturbing the other register bits. These bits protect the value of the associated control bit, therefore avoiding the need to do a read-modify-write.

4.3 Wake-Up Events

The DA9061/2 offers two types of wake-up event: user events and system events. Non-suppressed user events (for example nONKEY and GPIOs) are always processed and trigger a wake-up. Wake-ups progress the PMIC out of POWERDOWN mode. If a DA9062 device is in RTC mode, a wake-up event progresses the device out of this state.

The various types of wake-up event can be individually suppressed by setting the related IRQ mask bit. When nONKEY_LOCK is asserted, a wake-up requires the debounced signal from nONKEY to be low for a time longer than the configured KEY_DELAY. It is not recommended to mask system events: instead, disable the unwanted event sources (GPIs, for example). The wake-up from GPIs (or the selected alternate features that use a shared GPI event) has to be enabled via the GPIOx_WEN bits.

After a valid wake-up condition is detected, a subset of the OTP configuration is read and the values are used to reconfigure the regulator voltage registers Vxxx_A, the power domain enable settings (if not suppressed via SYSTEM_EN_RD) and the sequencer timing register SEQ_TIMER.

The DA9061/2 then configures regulators with an ID pointing at slot 0 to their target state (dependent on the DEF_SUPPLY settings). If the power domains are not pre-enabled from OTP settings, the host processor can control further application start-up via the power domain controls, SYSTEM_EN, POWER_EN, and POWER1_EN. The SYSTEM and POWER domains can also be enabled via the GPIO alternate functions SYS_EN and PWR_EN. Alternatively, the DA9061/2 continues powering up the OTP-enabled domains via the sequencer, but the power sequencer will not start to enable the SYSTEM domain supplies unless SYSTEM_EN is asserted.

4.4 VDD_START Faults and VDD_WARN

The DA9061/2 VDD_START feature prevents endless looping of false starts in a weakly-powered system. VDD_START limits the number of automatic restart attempts to three. With reference to Figure 2:

- Figure 2(a): The PMIC starts from NO-POWER mode.
- Figure 2(b): First startup attempt. The PMIC transitions to the ACTIVE state when V_{SYS} rises above $V_{DD\_FAULT\_UPPER}$.
- Figure 2(c): If, during the first startup attempt, the V_{SYS} supply drops below $V_{DD\_FAULT\_LOWER}$ for more than 100 ms, the PMIC shuts down to the SHUTDOWN state. $V_{DD\_FAULT\_UPPER}$ is increased automatically by 250 mV. However, the increased $V_{DD\_FAULT\_UPPER}$ is limited to a maximum of 3.70 V.
- Figure 2(d): Second startup attempt. If V_{SYS} rises above the new $V_{DD\_FAULT\_UPPER}$ threshold, then the PMIC will power-up to the ACTIVE state.
- Figure 2(e): If, during the second startup attempt, the V_{SYS} supply drops below $V_{DD\_FAULT\_LOWER}$ for more than 100 ms, the PMIC shuts down to the SHUTDOWN state. $V_{DD\_FAULT\_UPPER}$ is increased automatically by a further 250 mV (500 mV above its original setting). However, the increased $V_{DD\_FAULT\_UPPER}$ is limited to a maximum of 3.70 V.
- Figure 2(f): Third startup attempt. If V_{SYS} rises above the new $V_{DD\_FAULT\_UPPER}$ threshold, then the PMIC will power-up to the ACTIVE state.
- Figure 2(g): If, during the third startup attempt, the V_{SYS} supply drops below $V_{DD\_FAULT\_LOWER}$ for more than 100 ms, the PMIC shuts down. From then on, AUTO_BOOT and wake-up from non-user events are temporarily disabled. 'User events' are defined as an ONKEY press or a GPI passive to active transition where GPIO<x>_PIN = 0b01 and GPIO3_WEN = 1. GPIO4 configured as SYS_EN and GPIO2 configured as PWR_EN are not 'user events'.

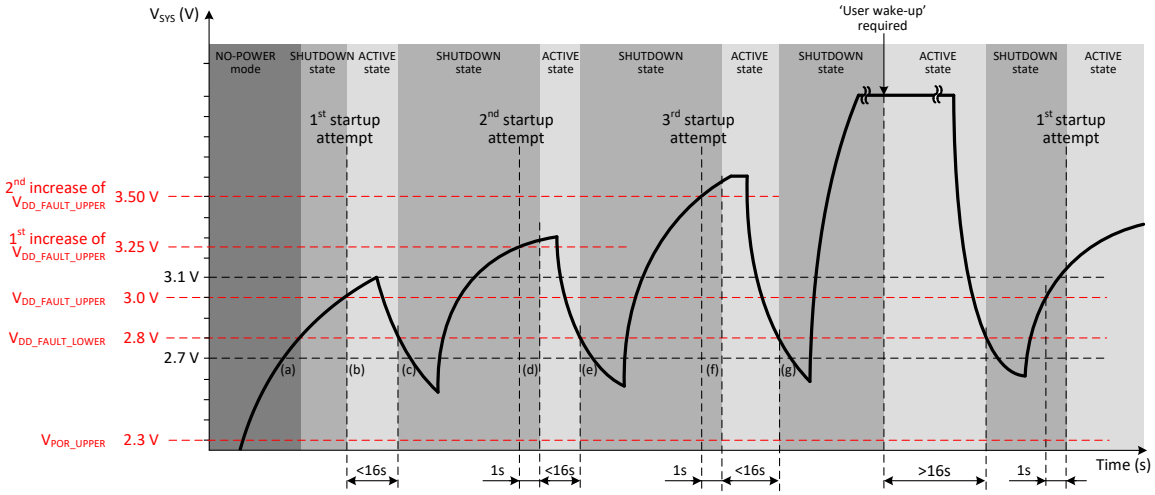

Figure 2: VDD_START Faults

NOTE

- During an attempt to restart, the entry into the ACTIVE state is delayed by 1 s.
- The ACTIVE state also includes POWER1 mode. The PMIC has the same VDD_START behavior from the POWERDOWN and SYSTEM modes as from the ACTIVE state.
- AUTO_BOOT and wake-up from non-user events are re-enabled after the application has successfully powered up to the ACTIVE state for more than 16 s. This also resets the start-up threshold to $V_{DD\_FAULT\_UPPER}$ + 0 mV.

Also refer to the V_{SYS} monitoring described in [1] and [2] in the System Supply Voltage Supervision sections, and Voltage Monitoring [7] for the DA9063.

nVDD_FAULT is a signal to the host processor to indicate a supply voltage (V_{SYS}) low status. Asserting nVDD_FAULT indicates that the main supply input voltage is low ($V_{SYS} < V_{DD\_FAULT\_UPPER}$) and therefore informs the host processor that the power will shut down soon. The event control E_VDD_WARN is asserted and the nIRQ line is asserted (if not masked). After that, the processor may operate for a limited time from the remaining battery capacity or the processor may enter a STANDBY mode. Even if V_{SYS} does not recover, the host can re-enable the nIRQ line by asserting M_VDD_WARN or clearing E_VDD_WARN.

4.5 Sequencer WAIT_STEP

With control bit WAIT_MODE = 0, the power sequencer will wait at the slot contained in WAIT_STEP until GPIO3 becomes active. This feature can be used, for example, to synchronize the PMIC state with the state of a host processor.

To begin the wait step, the event bit E_GPI3 must be clear. This is the typical case for a system cold-boot. The wait is terminated when an event is detected by the PMIC on GPI3. To use this feature during a warm-boot, such as waking up after a power-down from ACTIVE to POWERDOWN, the E_GPI3 bit must first be cleared of any previous GPI3 event. (The wait would therefore be skipped if the E_GPI3 bit is already set when entering WAIT_STEP slot.)

A safety timeout of 500 ms can be selected by asserting TIME_OUT. Then, if GPIO3 fails to become active within this period, the PMIC powers down to RESET mode. (This timeout fault causes the assertion of the WAIT_SHUT bit in the FAULT_LOG register.)

Alternatively, with control bit WAIT_MODE = 1, an asynchronous wait is possible. Its duration is configured by WAIT_TIME. For symmetric power-up/-down sequence timing, ID WAIT_STEP should not share a sequencer slot with other IDs.

In the case of an emergency shutdown sequence into RESET mode (for example due to a VDD_FAULT condition), the delay associated with WAIT_STEP is skipped.

4.6 LDO Default Supplies and Always-On Regulator

The controls for DA9061/2 regulators provide a high degree of configurability. The datasheet gives full details of the controls. As a supplement to that description, Table 2 is a guide to the most common use-cases. The main controls affecting behavior are LDO<x>_CONF, DEF_SUPPLY and LDO<x>_AUTO.

NOTE
The regulators are most commonly controlled by the sequencer or a GPIO pin. In these cases, the turning on of the LDO is controlled by the DA9061/2 itself. Therefore, the LDO<x>_EN bit is usually left as a '0' in OTP, and is only changed on-the-fly to a '1' by the PMIC's internal sequencer.

LDO<x>_CONF can be considered as a control to keep the LDO turned on when returning from the ACTIVE state to POWERDOWN mode.

The DEF_SUPPLY makes all un-sequenced regulators (where LDO<x>_STEP = 0) turn on in POWERDOWN mode. This happens as soon as the PMIC starts up from a cold boot (leaving NO-POWER mode) or when the PMIC leaves RTC / DELIVERY mode.

For most use-cases, LDO<x>_AUTO is set to '1'. Setting it to '0' is used for manual operation of the regulator where the LDO is turned on and off by simple I^2C writes to LDO<x>_EN.

Table 2: LDO Regulator Configuration Guide

DEF_SUPPLY	LDO<x>_CONF Note 1	LDO<x>_STEP	LDO<x>_GPI	LDO<x>_EN Note 2	LDO<x>_AUTO	Behavior
0	0	≥ 1	0	0	1	This is the typical use-case. The LDO is off when in POWERDOWN and on when in the ACTIVE state. The output voltage is set by VLDO<x>_A
0	1	≥ 1	0	0	1	This is used when the A-voltage and B-voltage feature is required. In the ACTIVE state, the LDO is at the voltage set by VLDO<x>_A. When returning from the ACTIVE state to POWERDOWN mode, the LDO remains turned on, but transitions to the voltage set by VLDO<x>_B. Setting VLDO<x>_A = VLDO<x>_B means the LDO remains at a fixed voltage after first entering the ACTIVE state, unless the PMIC passes through RESET Mode or RTC Mode.
1	1	0	0	0	1	Default supply. This configures the LDO as a default supply. With DEF_SUPPLY = 1, *all* LDOs with LDO<x>STEP = 0 turn on when powering up into Slot0. The output voltage is set by VLDO<x>_A.
1	0	0	0	0	0	This is for an unused supply or one that is to be controlled only by I^2C. The regulator therefore has LDO<x>_STEP = 0. But where DEF_SUPPLY = 1 is being used for other regulators, this configuration of LDO<x>_AUTO = LDO<x>_CONF = 0 prevents this regulator from also being turned on in Slot 0 / POWERDOWN.

Note 1 X = don't care.

Note 2 This is the value to be configured in OTP. This control is changed automatically by the PMIC during device operation.

NOTE

- In most use-cases, LDO<x>_EN control should be '0' in OTP. To configure a default supply, the method in Table 2 is recommended. Alternatively, it is possible to set LDO<x>_EN = 1 in OTP. This effectively forces the LDO to be enabled, and bypasses the other controls.
- LDO1 can be configured as an 'always-on' supply by configuring it as a 'default supply' as described in Table 2. Unlike the other LDOs, LDO1 remains on when the DA9061/2 passes through the RESET state. However, all LDOs including LDO1 are off in NO-POWER, RTC and DELIVERY modes.

4.7 Buck Default Supplies

Configuring a buck as a default supply follows a similar method as the LDOs, as described in Section 4.6 above.

4.8 Buck4 VTT Mode

This section only applies to DA9062.

4.8.1 VTTR Reference

The VTTR reference supply can be used independently of the Buck4 VTT feature. This might be required, for example, where an external discrete buck converter is used to drive the tracking supply voltage for a VTT termination network but cannot create the VTTR reference.

To configure the GPIO0 and GPIO1 pins as VTTQ and VTTR, the control bit BUCK4_VTTR_EN should be set. This does not affect the configuration of Buck4 which will continue to function as a normal buck when BUCK4_VTT_EN = 0.

Application note AN-PM-029 [4] provides further information regarding VTT termination using Dialog PMICs.

4.8.2 VTT Mode for DDR Termination

When using DA9062 Buck4 in VTT Mode for DDR termination (BUCK4_VTT_EN = 1), the following settings must be used: BUCK4_MODE = 0, BUCK4_SL_A = 1, BUCK4_SL_B = 1, VBUCK4_A = 0.71 V, VBUCK4_B = 0.71 V.

4.9 GP_ID Registers

These are general purpose read/write registers that can be used by the system for any purpose.

Data stored in GP_ID_10 to GP_ID_19 persist through a warm reset, such as triggered by the nRESETREQ pin or by the SHUTDOWN control in register CONTROL_F. The other GP_ID registers are reloaded from OTP. A cold-boot or exiting RTC mode reloads all GP_ID register values from OTP.

It might be found that Dialog has used GP_ID_0 for tracking OTP production variant information. If the GP_ID_0 register is required solely for system use, then please discuss this with your Dialog support representative.

4.10 Electronic Device Identification

The VRC field in register VARIANT_ID typically holds the following values: 0x1 = DA9061; 0x2 = DA9062. This is subject to change without notice.

4.11 Watchdog False Trigger Shutdowns

It is important to understand the implications of the t_{WDMIN} specification for minimum watchdog time. To protect the system against watchdog triggers that could be indicative of a malfunctioning system, the PMIC will shut down if more than one watchdog triggers are received by the PMIC within a period t_{WDMIN}. This applies to the 2-wire bus writes to the WATCHDOG bit in register CONTROL_F and also triggers via the GPIO_0 port (when appropriately configured with GPIO0_PIN = 00).

4.12 Register TRIM_CLDR

This register is for system development debug only. It has no purpose in volume manufacture.

4.13 Buck Soft-Start

To limit inrush current from VSYS, the buck converters are able to perform a soft-start. The duration of the start-up varies depending on buck configuration and load, but may take up to 3 ms. The soft-start feature is enabled by BUCK_SLOWSTART in register CONTROL_B. During normal start, the output voltage is temporarily held at the regulator's minimum voltage before ramping linearly to the set voltage. Simplistically, the buck behavior can be interpreted as being a current source during a soft-start and as a voltage source during a normal start.

NOTE
Soft-start limits the input current and therefore, if the demanded output load exceeds the current limit, the buck cannot achieve the required output voltage until the end of the 3 ms soft-start period. Figure 4 illustrates the voltage- and current-limiting period. The system developer should consider whether such a delay may represent an unintentional change to the start-up sequence.

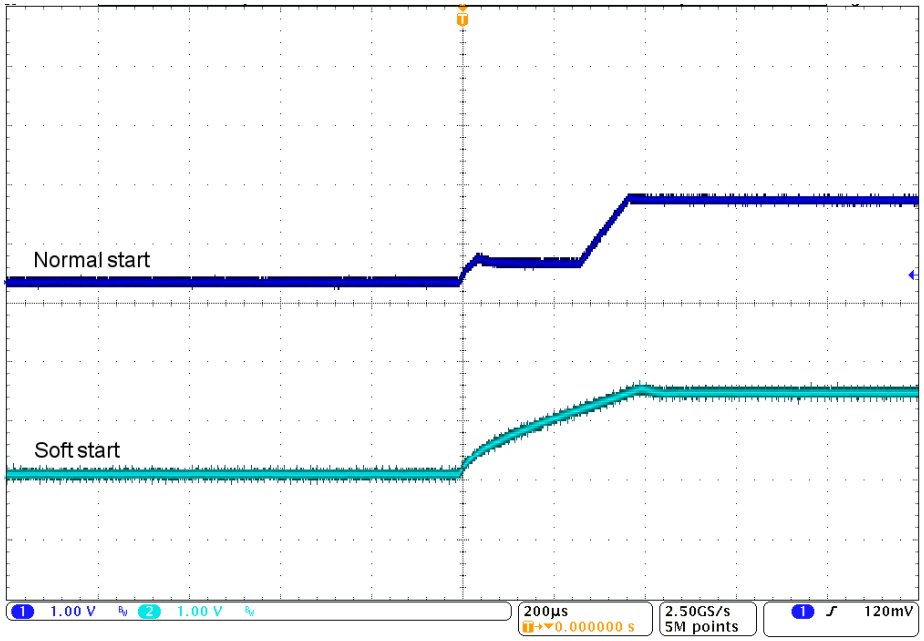

Figure 3: Buck Soft-Start and Normal Start

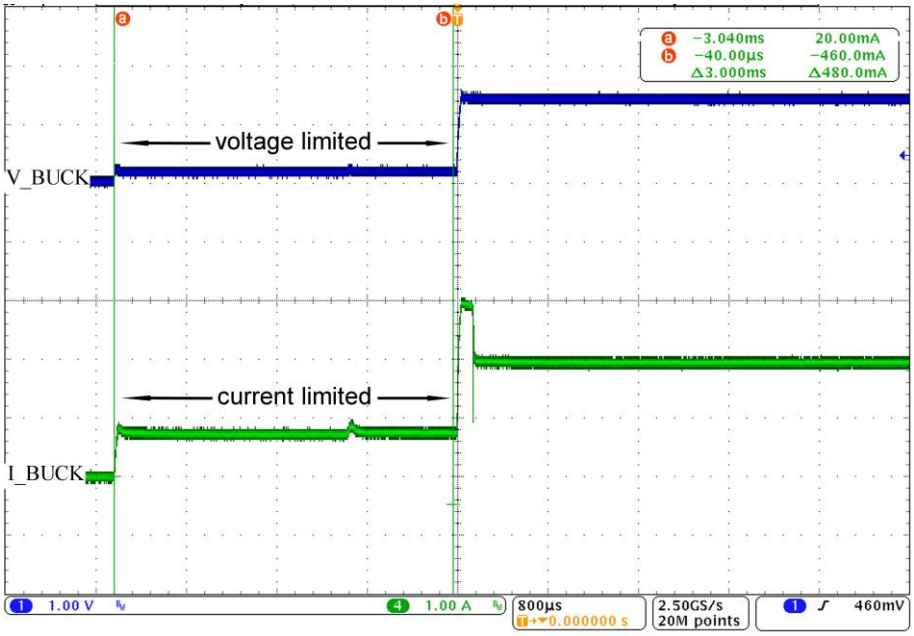

Figure 4: Buck Soft-Start with High Load

4.14 Buck Clock Control

Integrated PMICs are designed to have synchronous clocks. Dialog carefully designs its bucks with the ability to configure the clock polarity to minimize buck crosstalk and jitter. The DA9061/2 controls BUCK<x>_CLK_INV (register CONFIG_C) provide control of the buck clock phases. The recommended register setting of 0x1C is typically the optimum.

4.15 Buck Forced-Sync

It is sometimes desirable to force the buck operation into sync mode (PWM). This is typically done by setting BUCK<x>_MODE = Synchronous. However, when the output voltage is set below approximately 0.7 V, the bucks are designed to enter sleep mode (PFM) regardless of the

BUCK<x>_MODE setting. To ensure the buck is in sync mode at any output voltage and any load condition, the following configuration can be used:

- Set BUCK<x>_MODE = 0 (Controlled by BUCK<x>_SL_A and BUCK<x>_SL_B)
- Set BUCK<x>_SL_A = 0 (Force sync)
- Set BUCK<x>_SL_B = 0 (Force sync if B settings are selected, although in many configurations this control is not used)

Setting Buck4 into Forced-Sync Mode is necessary when using it for DDR termination, see Section 4.8.2.

4.16 RTC Tick Events

A periodic tick signal can be generated every second or minute by enabling TICK_ON. It is important that a write to register ALARM_Y is performed after modifying the associated registers TICK_TYPE or TICK_WAKE, otherwise the new values will be disregarded.

When using the tick feature in ultra-low power applications where there are no bucks with loads greater than 150 mA, please contact your Dialog support representative to discuss optimization of software interrupt handling.

4.17 32 kHz External Clock

When a 32 kHz clock is available from elsewhere in the system, a crystal oscillator is not required for DA9062 as the system signal may be applied to port XTAL_OUT. In this configuration, bit CRYSTAL should be cleared in register EN_32K. The signal is forwarded into the PMIC phase-inverted.

5 Application Information

The following sub-sections provide system architecture guidance.

5.1 Regulator Usage

The DA9061/2 regulators can be used for any purpose as long as they are operated in specification. Typically, their assignment will be dictated by their voltage and current operating windows. However, the following may be used as a starting-point when mapping DA9062 regulators to system requirements:

- Buck3 has a higher voltage range than other bucks. Therefore, it is often most suited for driving peripherals.
- Bucks 1, 2, and 4 have better load transient response than Buck3 at similar test conditions.
- Bucks 1 and 2 can be merged to give a 5 A supply. These are therefore optimized for supplying a processor core.
- Buck4 is optimized for VTT mode: it is capable of sinking as well as sourcing current.
- LDO1 is the only regulator that can provide an always-on supply. All other regulators turn off when the PMIC enters RESET mode.

Examples of mapping for systems based on the NXP® i.MX 6SoloLite™ and 6Dual™ processors are illustrated in Figure 5 and Figure 6. These are conceptual mappings only as they do not consider peripheral rail requirements, type of memory, and so on. In the 6Dual solution, Buck4 has been used to drive peripherals, but could readily be used as the VTT supply. Where one or more additional regulators are required, potential solutions include:

- Use a Dialog sub-PMIC. These components are designed as companion ICs to the DA9061/2. Software is simplified since the sub-PMIC can be configured as a slave and may not require an additional software driver.
- Move the design from DA9061 to DA9062, or from DA9062 to DA9063.
- Use an external discrete switching regulator or LDO (as implemented in Figure 6 as a VTT buck).

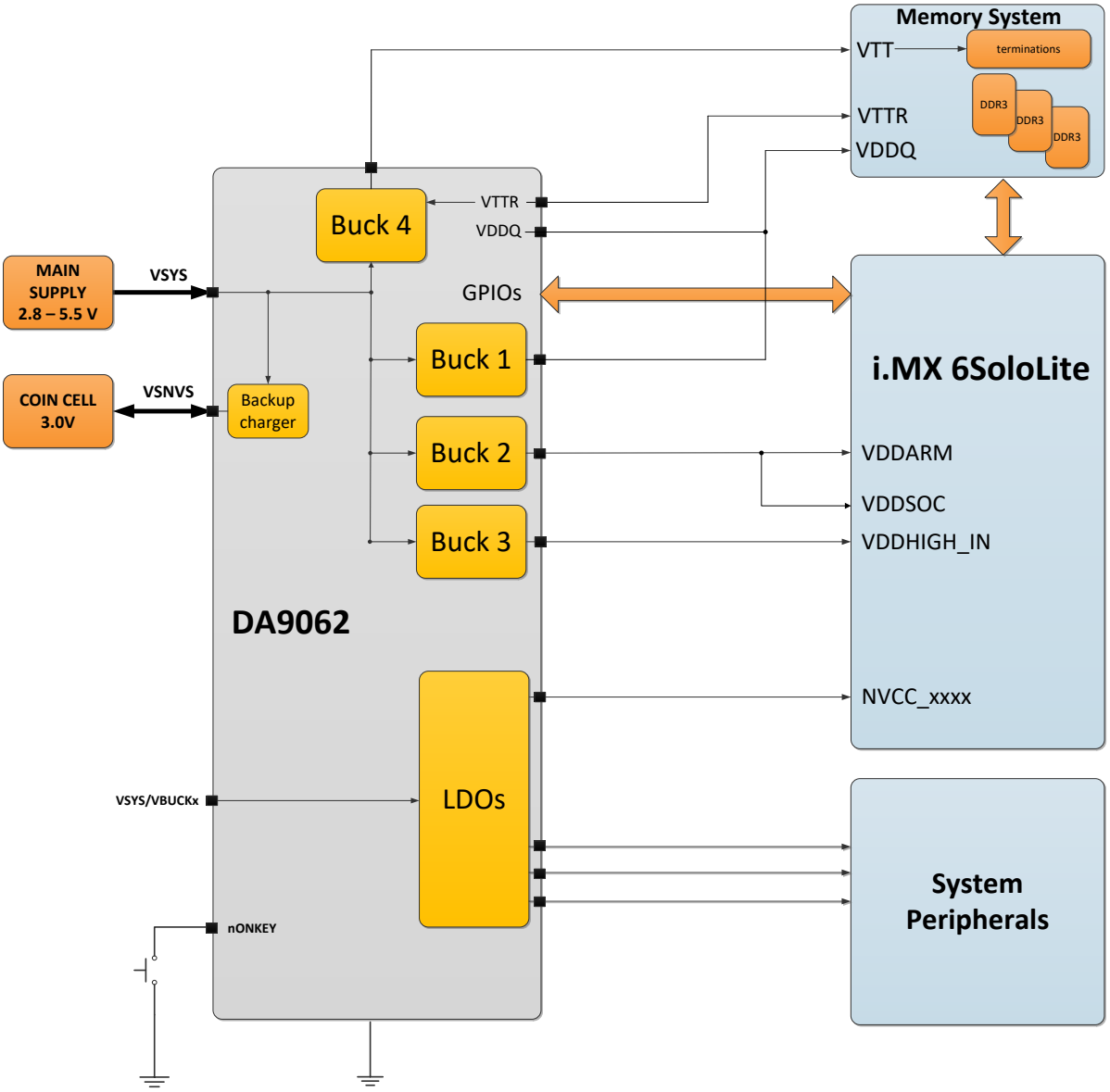

Figure 5: Conceptual Regulator Mapping for an i.MX 6SoloLite Processor Application

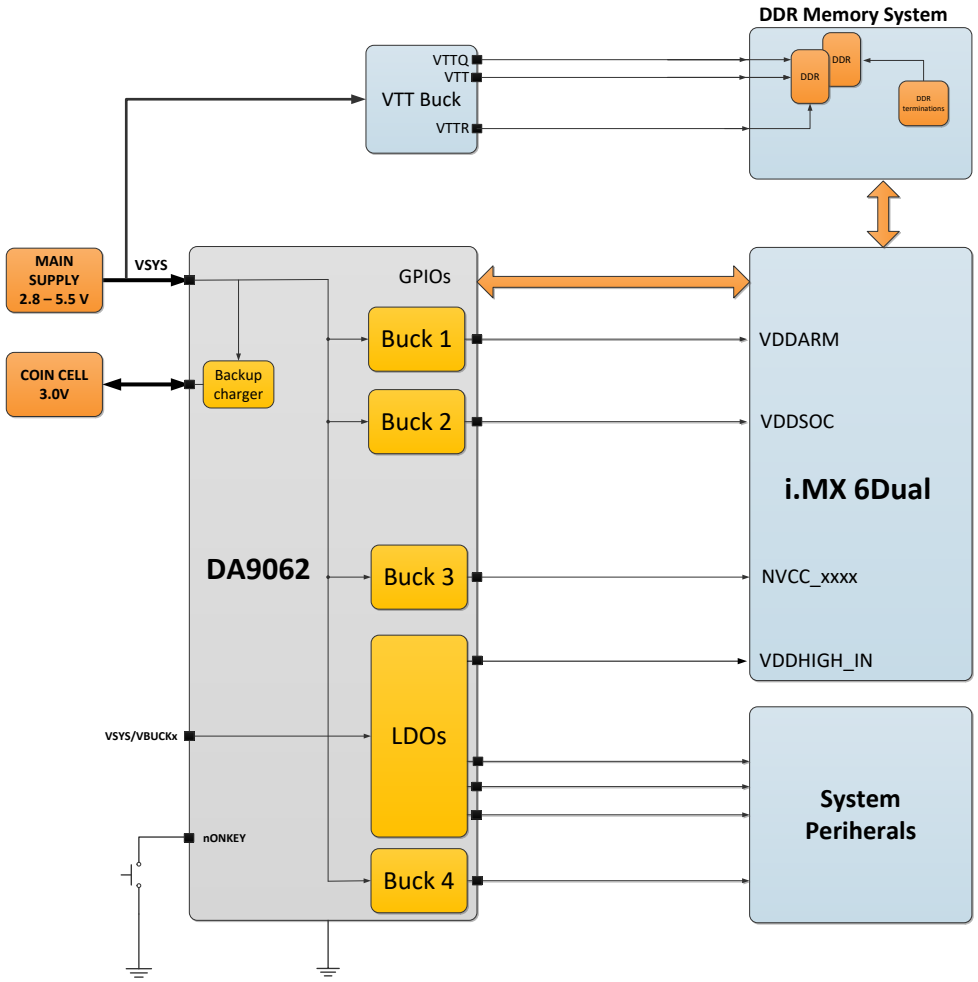

Figure 6: Conceptual Regulator Mapping for an i.MX 6Dual Processor Application

5.1.1 LDO Merging for Higher Load Capability

LDO outputs can be tied directly together to drive a rail demanding greater than the current capabilities of an individual LDO. This technique is best implemented when the supplies are sequenced since both can be placed in the same sequencer slot. Care should be taken to avoid having one LDO on and the other off, especially when the default pull-down configuration has not been changed. The internal pull-down resistors can be disabled via the LDOx_PD_DIS controls.

5.1.2 Regulator Output Capacitors

The datasheets include specifications for regulator output capacitors, C_{OUT}. The purpose of the maximum C_{OUT} values is to ensure that the specified turn-on time, t_{ON}, can be met. However, a system designer may wish to add additional rail capacitors to reduce voltage ripple or to improve transient load regulation. This is acceptable on the understanding that t_{ON} may exceed the datasheet specification, inrush current may increase and DVC slew rates may be affected.

5.1.3 Unused Pins

The following is best practice for unused pins of the DA9061/2:

- Unused GPIO pins configured in OTP as inputs should be driven to their inactive states
- Unused GPIO pins configured in OTP as outputs should be left floating
- If no crystal oscillator is used, XTAL_IN and XTAL_OUT should be tied to GND
- Unused bucks:

- VDD_BUCK<x> = GND
- VBUCK<x> = GND
- VLX_BUCK<x> floating
- Current limits set in software to minimum
- This configuration minimizes leakage from VSYS in case the buck is accidentally enabled in software.

- Unused LDOs: VDD_LDO<x> = GND; VLDO<x> floating
- VBBAT should include a small stabilization capacitor (for example 470 nF)

TP should be tied to ground. Ideally, it should be connected to ground via a 0 Ω link (the link's removal allows access to this pin for application debug purposes). A 100 kΩ pull-down resistor should instead be used if in-circuit programming is planned, see 'In-Circuit Programming of DA9061/2/3' [8].

5.1.4 nRESETREQ

Customers familiar with the DA9063 may wish to note that the DA9063 nSHUTDOWN pin has the same function as the DA9061/2 nRESETREQ.

Also, see 'DA9061/2/3 Configuration of nSHUTDOWN / nRESETREQ and nOFF' [3], which discusses appropriate external pull-up rails for this input.

5.2 Defining an OTP Configuration

At system start-up, much of the DA9061/2 configuration can be written via the I²C interface by the host processor. However, there are PMIC configuration registers that must be set correctly prior to the host starting up. These settings must be programmed into the PMIC OTP. This configurability is a feature of Dialog power management products that enables most applications to be supported.

Once the system regulator mapping is complete, the process to define the OTP configuration is generally:

1. Communicate project requirements with your Dialog support representative.
2. Begin with an appropriate standard Dialog ini file as the seed. These reference ini files are typically included with the SmartCanvas™ software and within the product evaluation kits.
3. Modify the configuration to suit the application. Development and testing is achieved using the Power Commander Mode feature (Section 5.3).
4. Review the draft OTP configuration ini file with your Dialog support representative.

In some cases it may be possible to use a standard configuration file without modification. Please discuss this with your Dialog support representative.

5.3 Power Commander Mode

This is a special mode for evaluation and configuration of Dialog PMICs. In Power Commander Mode, the DA9061/2 is configured to load the register values via the I²C interface instead of from the OTP cells. This allows unprogrammed DA9061/2 samples to power up and allows a PC running SmartCanvas software to load all the configuration registers.

Power Commander Mode is enabled by driving the TP pin to V_{SYS} prior to applying power to the PMIC.

After an initial start-up of the DA9061/2 with TP at V_{SYS}, the PMIC pauses at an intermediate state, indicating to the PC that it is waiting to receive the configuration data. The software running on the PC responds by uploading the appropriate values to the DA9061/2. A second transfer occurs when the PMIC is waking up and leaving the POWERDOWN state. This second transfer is limited to a subset of registers (VBUCK<x>_A and VLDO<x>_A, plus CONTROL_A and SEQ_TIMER). However, this transfer can be suppressed by clearing control OTPREAD_EN. Additionally, the transfer of the SYSTEM_EN bit can individually be suppressed by setting bit SYSEM_EN_RD in the CONFIG_D register.

A practical guide to using Power Commander Mode is included in the User Manual of the DA9061/2 PowerCommander software (via the Help menu).

One of the few limitations is that Power Commander Mode cannot be used to evaluate sequencer timings, as they are affected by the USB communication speed to the PC. Sequencer timings can be verified using a programmed device.

6 PCB Layout

The DA9061/2, supplied in a QFN package, is compatible with low-cost PCB technology such as Type-II two-layer boards. Note that reliable system performance relies on good PMIC layout practice, as discussed in 'PCB Layout Guidelines' [6] and in the following sections.

6.1 General DA9061/2 Recommendations

- Appropriate trace width and a sufficient number of vias should be used for all power supply paths.
- Too high trace resistances can prevent the system from achieving the best performance. For example, the efficiency and the current ratings of buck converters might be degraded. Furthermore, the PCB may be exposed to thermal hot spots, which can lead to critical overheating due to the positive temperature coefficient of copper.
- Traces for high current pins should be connected with the same width as the pads and should become wider as soon as possible. (Corner pins can be connected from the side using a trace the same length as the pad.)
- It is important to take note of the datasheet guidance relating to the quiet board region required for VREF, IREF, and the crystal oscillator. Note that the ground connections of the associated components are connected not only to the VSS_ANA pin of the DA9061/2 but also to the main PMIC ground using a narrow trace. This connection must not be omitted.
- Generally, all power traces with discontinuous high currents should be kept as short as possible.
- Noise-sensitive analog signals such as buck feedback lines or crystal connections should be kept away from traces carrying pulsed analog or digital signals. This can be achieved by separation (distance) or shielding with quiet signals or ground traces.

6.2 LDOs and Buck Convertors

- The placement of the distributed capacitors on the VSYS rail must ensure that all VDD inputs – and especially to the VSYS pin, the buck converters, and LDOs – are connected to a bypass capacitor close to the pads.
- Using a local power plane underneath the chip for V_{SYS} might be considered.
- Transient current loops in the area of the buck converters should be minimized.
- Care must be taken with trace routing to ensure that no current is carried on buck feedback lines (VBUCK<x>).
- The inductor placement is less critical since parasitic inductances have negligible effect.

6.3 LDO Remote Capacitors

LDOs require a stabilization capacitor, as defined in the datasheet specification. By default, the capacitors should be placed as close as possible to the PMIC. They can also be placed remotely from the DA9061/2, but the following should be considered:

- The voltage drop (load current * parasitic trace impedance) must be considered when configuring the LDO output voltage.
- Transient load regulation will also be affected by the trace impedance between the PMIC and the load.

This topic is also discussed in PCB Layout Guidelines [6].

6.4 Thermal Connection and Solder Stencil

The DA9061/2 QFN package provides a central thermal pad area which is to be soldered to the PCB main ground pad. This PCB pad must be connected with as many vias and as direct as possible to the PCB's main ground plane in order to achieve good thermal performance.

Careful solder stencil design is required to avoid problems such as the package floating on top of excess solder and causing open circuit pins. A slotted stencil pattern, or similar, should be used.

6.5 Reference Layouts

The Applications Information sections of the DA9061/2 datasheets [1], [2] illustrate the principals of fan-out for the PMIC and associated external passive components. Reference layout source files are available from Dialog for a six-layer (232-03-B.pcb) board and two-layer (232-16-A.pcb, Figure 7) board.

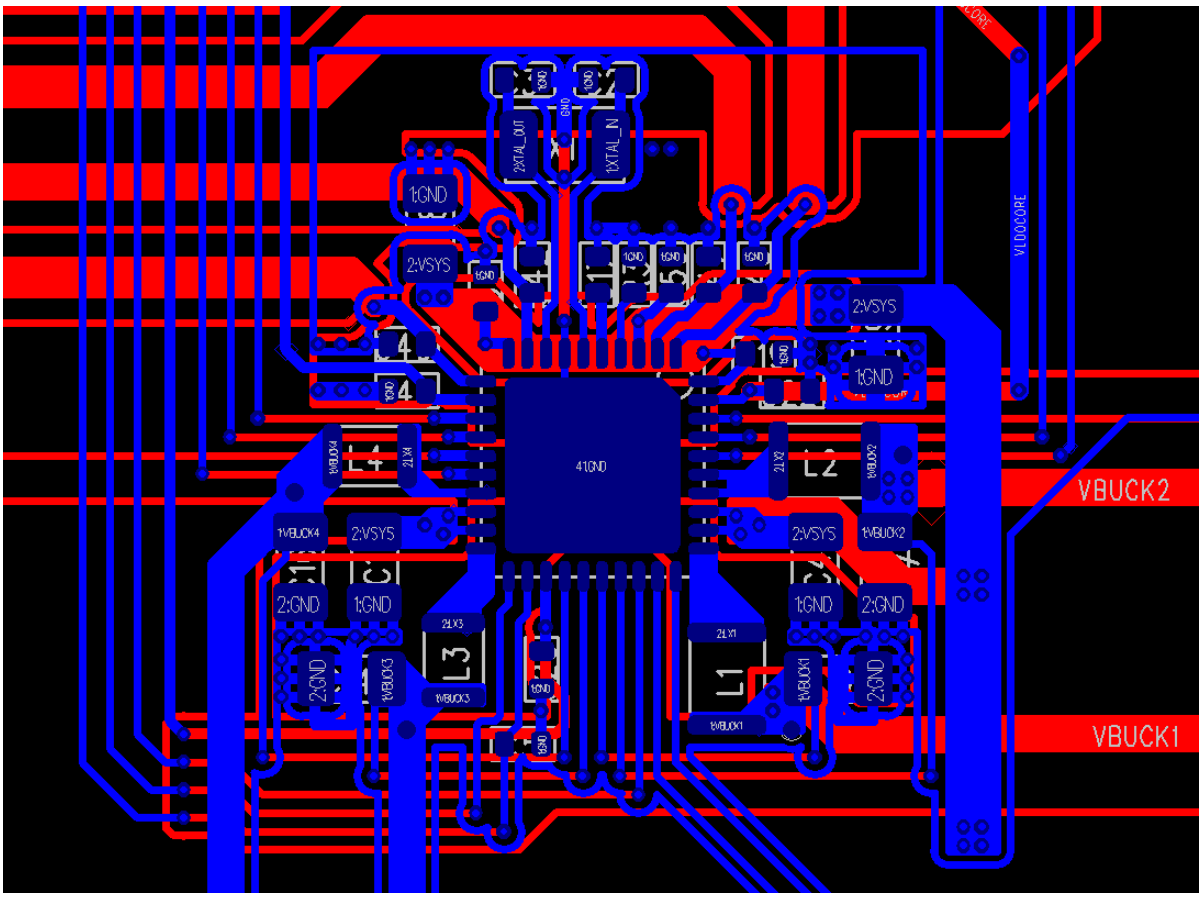

Figure 7: DA9062 on a Two-Layer Board Adhering to AN-PM-010 Layout Guidelines

7 Definitions

The following definitions are provided to assist with thermal design and interpretation of the datasheet test conditions.

7.1 Power Dissipation and Thermal Design

When designing with the DA9061/2, consideration must be given to power dissipation as the level of integration of the device can result in high power when all functions are operating with high battery voltages. Exceeding the package power dissipation capabilities results in the internal thermal sensor shutting down the device until it has sufficiently cooled. The package includes a thermal management pad to improve heat spreading into the PCB, see Section 6.4.

7.1.1 LDO Regulators

Linear regulators operating with a high current and high differential voltage between input and output dissipate the following power:

$$P_{diss} = (V_{in} - V_{out}) * I_{out}$$

Example: a regulator supplying 150 mA at 2.8 V from a fully charged lithium battery (VDD = 4.1 V):

$$P_{diss} = (4.1\,V - 2.8\,V) * 0.15\,A = 195\,mW$$

7.1.2 Buck Regulators

With,

$$P_{out} = P_{in} * Efficiency$$

it follows,

$$P_{diss} = P_{in} - P_{out}$$

$$P_{diss} = \frac{P_{out}}{Efficiency} - P_{out}$$

$$P_{diss} = P_{out} * \left(\frac{1}{Efficiency} - 1\right)$$

$$P_{diss} = I_{out} * V_{out} * \left(\frac{1}{Efficiency} - 1\right)$$

Example: an 85 % efficient buck converter supplying 1.2 V at 400 mA:

$$P_{diss} = 1.2\,V * 0.4\,A * \left(\frac{1}{0.85} - 1\right) = 85\,mW$$

Since the DA9061/2 has multiple regulators, each supply must be separately considered and their powers summed to give the total device dissipation. (Current drawn from the reference and control circuitry can be considered negligible in these calculations.) This provides a worst-case PMIC dissipation figure as the measurements and calculations do not differentiate between the losses in the device and the losses in the PCB traces, inductors and output capacitors.

7.2 Regulator Parameter – Dropout Voltage

In the DA9061/2, a regulator's dropout voltage is defined as the minimum voltage differential between the input and output voltages while regulation still takes place. Within the regulator, voltage control takes place across a PMOS pass transistor and, when entering the dropout condition, the transistor is fully turned on and therefore cannot provide any further voltage control. When the transistor is fully turned on, the output voltage tracks the input voltage and regulation ceases. As the DA9061/2 is based on CMOS technology and uses a PMOS pass transistor, the dropout voltage is directly related to the on-resistance of the pass transistor. The pass transistors are sized to provide the optimum balance between required performance and silicon area. By employing a 0.25 µm

process, Dialog is able to achieve very small pass transistor sizes for superior performance. The dropout voltage is defined as:

$$V_{dropout} = V_{in} - V_{out} = R_{dson} * I_{out}$$

When defining dropout voltage, it is specified in relation to a minimum acceptable change in output voltage. For example, all Dialog regulators have dropout voltage defined as the point at which the output voltage drops 10 mV below the output voltage at the minimum guaranteed operating voltage. The worst-case conditions for dropout are high temperature (highest on-resistance for the PMOS pass device) and maximum current load.

7.3 Regulator Parameter – Power Supply Rejection Ratio

The Power Supply Rejection Ratio (PSRR) is especially important in the supplies to RF and audio circuits. In a TDMA phone system such as GSM, the 217 Hz transmit burst from the power amplifier results in significant current pulses being drawn from the battery. These can peak at up to 2 A before reaching a steady state of 1.4 A. Due to the battery having a finite internal resistance (typically 0.5 Ω), these current peaks induce ripple on the battery voltage of up to 500 mV. Since the supplies to the audio and RF are derived from this supply, it is essential that this ripple is removed otherwise it would show as a 217 Hz tone in the audio and could also affect the transmit signal. Power supply rejection should always be specified under worst-case conditions – when the battery is at its minimum operating voltage and when there is minimum headroom available due to dropout.

7.4 Regulator Parameter – Line Regulation

Static line regulation is a measurement that indicates a change in the regulator output voltage, ΔV_{reg} (regulator operating with a constant load current), in response to a change in the input voltage, ΔV_{in}. Transient line regulation is a measurement of the peak change, ΔV_{reg}, in regulated voltage seen when the line input voltage changes.

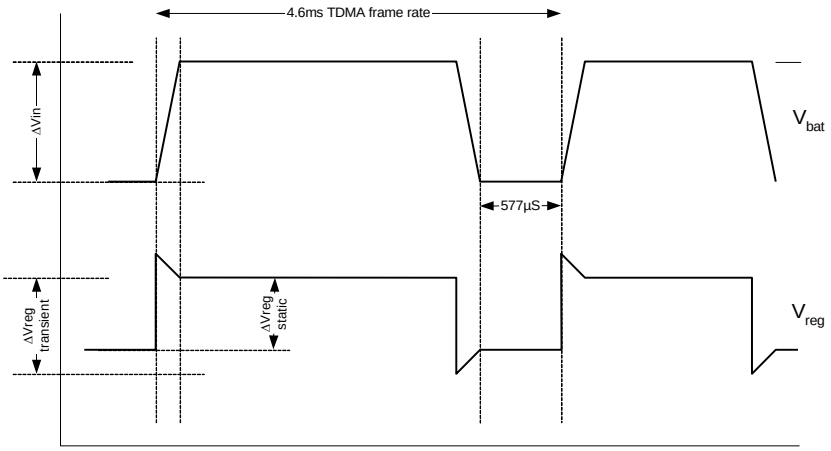

Figure 8: Line Regulation

7.5 Regulator parameter – Load Regulation

Static load regulation is a measurement that indicates a change in the regulator output voltage, ΔV_{reg}, in response to a change in the regulator loading, ΔI_{load}, while the regulator input voltage remains constant. Transient load regulation is a measurement of the peak change in regulated voltage, ΔV_{reg}, seen when the regulator load changes.

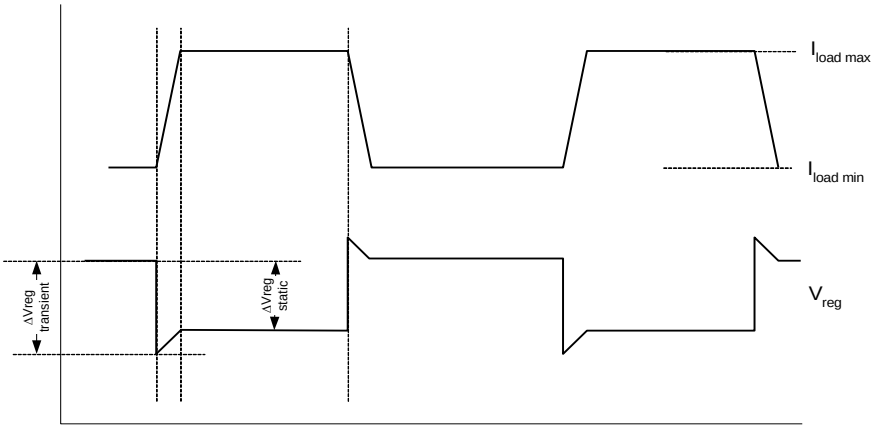

Figure 9: Load regulation

8 Conclusions

The guidance in this application note equips developers to design reliable systems based on Dialog DA9061/2 power management solutions.

Revision History

Revision	Date	Description
1.4	12-Sep-2018	
Change details: ● Removed repeated and incorrect LDO<x>_GPI column from Table 2: LDO Regulator Configuration Guide ● Reworded the text and figure of section 4.4 'VDD_START Faults and VDD_WARN' to improve clarity.		
1.3	30-May-2018	
Change details: ● Added Section 4.2.3 Masking the Domain Register Bits ● Added Section 4.6 LDO Default Supplies and Always-On Regulator and Section 4.7 Buck Default Supplies ● Changed the recommended settings in Section 4.8.2 VTT Mode for DDR Termination		
1.2	23-Mar-2017	
Change details: ● Expanded section on VDD_START ● Added section on buck Forced-Sync mode ● Added Force-Sync mode requirement to section discussing Buck VTT ● Mode operation ● Minor typographical improvements ● File regenerated on 11-May-2017 due to incorrect title page and header ● File regenerated on 22-May-2017 to correct and clarify cross references.		
1.1	22-Oct-2015	
Change details: ● Expanded section on buck soft start ● Added section on RTC tick		
1.0	06-Oct-2015	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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