Application Note

DA9061 / AtlasVI Power Connections

AN-PM-082

Abstract

This document describes the connectivity between the Dialog DA9061 Power Management Integrated Circuit (PMIC) and Qualcomm AtlasVI™ system processor.

Contents

Figures

Tables

1 Terms and Definitions

GUI	Graphical User Interface
AtlasVI	Qualcomm SoC, formally known as CSR SiRFatlasVI™
SoC	System on a Chip
PMIC	Power Management Integrated Circuit

2 References

[1] DA9061, Datasheet, Dialog Semiconductor

[2] SiRFatlasVI, http://www.csr.com/products/148/sirfatlasvi [Accessed 14-Jul-2016]

[3] DA9062, Datasheet, Dialog Semiconductor

[4] The Linux Kernel Archives, https://kernel.org/ [Accessed 13-Sep-2016]

3 Introduction

This document provides details of integrating the DA9061 with the AtlasVI SoC [2], suitable for low-end and mid-range infotainment applications. For high-end applications, integration of Dialog DA9062 [3] and Atlas7™ is recommended.

4 System Block Diagram

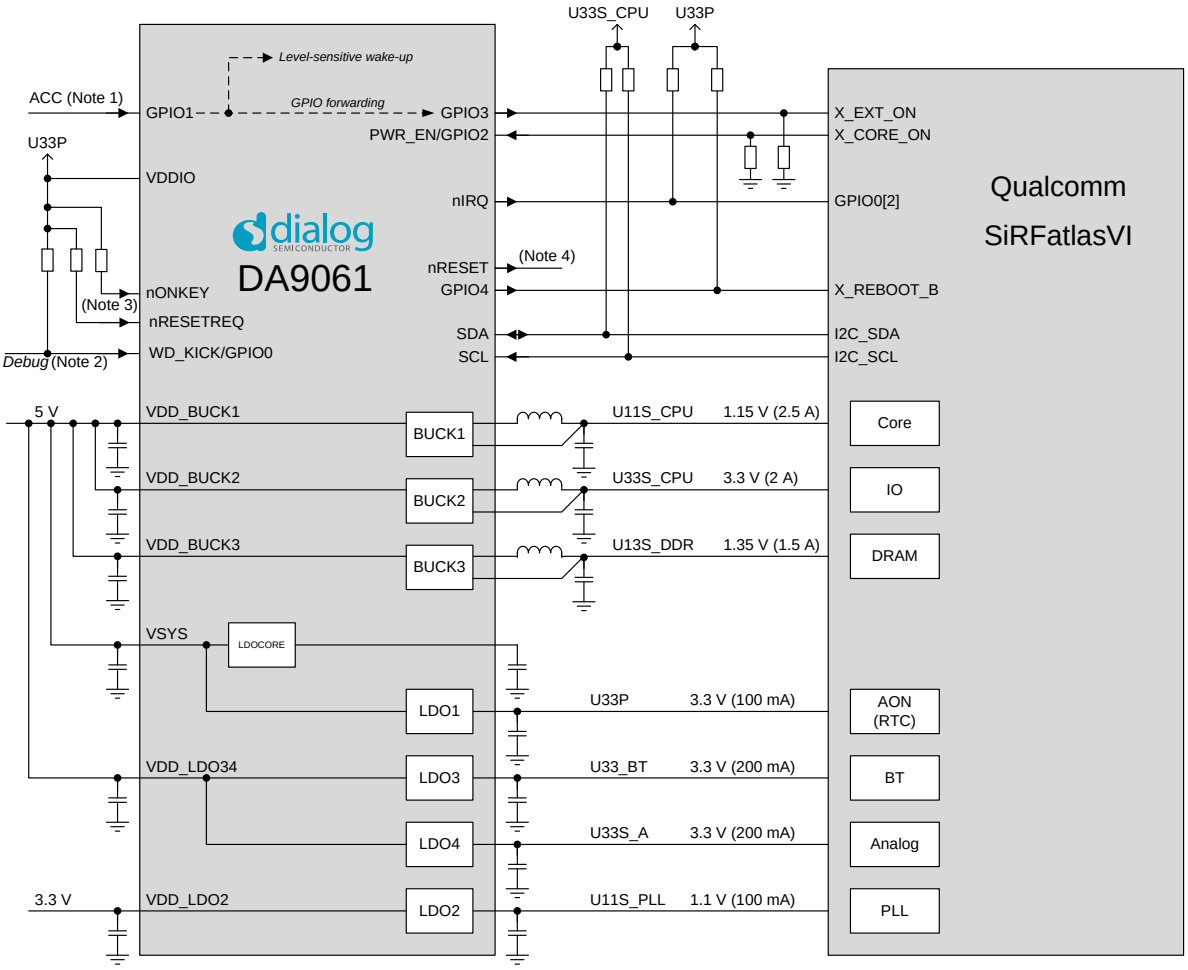

Figure 1: DA9061 to AtlasVI Mapping

Note 1 The ACC GPIO1 signal is to be derived from the 12 V ACC (automotive) accessory line.

Note 2 The WD_KICK/GPIO0 input requires a pulse every 2 s (as set by register control TWDSCALE). Alternatively, the input can be permanently asserted using the pull-up shown. This may be useful during application debugging.

Note 3 nONKEY is not used. System start-up is initiated by ACC / GPIO1.

Note 4 nRESET is not used.

Table 1: GPIO Mapping for AtlasVI

GPIO	Function	Description
GPIO0	WD_KICK	Watchdog kick/disable
GPIO1	GPI	ACC in (derived from the 12 V ACC accessory line)
GPIO2	PWR_EN	Power enable
GPIO3	GPO push-pull (forwarded from GPIO1)	ACC out
GPIO4	GPO push-pull	Core reset for AtlasVI, controlled by the sequencer

5 Timing Diagrams

The numbered notes below each figure correspond to the numbered events within the figure.

5.1 Cold Boot

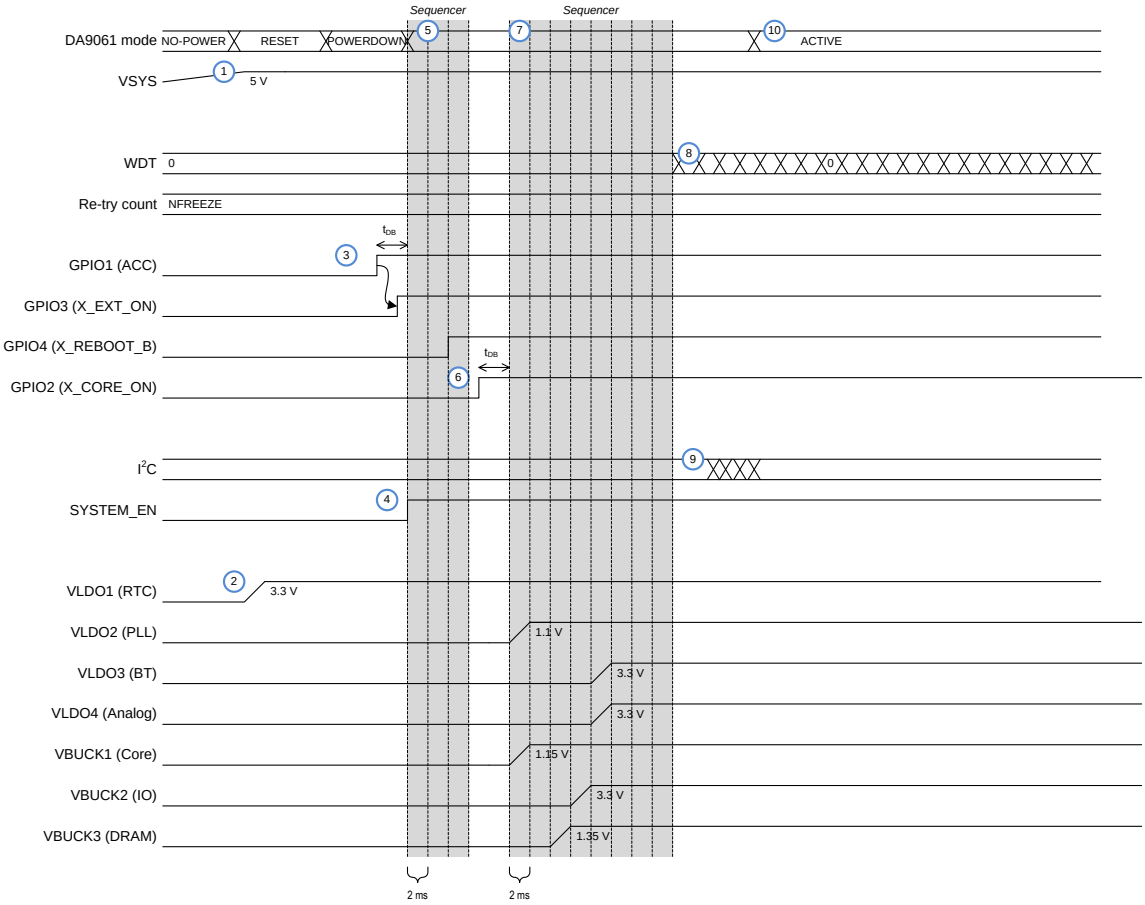

Figure 2: Timing Diagram for Cold Boot

1. The system supply rises above a threshold value after which the internal supplies of DA9061 are enabled and the device enters the RESET mode and then automatically proceeds to the POWERDOWN mode.
2. The always-on supply LDO1 is enabled in the RESET mode.
3. GPIO1 (ACC) is asserted (level-sensitive signal) which triggers a power-up sequence, and the signal is also forwarded to GPIO3 (X_EXT_ON). The delay between the rising edge of the GPIO1 (ACC) and the sequence starting is defined by the debouncing time t_{DB}.
4. A partial OTP read is executed at the beginning of the power-up sequence which asserts control SYSTEM_EN.
5. DA9061 executes the first part of the power-up sequence during which GPIO4 (X_REBOOT_B) is de-asserted.
6. AtlasVI asserts the X_CORE_ON signal which triggers the second part of the power-up sequence. The delay between the rising edge of the GPIO2/PWR_EN (X_CORE_ON) and the sequence starting is defined by the de-bouncing time t_{DB}.
7. DA9061 executes the second part of the power-up sequence during which the supplies are enabled in the programmed order. The time between the sequencer steps is 2 ms.
8. The watchdog starts running when the power-up sequence completes.
9. AtlasVI software performs the first watchdog kick through I^2C.
10. DA9061 enters the ACTIVE mode.

5.2 Power-Down

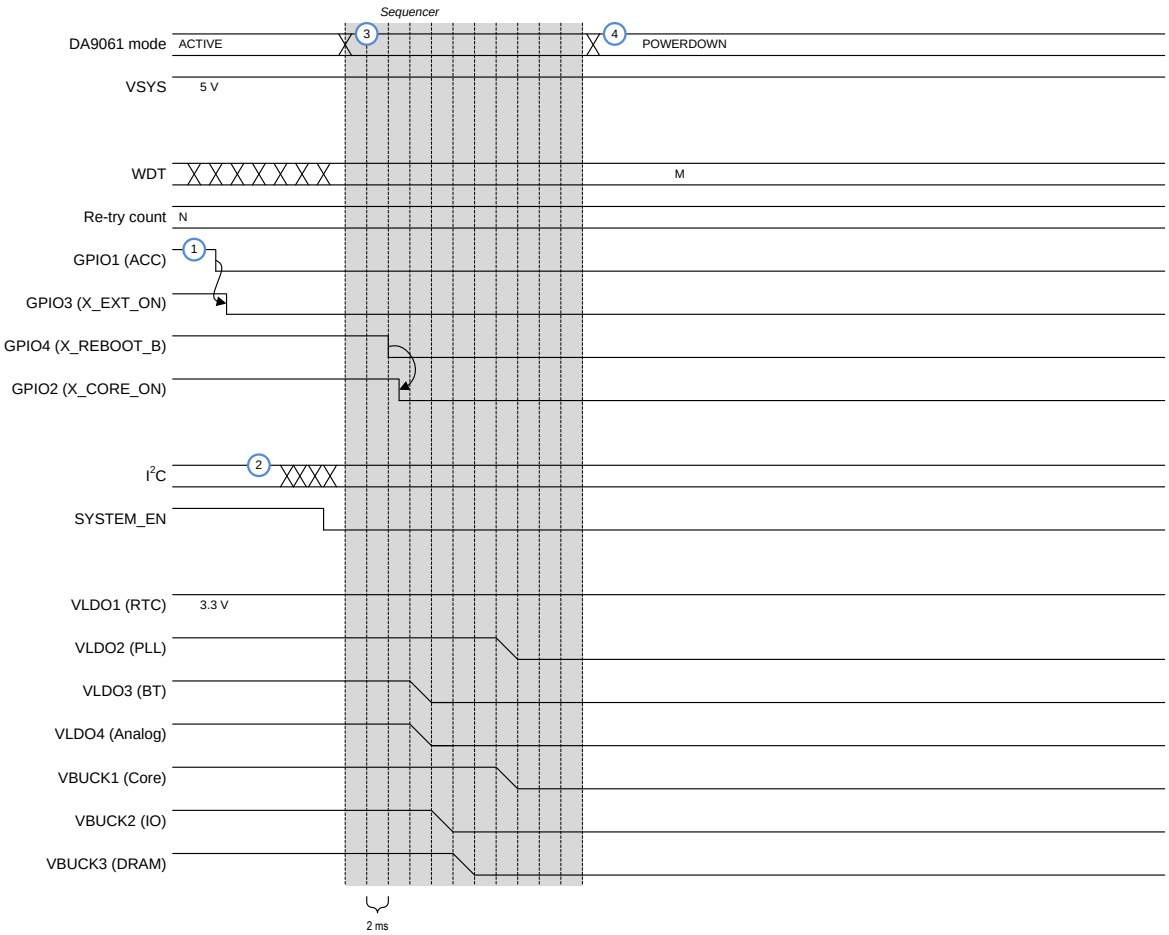

Figure 3: Timing Diagram for Power-Down

1. GPIO1 (ACC) is de-asserted and the signal is forwarded to GPIO3 (X_EXT_ON).
2. AtlasVI software sees the de-asserted X_EXT_ON and performs necessary preparations for power-down and then de-asserts control SYSTEM_EN through I^2C.
3. DA9061 executes the power-down sequence during which GPIO4 (X_REBOOT_B) is asserted and supplies are disabled in the reverse order. X_CORE_ON is de-asserted asynchronously when GPIO4 (X_REBOOT_B) is asserted. The time between the sequencer steps is 2 ms, because the power-down was triggered by de-asserting control SYSTEM_EN, the sequencer proceeds directly to the POWERDOWN mode.
4. DA9061 completes the power-down sequence and enters the POWERDOWN mode. The watchdog is not counting in POWERDOWN mode.

5.3 Power-Up

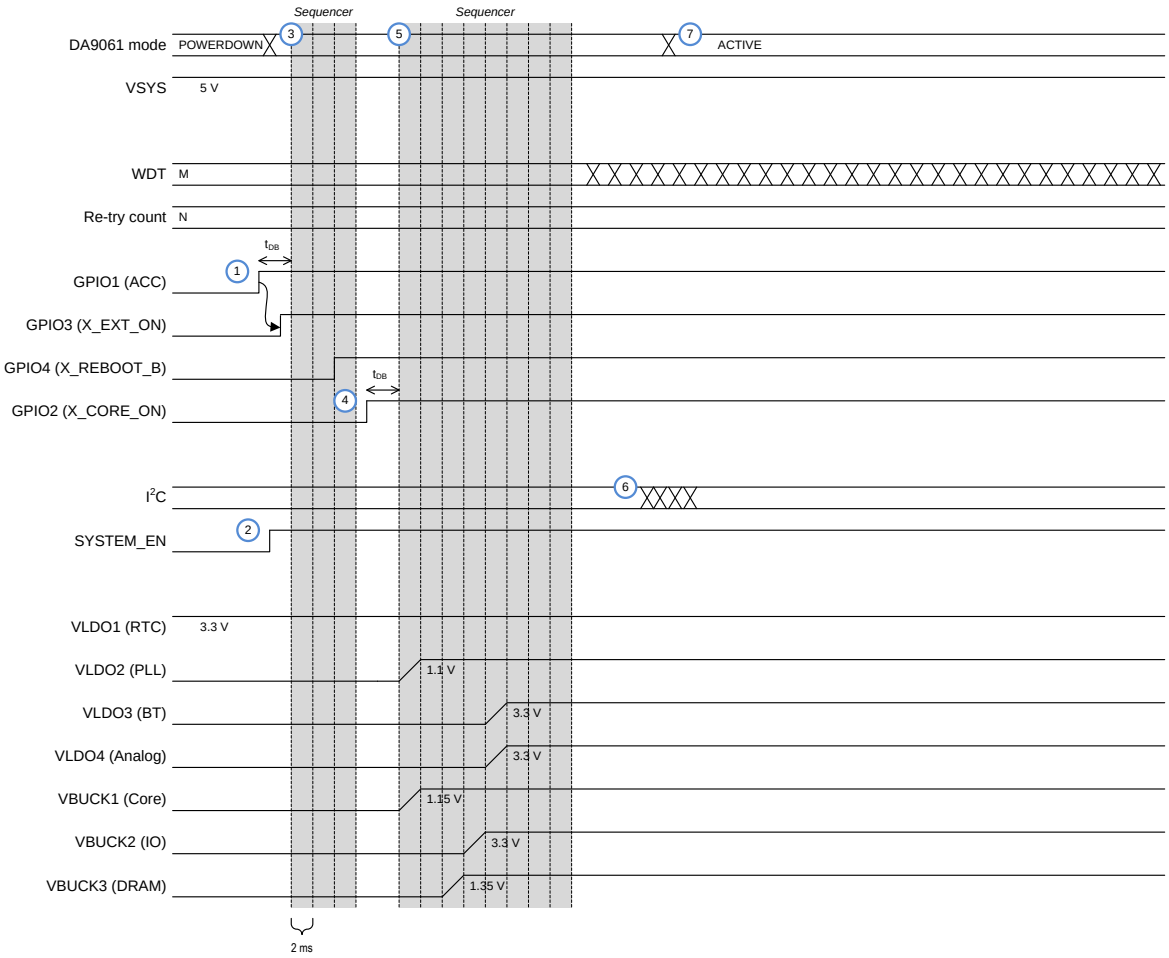

Figure 4: Timing Diagram for Power-Up

1. GPIO1 (ACC) is asserted (level-sensitive signal) which triggers a power-up sequence, and the signal is also forwarded to GPIO3 (X_EXT_ON). The delay between the rising edge of the GPIO1 (ACC) and the sequence starting is defined by the de-bouncing time t_{DB}.
2. A partial OTP read is executed at the beginning of the power-up sequence which asserts control SYSTEM_EN.
3. DA9061 executes the first part of the power-up sequence during which GPIO4 (X_REBOOT_B) is de-asserted.
4. AtlasVI asserts the X_CORE_ON signal which triggers the second part of the power-up sequence. The delay between the rising edge of the PWR_EN (X_CORE_ON) and the sequence starting is defined by the de-bouncing time t_{DB}.
5. DA9061 executes the second part of the power-up sequence during which the supplies are enabled in the programmed order. The timing between the sequencer steps is 2 ms.
6. AtlasVI software performs the first watchdog kick through I^2C.
7. DA9061 enters the ACTIVE mode.

5.4 Software Initiated Power-Down

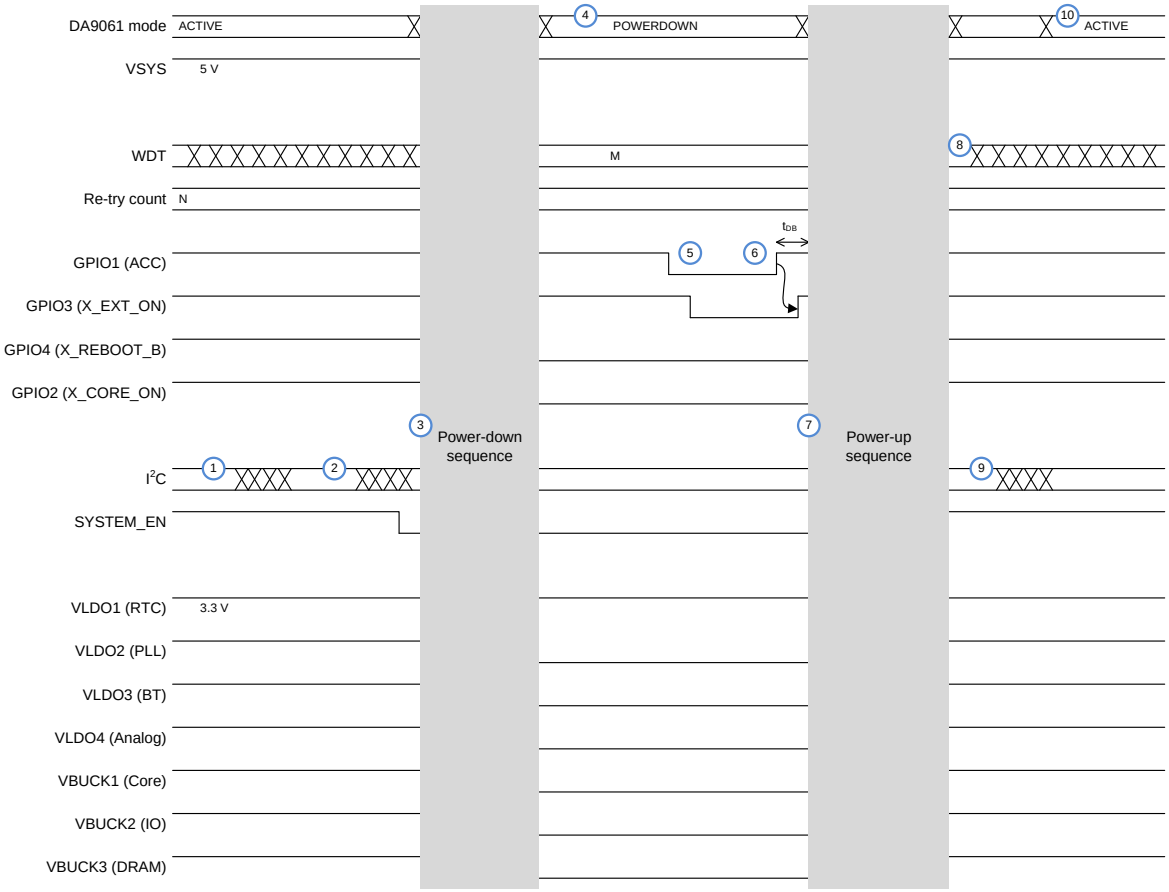

Figure 5: Timing Diagram for a Software Initiated Power-Down

1. AtlasVI software re-configures GPIO1 from level sensitive to edge sensitive.
2. AtlasVI software performs necessary preparations for a power-down and then de-asserts control SYSTEM_EN through I^2C.
3. DA9061 executes the power-down sequence as described in Section 5.2.
4. DA9061 completes the power-down sequence and enters the POWERDOWN mode. The watchdog is not counting in POWERDOWN mode. Because GPIO1 (ACC) was re-configured as edge sensitive a power-up sequence is not triggered by the GPIO1 (ACC) level.
5. GPIO1 (ACC) is de-asserted.
6. GPIO1 (ACC) is asserted and the detected rising edge triggers a power-up sequence. The signal is also forwarded to GPIO3 (X_EXT_ON).
7. DA9061 executes the power-up sequence as described in Section 5.3. During the power-up sequence, an OTP read is executed that restores the GPIO1 (ACC) setting as level sensitive.
8. DA9061 completes the power-up sequence and the watchdog continues running.
9. AtlasVI software performs a watchdog kick through I^2C.
10. DA9061 enters the ACTIVE mode.

5.5 Watchdog Reset (No Freeze)

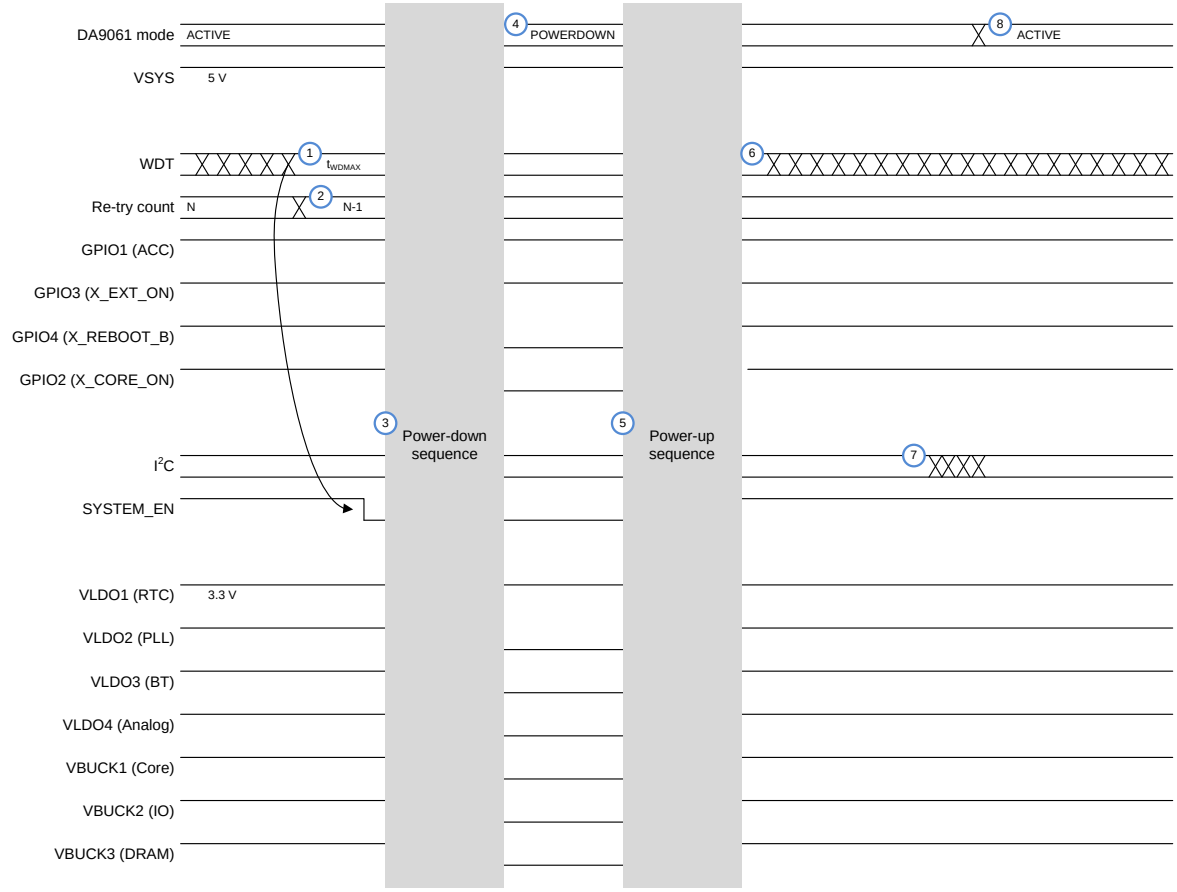

Figure 6: Timing Diagram for Watchdog Reset

1. The watchdog timer reaches its maximum value causing a watchdog error. This de-asserts control SYSTEM_EN which triggers a power-down sequence.
2. The re-try counter is decremented as a result of the watchdog error.
3. The sequencer executes the power-down sequence as described in Section 5.2
4. The power-down sequence is completed and DA9061 enters the POWERDOWN mode but because GPIO1 (ACC) remains asserted a new power-up sequence is immediately triggered.
5. DA9061 executes the power-up sequence as described in Section 5.3.
6. DA9061 completes the power-up sequence and the watchdog continues running.
7. AtlasVI software performs a watchdog kick through I^2C.
8. DA9061 enters the ACTIVE mode.

5.6 Watchdog Reset (With Freeze)

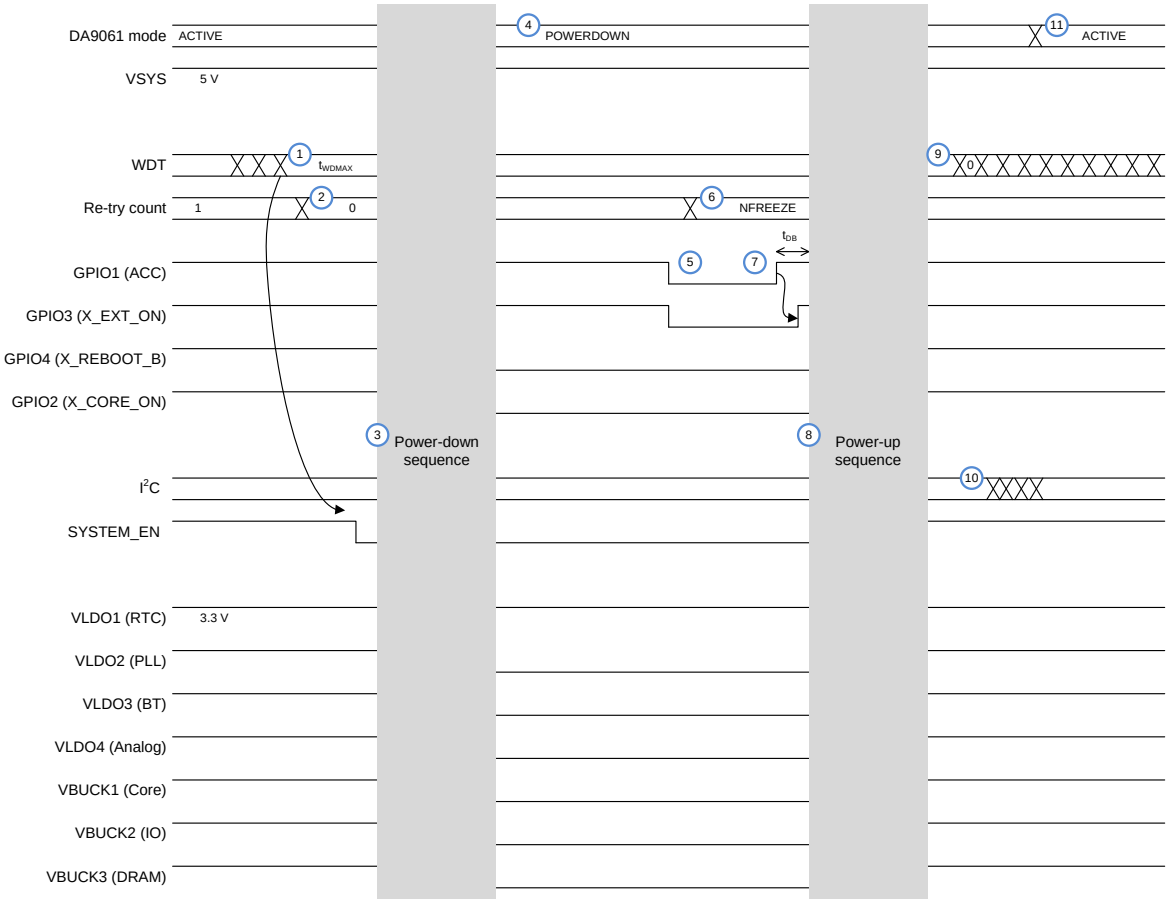

Figure 7: Timing Diagram for Watchdog Reset Causing a Freeze

1. The watchdog timer reaches its maximum value causing a watchdog error. This de-asserts control SYSTEM_EN which triggers a power-down sequence.
2. The re-try counter is decremented as a result of the watchdog error. This time, the re-try count reaches zero which causes the freeze function to be activated.
3. The sequencer executes the power-down sequence as described in Section 5.2.
4. The power-down sequence is completed and DA9061 enters the POWERDOWN mode. Because the freeze function is active, a power-up sequence is not triggered even though ACC remains asserted.
5. GPIO1 (ACC) is de-asserted.
6. As a result of the de-asserted level sensitive wakeup, the re-try counter is reset and the freeze function is de-activated.
7. GPIO1 (ACC) is re-asserted which triggers a power-up sequence, and the signal is also forwarded to GPIO3 (X_EXT_ON). The delay between the rising edge of the GPIO1 (ACC) and the sequence starting is defined by the de-bouncing time t_{DB}.
8. DA9061 executes the power-up sequence as described in Section 5.3.
9. DA9061 completes the power-up sequence and the watchdog continues running.
10. AtlasVI software performs a watchdog kick through I^2C.
11. DA9061 enters the ACTIVE mode.

5.7 Temperature Warning and Temperature Error

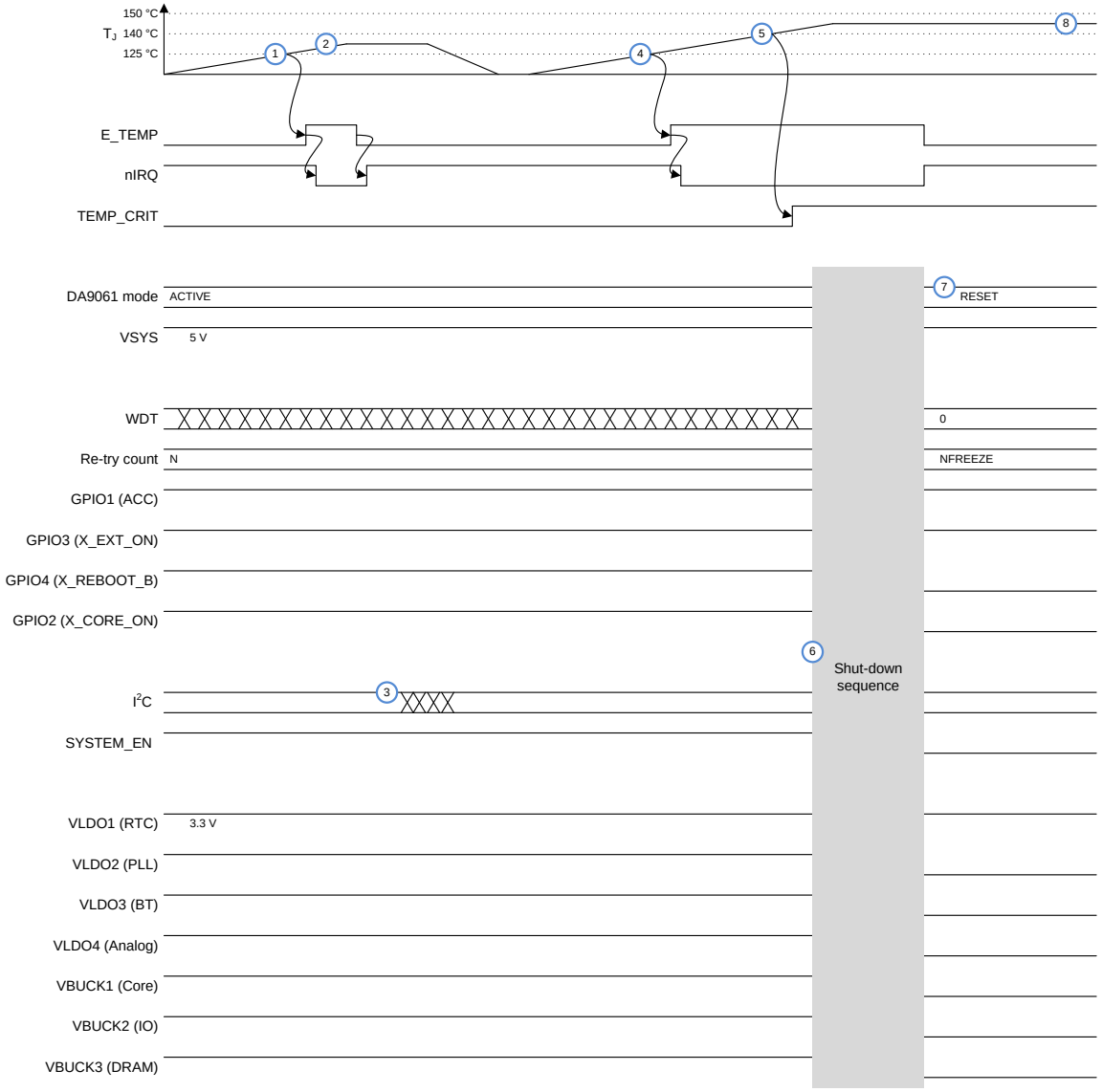

Figure 8: Timing Diagram for Temperature Warning and Temperature Error

1. The die temperature exceeds T_{WARN} which causes the event E_TEMP to be asserted. The event, if not masked, asserts nIRQ.
2. AtlasVI software sees the temperature warning and reduces the activity of the platform.
3. AtlasVI software clears the event E_TEMP. If no other events are active, this de-asserts nIRQ.
4. The die temperature exceeds T_{WARN} again which causes the event E_TEMP to be asserted. The event, if not masked, asserts nIRQ.
5. The die temperature exceeds T_{CRIT} which causes the temperature error flag TEMP_CRIT to be asserted, and a shut-down sequence is triggered.
6. DA9061 executes the shut-down sequence which is the same as the power-down sequence described in Section 5.2, but a shut-down sequence triggered by a temperature error proceeds straight to the RESET mode.
7. DA9061 completes the shut-down sequence and enters the RESET mode. The re-try count is reset, but the temperature error flag is not reset.
8. DA9061 stays in RESET mode as long as the die temperature stays above T_{CRIT}. After this, the power-up sequence is executed in the same way as in the cold boot use case described in Section 5.1.

5.8 Temperature Power-On Reset

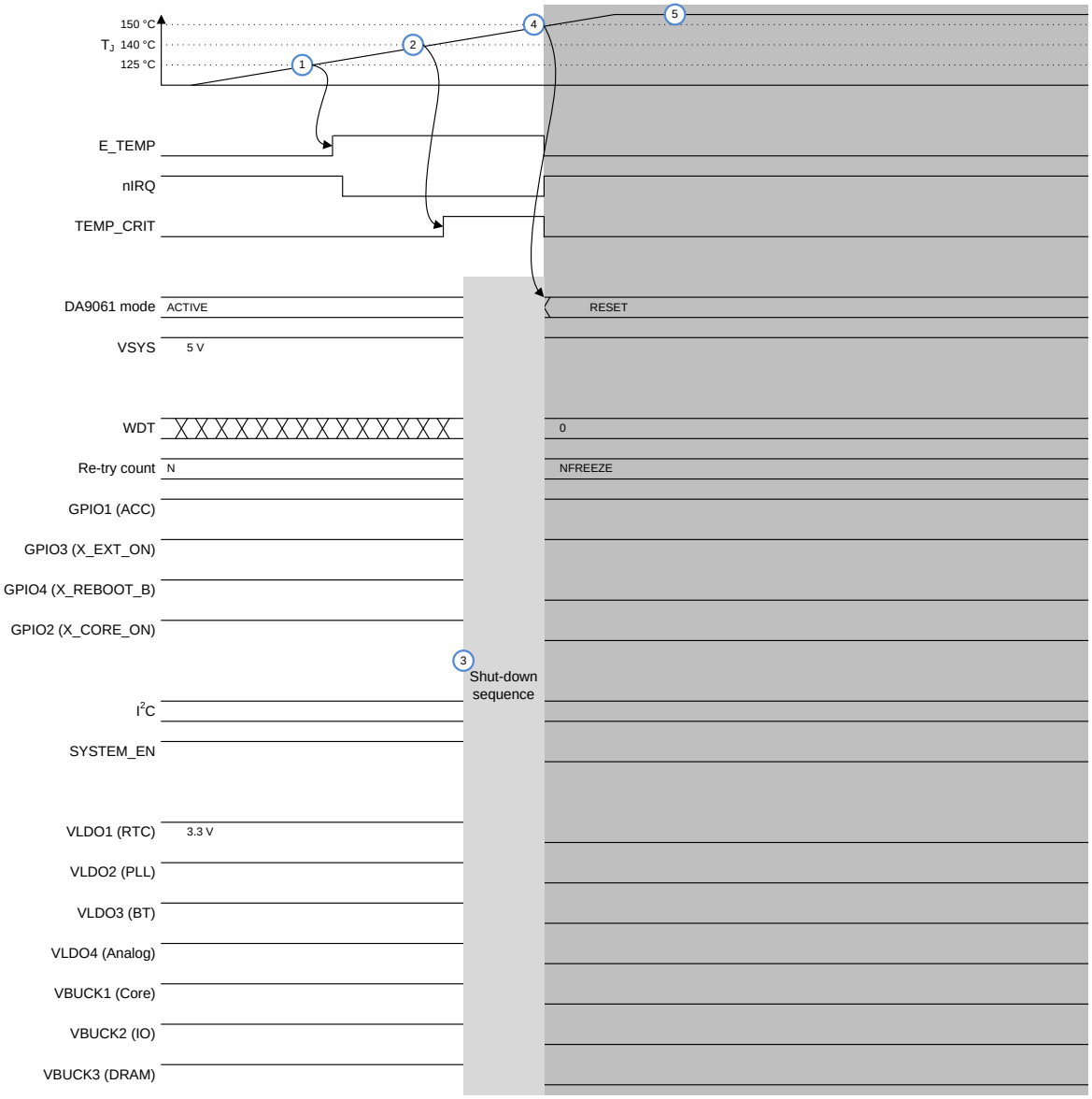

Figure 9: Timing Diagram for Temperature Power-On Reset

1. The die temperature exceeds T_{WARN} which causes the event E_TEMP (in register EVENT_B) to be asserted. The event, if not masked, asserts nIRQ.
2. The die temperature exceeds T_{CRIT} which causes the temperature error flag TEMP_CRIT (in register FAULT_LOG) to be set, and a shut-down sequence is triggered.
3. DA9061 executes the shut-down sequence which is the same as the power-down sequence described in Section 5.2 but a shut-down sequence triggered by over-temperature proceeds straight to the RESET mode.
4. The die temperature exceeds T_{POR} which causes DA9061 to enter the RESET mode without any sequencing. Also the always-on LDO1 is disabled.
5. DA9061 stays in the RESET mode as long as the temperature stays above T_{CRIT}. After this a cold boot is executed as described in Section 5.1.

5.9 System Supply Under-Voltage

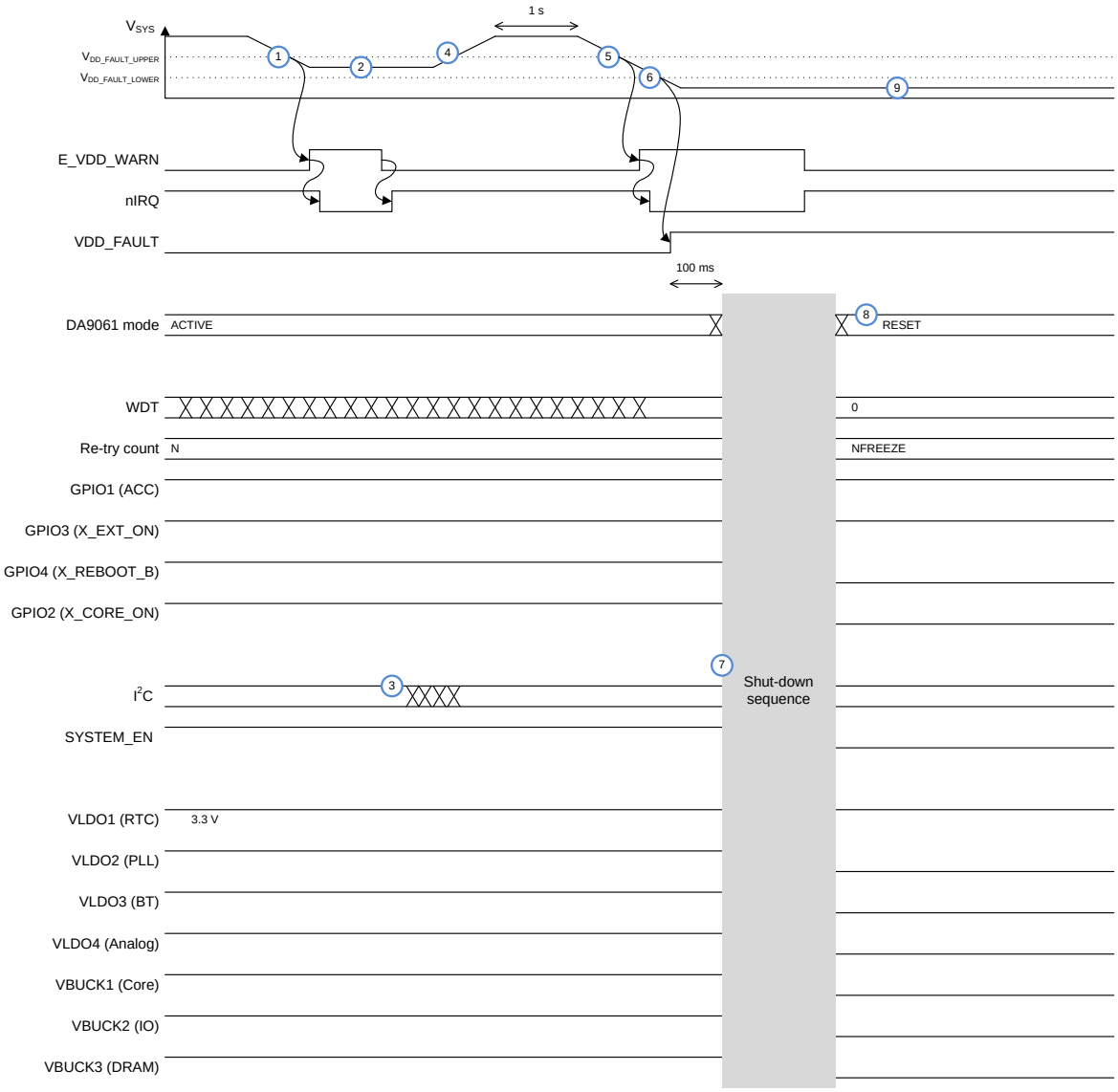

Figure 10: Timing Diagram for System Supply Under-Voltage

1. The system supply (V_{SYS}) drops below $V_{DD\_FAULT\_UPPER}$ which causes the event E_VDD_WARN (in register EVENT_B) to be asserted. The event, if not masked, asserts nIRQ.
2. AtlasVI software sees the system supply warning and reduces the activity of the platform. This should reduce the current draw of the platform and stabilize the system supply.
3. AtlasVI software clears the event E_VDD_WARN. If no other events are active, this de-asserts nIRQ.
4. The system supply recovers above the $V_{DD\_FAULT\_UPPER}$ threshold. After this, there is a 1 s debounce period for V_{SYS}. During this period the system supply comparators are not enabled and if V_{SYS} drops below $V_{DD\_FAULT\_UPPER}$ no event is generated.
5. V_{SYS} drops below $V_{DD\_FAULT\_UPPER}$ again which causes the event E_VDD_WARN to be asserted. The event, if not masked, asserts nIRQ.
6. V_{SYS} drops below $V_{DD\_FAULT\_LOWER}$ which causes the system supply error flag VDD_FAULT (in register FAULT_LOG) to be set, and a shut-down sequence is triggered.
7. DA9061 executes a shut-down sequence which the same as the power-down sequence described in Section 5.2 but a shut-down sequence triggered by a voltage error proceeds directly to the RESET mode.

8. DA9061 completes the shut-down sequence and enters the RESET mode. The re-try count is reset but the system supply error flag is not.
9. DA9061 stays in RESET mode as long as the system supply stays below VDD_FAULT_LOWER. After this, the power-up sequence is executed in the same way as in the cold boot use case described in Section 5.1.

6 Software Driver

After the DA9061 has started the AtlasVI system, software can read and write to the PMIC via the I^2C bus. This can be used for further PMIC configuration, such as the GPIOs, interrupt servicing, watchdog 'keep-alive' writes, and so on. Dialog drivers for Linux™ are available in the Linux kernel from https://kernel.org/ [4] or, if interim assistance is required, from your Dialog Sales representative.

7 Development Support Tools and PMIC Configuration Files

To assist with hardware and software development, Dialog provides the following:

- DA9061 Evaluation Kit

This contains motherboard and daughterboard for hardware evaluation and software development. It also includes the SmartCanvas™ GUI software.

- SmartCanvas GUI

This is PC-driven software to provide easy access to a device under test (DUT). The GUI is used to exercise the DUT using the I^2C interface. Control or measurement of analog and digital pins is supported. SmartCanvas supports the Dialog PMIC OTP configuration file (.ini file) format.

- OTP configuration .ini file DA9061-03_Atlas6_0v1_547A.ini

This file defines the configuration of the DA9061 at boot. The file is available from the Dialog Support website. The .ini file is opened using the SmartCanvas GUI.

- Linux software driver. See Section 6.

8 Device Identification and Ordering

Available parts are shown in Table 2. If the DA9061-03 proves unsuitable for your target AtlasVI design, please contact your Dialog sales representative to discuss custom variants. (Minimum order quantities apply for custom variants.)

Table 2: Product Part Numbers

Part Number	Description (Note 1)
DA9061-03AMx	Industrial grade
DA9061-03AMx-A	Automotive AEC-Q100 Grade 3

Note 1 See the DA9061 datasheet [1] for further information regarding part ordering. All parts are available in Tray (x = 1) or Tape & Reel (x = 2).

Revision History

Revision	Date	Description
1.0	15-Sep-2016	Initial version

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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