Application Note

DA9313 Frequently Asked Questions

AN-PM-090

Abstract

Using a question-and-answer format, this application note presents solutions to various application topics when designing-in the DA9313 into a system.

DA9313 Frequently Asked Questions

Contents

1 Terms and Definitions

OVP	Over Voltage Protection
PVC	Power Voltage Converter
SoC	System on Chip
OD	Open Drain

2 References

[1] DA9313-Datasheet, Dialog Semiconductor

3 Introduction

The purpose of this applications note is to help customers understand the various aspects of the DA9313 converter when designed into their systems.

4 Frequently Asked Questions

4.1 External Components

1. Could the flying capacitor value or quantity be reduced?

Reducing the flying capacitor value will impact efficiency. Reducing the quantity of capacitors may impact reliability. The flying capacitor must have the appropriate ripple current rating to meet the maximum 20 ºC temperature rise requirement.

2. What is the flying capacitors (CFLY) effective capacitance?

C_{FLY} per phase must be rated to ≥ 18 µF @ 5 V, I_{RMS} = 8 A. For a lower output load current, contact ic-support@diasemi.com for technical support.

Note that there are two CFLY in parallel per phase, therefore each capacitor must be rated to ≥ 9 µF @ 5 V, I_{RMS} = 4 A.

3. What is the VCORE capacitor (CO_VCORE) effective capacitance?

The external CO_VCORE effective capacitance should be min 0.5 µF, max 1.3 µF and is typically 1.0 µF.

What are VIN to VOUT and VOUT to GND decoupling capacitors used for? Could I reduce their values?

They are used to decouple the internal FET drivers that are connected to VIN, VOUT and GND.

The VIN to VOUT capacitor value could be reduced to 1 µF because there should be a localized decoupling to VIN (2 x 4.7 µF or 1 x 10 µF as recommended in the datasheet). The VOUT to GND cap must be 4.7 µF as specified in the datasheet.

4. Could I add a large decoupling capacitor on VIN, as recommended in the datasheet, knowing that I need to meet the USB requirements limiting the capacitor to 1 µF?

Yes. Generally an OVP IC is added at the front end of the DA9313, this limitation is for the OVP IC.

5. Has the DA9313 got an integrated over-voltage protection (OVP)?

No. The following tiny external OVP devices could be used: TI TPD1S514, Fairchild FPF2280, and Kinetic KTS1682. They all are pinout compatible parts with a very similar feature set.

6. What is the maximum output capacitance allowed at the output of the PVC?

470 µF (it can be distributed).

4.2 Power Voltage Converter

7. What is the allowed maximum DC load current of the PVC?

Typically, it is 8.2A (DC) continuously (10A peak) but it depends on the use case.

8. What defines the PVC ramp-up time?

The value of output capacitor and the startup current set by I_STUP_PVC, configured from 500 mA to 2 A.

9. When should I apply a load at the output of the PVC?

Monitor that the PVC output reaches $V_{DD}/2$ – 80 mV before a load greater than half of I_STUP_PVC is applied to its output for both standalone and master/slave modes.

10. Could I operate the PVC above 10.5 V?

No. When the PVC is enabled (PVC_EN = 1), V_{IN} must be limited to 10.5 V maximum.

If the PVC is disabled (PVC_EN = 0), 20 V could be applied to V_{IN} assuming that V_{IN} ramp < 1 V/µs.

11. Could I operate the PVC below 5 V?

No. The internal FET drivers operating voltage is 5 V minimum.

4.3 I²C Compatible Interface

12. Could the DA9313 slave be controlled by I2C?

No. The slave I^2C lines must be grounded.

13. What is the master/slave interface (MS_IF) protocol on GPIO_0?

GPIO_0, used as MS_IF, voltage domain is VCORE.

a. GPIO_0 is asserted high during the PVC ramp up.
b. Then it remains low until a load higher than approximately 3 A is applied
c. The GPIO_0 then starts toggling to control the switching of the slave's phases; phase 1 and phase 2 in turn. The more load that is applied the more the slave switches between phase 1 and phase 2.
d. When the PVC is disabled the master sends a 100 ns shutdown pulse (low) to the slave.
e. The slave stops switching, GPIO_0 will then stay high during the duration of the PVC shutdown phase and eventually GPIO_0 will be asserted low.

14. **What is the voltage domain of all IOs (GPIOs and I2C) when operating the DA9313 in** master/slave?

All IOs are reference to VCORE (4 V). They may need to be level shifted externally. VDDIO_EN and VDDIO_CONF controls are ignored.

15. What is the master/slave current sharing ratio?

From approximately 3 A both the master and slave start sharing the output load. When the output load reaches approximately 4 A the current sharing is approximately equally distributed.

16. How does the master know when to operate the slave?

By monitoring V_{OUT} and comparing it to the voltage at the master slave interface level (V_{MSI}). This monitoring is used to trigger the slave device via the master/slave interface (MS_IF). The level at which the master triggers the slave is defined in PVC_MS_DROP.

a. When the V_{OUT} voltage decreases beyond V_{MSI} due to progressive output loading, the master DA9313 enables the slave DA9313 over MS_IF.
b. When the V_{OUT} voltage increases above V_{MSI} + $V_{PVC\_MS\_HYST}$ (defined in register bits PVC_MS_HYST), the master DA9313 disables the slave DA9313 over MS_IF.

$V_{MSI} = V_{CCM} – V_{PVC\_MS\_DROP}$

Where:

- $V_{CCM} = (V_{BAT}/2 - V_{PVC\_DROP} - V_{PVC\_HYSTMAX})$
- $V_{PVC\_HYSTMAX}$ is a constant value of 30 mV

17. Could I use the master GPIO_1 when operating in master/slave?

Yes. GPIO_1 is used as SLAVE_ID. For the slave, GPIO_1 is connected to its own VCORE. For the master, GPIO_1 must be un-driven by the System on Chip (SoC).

If the master's GPIO_1 is used in Open Drain (OD) with an external pull-up then Dialog would recommend that the pull-up resistor must be > 820 kΩ to prevent a false SLAVE_ID recognition.

Could I communicate with the DA9313 in POWER_DOWN mode?

No. The host processor should wait for DA9313 to reach the ACTIVE mode following a start-up from OFF or POWER_DOWN before starting the I^2C communication with DA9313.

18. If I don't use the master or standalone I2C lines, how should I connect them?

If the I^2C is not being used, then the I^2C lines must be connected to GND.

4.4 Other

19. Could I overdrive the nONKEY pin?

No. The nONKEY port should be never externally overdriven to a voltage higher than VCORE (4 V).

20. Is there a Linux driver available for DA9313?

A Linux driver will be available in March 2017. Please contact ic-support@diasemi.com for technical support.

21. What are the VIH and VIL levels of the integrated GPI Schmitt trigger?

V_{IH} is 60 % to 67.9 % of IOVDD and V_{IL} is 34.7 % to 40.2 % of IOVDD over PVT (Process Voltage Temperature).

Revision History

Revision	Date	Description
1.0	21-Feb-2017	Initial version.

DA9313 Frequently Asked Questions

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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