Application Note

DA9061/2 Schematic Checklist

AN-PM-103

Abstract

Optimizing the schematic for DA9061/2 ensures correct and efficient operation of the PMIC and the system. This is achieved by selecting appropriate external passive components, and appropriate configuration of the PMIC OTP.

DA9061/2 Schematic Checklist

Contents

1 Terms and Definitions

GUI	Graphical user interface
OTP	One-time programmable (memory)
RTC	Real time clock
SoC	System-on-chip
PMIC	Power management integrated circuit
SmartCanvas™	Dialog GUI

2 References

[1] DA9062, Datasheet, Dialog Semiconductor

[2] DA9061, Datasheet, Dialog Semiconductor

[3] UM-PM-008, SmartCanvas™ DA9061/2 User Manual, Dialog Semiconductor

3 Introduction

DA9061/2 is a power management integrated circuit (PMIC) optimized for supplying systems with single- and dual-core processors, I/O, DDR memory, and peripherals. It targets mobile devices, medical equipment, IVI systems, and FPGA-based applications.

This checklist is intended to help a hardware designer identify common errors that can arise in schematics containing the DA9061/2. The checklist is only a reference to common errors, and is not a substitute for rigorous system development and an understanding of the PMIC behavior as described in the DA9061/2 datasheet [1] [2].

4 Schematic Checklist

Table 1: Checklist

General	**Comments**		
Design name			
Schematic version			
Review date			
OTP variant	**Notes**	**Checked (Y/N)**	**Comments**
Which OTP variant is being used?	This can provide useful background for the review.		
OTP version number			
Core Operation			
V_{SYS}	2.8 V to 5.5 V		
V_{DDIO}	1.2 V to 3.6 V		
VSYS capacitor	1 µF		
IREF resistor	200 kΩ. Must be ≤1 % tolerance.		
VREF capacitor	2.2 µF		
VBBAT capacitor	470 nF		
VDDCORE capacitor	2.2 µF		
Crystal	The RTC requires an external crystal of 32.768 kHz as well as load Capacitors.		
XTAL_IN and XTAL_OUT	If the crystal is not required then both pins should be grounded.		

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Core operation	Notes	Checked (Y/N)	Comments
nRESET timing	The nRESET timer control can be set in SmartCanvas™. RESET_EVENT sets the start point of time and RESET_TIMER the time till reset event. Make sure nRESET is active until after the important rails have turned on.		
nRESET pin	Register control IRQ_TYPE determines if the pin is push-pull or open-drain. Check an external pull-up is present if open-drain.		
nRESETREQ	nRESETREQ is an active-low reset input. nRESETREQ should be either pulled high to V_{SYS} or tied to V_{SYS}, never floating.		
nONKEY	nONKEY should be either pulled high to V_{SYS} or tied to V_{SYS}, never floating.		
TP	TP should not be left floating. Pull down to ground, via 10 kΩ. Ideally, a test-point will be provided for system debug.		
LDOs			
LDO input voltages	LDO2/3/4: 2.8 V to 5.5 V If supplied by a buck, the minimum voltage is 1.5 V.		
LDO2/3/4 input capacitor	1 µF		
LDO1 output capacitor	1 µF		
LDO2/3/4 output capacitor	2.2 µF		
LDO output voltage	LDO1: 0.9 V to 3.6 V LDO2/3/4: 0.9 V to 3.6 V		
LDO output current	LDO1: 100 mA LDO2/3/4: 300 mA		
DVC_1 register control	If VDLO<x>_SEL_A and VDLO<x>_SEL_B have different voltages and only one specific voltage is desired, then the regulator needs to be set correctly.		
Bucks			
Buck supply voltage	2.8 V to 5.5 V Supply voltage minimum for Buck3 is 3.3 V if IOUT > 1.5 A.		
Input capacitors	2 x 22 µF or 4 x 10 µF		

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Bucks	Notes		Checked (Y/N)	Comments
Buck output voltage	Buck1/2: 0.3 V to 1.57 V Buck3: 0.8 V to 3.34 V Buck4: 0.53 V to 1.8 V			
Buck output current	Buck1/2: 2.5 A Buck3: 2 A Buck4: 1.5 A			
Buck1/2/3/4: current limit register settings I_{LIM}	Controlled with BUCK<x>_ILIM register. **Buck1/2:** Full Current Mode: 1400 mA to 4400 mA Half Current Mode: 700 mA to 2200 mA **Buck3:** 1700 mA to 3200 mA **Buck4:** 700 mA to 2200 mA			
Minimum ISAT values required at current limits	**Current limit:**	**ISAT:**		
	1500 mA	1750 mA		
	1200 mA	1460 mA		
	950 mA	1180 mA		
	750 mA	940 mA		
Buck1/Buck2 dual-phase mode	5 A output. Enabled by controls BUCK1_2_MERGE. Outputs from both inductors need to be routed together.			
Output capacitors	**Buck1/2:** Full Current Mode: 2 x 47 µF Half Current Mode: 2 x 22 µF **Buck3:** At $I_{OUT} \leq 1.5$ A: 2 x 22 µF At $I_{OUT} > 1.5$ A: 2 x 47 µF **Buck4:** 2 x 22 µF			
DVC_1 register control	If VBUCK<x>_SEL_A and VBUCL<x>_SEL_B have different voltages and only one specific voltage is desired then the regulator needs to be set correctly.			

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GPIOs	Notes	Checked (Y/N)	Comments
Unused GPIOs	Check that they are one of the following: ● configured as an input, with internal pull-down enabled via register CONFIG_K, or, ● configured as an output, or, ● tied to GND		
GPIO events	Check unused GPIOs have events masked in register IRQ_MASK_C.		
Are there any GPIOs configured to have special features? (SYS_EN, PWR_EN, Watchdog trigger input)	Check the signal behavior. Ensure the port is correctly configured as active-high or active-low using control GPIO<x>_TYPE.		
Power Sequencer			
Start-up sequence	Is it correct for the system requirements?		
WAIT_STEP and dummy slots	Has the WAIT_STEP feature been used correctly, or set to 0x00? If dummy (empty) slots are used, are they correct?		
Minimize in-rush	Turning all regulators on in the same slot will cause a large inrush current and potentially cause a drop in input voltage and cause the PMIC to power down.		
Are the sequencer pointers placed in a suitable slot?	PART_DOWN ≤ SYSTEM_END SYSTEM_END ≤ POWER_END POWER_END ≤ MAX_COUNT		

5 Further Assistance

For further assistance on debugging and for a detailed schematic and OTP check, please refer to the DA9061/2 Datasheet found on the Dialog website (https://www.dialog-semiconductor.com/pmics) or contact your local FAE.

Revision History

Revision	Date	Description
1.0	16-Nov-2017	Initial version.

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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