Application Note

FMEA of Pin-to-Pin Shorts and Opens for DA9061/2

AN-PM-110

Abstract

The design process of an electronic module in a safety-critical system often uses ISO 26262 as its basis. As an input to this process, this application note presents the likely failure modes in the case of pin-to-pin short faults or open circuit pin faults. The Dialog reference design for DA9061 and NXP® i.MX™ 6Solo processor is used as an example. This can be extended and revised for other Dialog PMICs and processor platforms.

Contents

1 Terms and Definitions

ASIL	Automotive Safety Integrity Level
FMEA	Failure Mode and Effects Analysis

2 References

[1] DA9061 Datasheet, Dialog Semiconductor
[2] ISO 26262, 'Road vehicles – Functional safety'
[3] AN-PM-081 'DA9061 / NXP i.MX 6Solo Power Connections', v2.0, 18-Jul-2016

3 Introduction

Dialog Semiconductor manufactures system PMICs and sub-PMICs for automotive, industrial and consumer applications. The design process of an electronic module in a safety-critical system often uses ISO 26262 as its basis. This requires an analysis of element failure modes, including those associated with the IC elements. As an input to this process, this application note presents the likely failure modes in the case of pin-to-pin short faults or open circuit pin faults. Note that these faults are considered as applied externally to the IC and therefore are board-level failures rather than IC-level reliability failures. Example sources of such faults are stray conductive filaments causing pin-to-pin shorts or a PCB manufacturing defect causing an open-circuit track: these are therefore distinct from the IC reliability failure mechanisms which are assessed by the IC qualification and reported in the Quality Report (available from Dialog upon request).

This application note uses the Dialog reference design for DA9061 and NXP® i.MX™ 6Solo processor as an example. Note that the failure modes are dependent on the configuration of the PMIC in the system. It is therefore necessary to extend and revise this example FMEA for other Dialog PMICs and systems, such as DA9062, DA9063 and DA9063L, and other platforms such as the i.MX 8 family, Renesas® R-Car™, and so on. This can be done by examining the details presented in this application note and extending to similar bucks, LDOs, GPIOs, and so on. Or please contact your Dialog sales representative for further support.

4 Failure Mode and Effects Analysis

The failure modes considered were pin-to-pin shorts and open-circuits, as applied to a DA9061 in an i.MX 6Solo system. This FMEA was based on the PMIC powered and in the ACTIVE state. Only the effect on the PMIC was assessed. The impact on other components in the system was not considered. It was assumed that pins around a package corner cannot be shorted. It was also assumed that the No Connect (NC) pins are configured as defined in the datasheet [1] which instructs, 'Do not use. Leave floating'.

Table 1: Pin-to-Pin Shorts Analysis

Pin Pair (Adjacent Pin) List		Electrical Behavior when the Pins are Shorted	Confidence in Assessment (1 to 5, where 5 is Certainty)
1 VLDO1	2 VLDO2	Shorted rail will be driven to the higher set voltage of VLDO2 = 3.0 V. VLDO1 will therefore be over-voltage. If the total load is > 300 mA then LDO2 may enter dropout and therefore be < 3.3 V.	4
2 VLDO2	3 VDD_LDO2	Shorted rail will be driven to the high voltage of VDD_LDO2 (5 V). VLDO2 will therefore be over-voltage.	5
3 VDD_LDO2	4 IREF	EOS damage likely. PMIC unlikely to start.	4
4 IREF	5 VREF	EOS damage likely. PMIC unlikely to start.	4
5 VREF	6 NC	Internal impedance of NC pin likely to upset VREF and the PMIC operation. Extended exposure may cause EOS.	3
6 NC	7 VSS_ANA	No effect	5
7 VSS_ANA	8 NC	No effect	5
8 NC	9 VLDO3	Internal impedance of NC pin may load LDO. Extended exposure may cause EOS.	2
9 VLDO3	10 VDD_LDO34	LDO3 over-voltage. There will be leakage through the pull-down resistor when the PMIC is in POWERDOWN mode.	4

Pin Pair (Adjacent Pin) List		Electrical Behavior when the Pins are Shorted	Confidence in Assessment (1 to 5, where 5 is Certainty)
11 VLDO4	12 NC	No effect	4
12 NC	13 SDA	Internal impedance of the NC pin may cause I^2C communications failure.	3
13 SDA	14 SCL	I^2C bus communications failure	5
14 SCL	15 nONKEY	Possible I^2C bus communications failure. The bus may continue to operate if the pull-up resistor from nONKEY to VSYS is weak.	3
15 nONKEY	16 nRESETREQ	No impact to PMIC as both pins are unused and pulled up to VSYS.	5
16 nRESETREQ	17 VLX_BUCK3	The PMIC will start with nRESETREQ initially low (no edge). LX switching will cause a PMIC reset. Drive from the LX may damage nRESETREQ or other system component.	3
17 VLX_BUCK3	18 VDD_BUCK3	Buck EOS may occur when the buck turns on. Rail will be over-voltage.	4
18 VDD_BUCK3	19 VDD_BUCK3	No effect (both pins are tied to VSYS)	5
19 VDD_BUCK3	20 VLX_BUCK2	Buck EOS may occur when the buck turns on. Rail will be over-voltage.	4
21 GPIO0	22 GPIO1	These pins are unused and grounded for DA9061-62-A. A short has no effect.	5
22 GPIO1	23 VDDIO	GPIO1 is grounded for DA9061-62-A. A short will therefore also ground VDDIO, supplied from Buck2. Buck2 EOS damage likely.	4
23 VDDIO	24 VBUCK3	VDDIO/Buck2 and Buck3 voltages will be incorrect. EOS likely to occur.	3
24 VBUCK3	25 VBUCK2	Buck voltages will be incorrect. EOS likely to occur.	3
25 VBUCK2	26 VBUCK1	Buck voltages will be incorrect. EOS likely to occur.	3
26 VBUCK1	27 NC	No effect	4
27 NC	28 GPIO2	If the NC pin is floating then no effect. If the NC pin is grounded, then the GPIO will be a stuck-at-0 fault.	5
28 GPIO2	29 GPIO3	A short will pull up GPIO2 to a logic '1'. This will result in VBUCK3 supplying 1.35 V instead of 1.5 V.	5
29 GPIO3	30 GPIO4	A short will pull down GPIO3 to a logic '0'. This will result in LDO2 supplying 3.3 V instead of 3.0 V.	5
31 VLX_BUCK1	32 VDD_BUCK1	Buck EOS may occur when the buck turns on. Rail will be over-voltage.	4
32 VDD_BUCK1	33 NC	No effect	5
33 NC	34 NC	No effect	5
34 NC	35 NC	No effect	5
35 NC	36 TP	No effect in normal system operation (TP = 0 V). Internal NC impedance may affect the ability to use debug mode where TP = 5.0 V. EOS may occur if attempting in-circuit programming with TP = 7.5 V.	3

Pin Pair (Adjacent Pin) List		Electrical Behavior when the Pins are Shorted	Confidence in Assessment (1 to 5, where 5 is Certainty)
36 TP	37 nIRQ	The pull-down on TP and the pull-up on nIRQ will cause the open-drain voltage of nIRQ to be lowered (depending on resistor values). Therefore nIRQ may not function.	4
37 nIRQ	38 nRESET	These are configured as open-drain outputs. A short will result in digital errors, for example causing the SoC to enter the reset state instead of receiving only an interrupt. No damage to the PMIC is expected.	4
38 nRESET	39 VDDCORE	The PMIC digital operation may be prevented when nRESET is low.	3
39 VDDCORE	40 VSYS	EOS damage is likely. The PMIC is unlikely to start.	4

Table 2: Pin Open-Circuit Analysis

Pin	Electrical Behavior when the Pins are Open-Circuit	Confidence in Assessment (1 to 5, where 5 is Certainty)
1 VLDO1	No VLDO rail	5
2 VLDO2	No VLDO rail	5
3 VDD_LDO2	No VLDO rail	5
4 IREF	The PMIC will not function. EOS damage may occur.	4
5 VREF	The PMIC will not function. EOS damage may occur.	4
6 NC	No effect	5
7 VSS_ANA	PMIC will not function reliably.	4
8 NC	No effect	5
9 VLDO3	No VLDO rail	5
10 VDD_LDO34	No VLDO rail	5
11 VLDO4	No VLDO rail	5
12 NC	No effect	5
13 SDA	I^2C bus communications failure	5
14 SCL	I^2C bus communications failure	5
15 nONKEY	No effect if the pin floats high. Risk of spurious PMIC resets if the voltage falls below V_{IH}.	4
16 nRESETREQ	No effect if the pin floats high. Risk of spurious PMIC resets if the voltage falls below V_{IH}.	5
17 VLX_BUCK3	No buck output voltage	4
18 VDD_BUCK3	No buck output voltage	5
19 VDD_BUCK2	No buck output voltage	5
20 VLX_BUCK2	No buck output voltage	4
21 GPIO0	No effect as GPIO is unused	5
22 GPIO1	No effect as GPIO is unused	5

Pin	Electrical Behavior when the Pins are Open-Circuit	Confidence in Assessment (1 to 5, where 5 is Certainty)
23 VDDIO	Digital push-pull output signals will be stuck at 0 V. Digital inputs will continue to function as the OTP has control GPI_V = 0.	4
24 VBUCK3	Loss of feedback control of buck. Risk of buck output being driven to the VDD supply voltage. System over-voltage.	5
25 VBUCK2	Loss of feedback control of buck. Risk of buck output being driven to the VDD supply voltage. System over-voltage.	5
26 VBUCK1	Loss of feedback control of buck. Risk of buck output being driven to the VDD supply voltage. System over-voltage.	5
27 NC	No effect	5
28 GPIO2	The internal pull-down will set the input to a '0' and therefore Buck3 = 1.5 V.	5
29 GPIO3	The internal pull-down will set the input to a '0' and therefore LDO2 = 3.3 V.	5
30 GPIO4	No effect as GPIO is unused	5
31 VLX_BUCK1	No buck output voltage. The rail will remain at 0 V unless pulled-up by other system components.	4
32 VDD_BUCK1	No buck output voltage	5
33 NC	No effect	5
34 NC	No effect	5
35 NC	No effect	5
36 TP	PMIC may not function reliably, especially if the pin floats above VIL.	5
37 nIRQ	No effect on PMIC. Hardware interrupts to the SoC will be lost.	5
38 nRESET	No effect on PMIC. Hardware reset to the system will be lost. This may risk EOS to system components if the supplies are not properly sequenced.	5
39 VDDCORE	The PMIC will not function reliably.	5
40 VSYS	The PMIC will not function reliably. However, the internal VSYS supply might be back-fed through other pins (for example the buck VDD pins or the VDDIO pin) and therefore the PMIC may operate.	5

5 Conclusions

An example FMEA for Dialog system PMICs has been presented based on DA9061 and i.MX 6Solo.This can be extended and modified for other Dialog PMICs such as DA9062, DA9063, DA9063L, and so on.

Revision History

Revision	Date	Description
1.0	16-Apr-2018	First release.

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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