

# Application note

## DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

AN-PM-31

### Abstract

*This application note provides the details of the required connectivity between the DA9053 Power Management Integrated Circuit (PMIC) and the NXP™ i.MX 6DualLite or Solo applications processors.*

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**1 Terms and definitions**

|      |                                     |
|------|-------------------------------------|
| PMIC | Power Management Integrated Circuit |
| DVS  | Dynamic Voltage Scaling             |
| HW   | Hardware                            |
| SW   | Software                            |

**2 References**

- [1] DA9053-00-IDS3a\_140114.pdf, Datasheet, Dialog Semiconductor,2014
- [2] AN-PM-007 Suspend and Resume 1r2.pdf, 2015
- [3] AN-PM-010\_PCB\_Layout\_Guidelines\_1v3.pdf,2015
- [4] IMX6DQ6SDLHDG.pdf, Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Applications Processors,2013
- [5] DA9053 Reference board, 44-179-115-04-A1,44-179-115-05-A1 or 44-179-115-02-C1, 2014
- [6] DA9053 iMX6DL Sabre schematic, 44-179-09-B1.pdf, 2013

## DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

### 3 Introduction

This document is a reference for connectivity between the DA9053 Power Management Integrated Circuit (PMIC) and the NXP™ i.MX 6 DualLite and Solo applications processors for a typical multimedia applications. The i.MX 6 DualLite and the i.MX 6 Solo processors are pin compatible and have compatible power requirements: as such, this document refers to the DualLite version, but is equally applicable to the Solo.

DA9053 PMIC is a highly integrated chip that supports the Dynamic Voltage Scaling (DVS) technology, enabling significant power savings by intelligently managing voltage and frequency changes similar to the technology used in many processors. As a result of its highly-integrated features, the DA9053 PMIC reduces overall system cost and size significantly when compared to an equivalent discrete solution. This document addresses only the power-supply related features; addressing all of the features and functions of the optimised PMIC is beyond the scope of this document.

For further information on the DA9053 please refer to the datasheet available via your local Dialog Sales Office.

For information about the NXP™ i.MX 6 applications processor family, please refer to [NXP™ website](#)

#### NOTE

Since this document was created Freescale™ has been acquired by NXP™. All references to Freescale™ now apply to NXP™

### 4 Purpose

This document:

- Briefly introduces the DA9053 PMIC
- Contains information about power domains, component selection, and DA9053 PMIC interconnection with the NXP™ i.MX 6 DualLite applications processor
- Bases its design on the NXP™ i.MX6 DualLite SABRE board

### 5 DA9053 description

The DA9053 is a highly-integrated PMIC with supply domain flexibility to support a range of multimedia processor platforms, their associated peripherals and user interface functions.

DA9053's applications are, for example, tablet PCs, embedded and industrial modules, mobile internet devices and consumer and in-vehicle infotainment devices.

Along with four buck convertors and 10 LDOs that are required to address the requirements of most i.MX6 DualLite based systems, the DA9053 also includes:

- A dual input charger with power path support
- A white LED boost convertor
- A watchdog timer
- A 3-channel general purpose 10-bit ADC
- A resistive touch screen interface

# DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

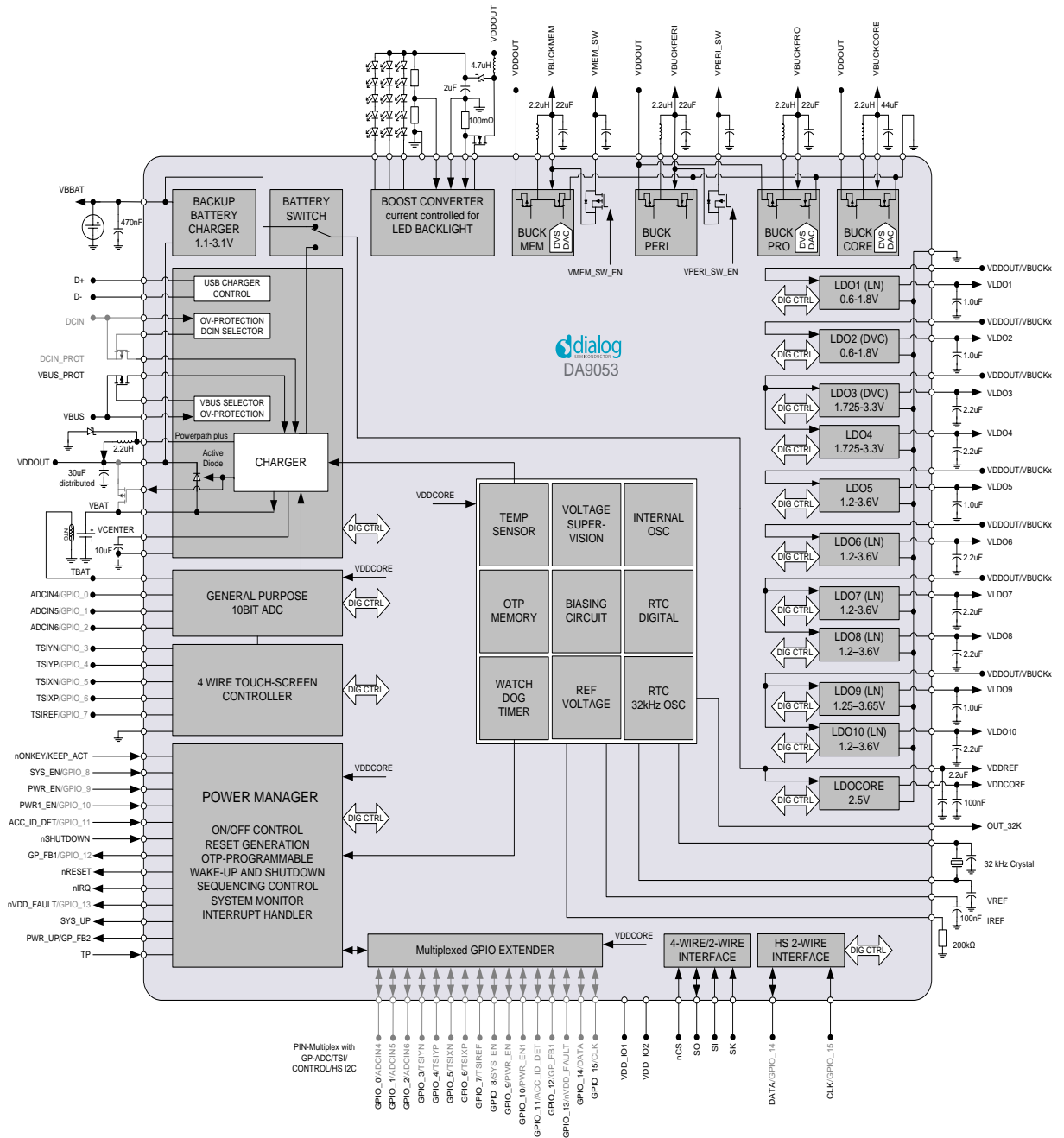


Figure 1: DA9053 system block diagram

## DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

**Table 1: DA9053 buck and LDO definition**

| Regulator                    | Output voltage,<br>(Note 1)                | Max<br>Current | Notes  |
|------------------------------|--|----------------|--|
| BUCKCORE                     | 0.5 – 2.075 V                              | 2000 mA        | DVC, 2 MHz, 25 mV steps, DVC ramp with controlled slew rate; pull-down disable   |
| BUCKPRO                      | 0.5 – 2.075 V                              | 1000 mA        | DVC, 2 MHz, 25 mV steps, DVC ramp controlled slew rate, pull-down resistor disable, common supply with BUCKPERI                                  |
| BUCKMEM                      | 0.95 – 2.525 V                             | 1000 mA        | DVC, 2 MHz, 25 mV steps, DVC ramp with controlled slew rate pull-down resistor disable 2 <sup>nd</sup> output with sequencer controllable switch |
| BUCKPERI                     | 0.95-2.525 V                               | 1000 mA        | 2 MHz, 25 mV steps, 2 <sup>nd</sup> output with sequencer controllable switch, common supply with BUCKPRO  |
| BOOST                        | 5 – 25 V                                   | 78 mA          | Current-controlled boost converter for three strings of up to six serial white LEDs. Over voltage protection via a voltage feedback pin.         |
| LDO1                         | 0.6 – 1.8 V                                | 50 mA          | High PSSR, low noise LDO, 50 mV steps, pull-down resistor disable  |
| LDO2                         | 0.6 – 1.8 V                                | 100 mA         | Digital LDO, 25 mV steps, DVC ramp with controlled slew rate, pull-down resistor disable   |
| LDO3                         | 1.725 – 3.3 V                              | 200 mA         | Digital LDO, 25 mV steps, DVC with controlled slew rate, common supply with LDO4   |
| LDO4                         | 1.725 – 3.3 V                              | 150 mA         | Digital LDO, 25 mV steps, optional HW control from GPI1, common supply with LDO3   |
| LDO5                         | 1.2 – 3.6 V                                | 100 mA         | Digital LDO, 50 mV steps, pull-down resistor switch off, optional HW control from GPI2,  |
| LDO6                         | 1.2 – 3.6 V                                | 150 mA         | High PSRR, low noise, 50 mV steps  |
| LDO7                         | 1.2 – 3.6 V                                | 200 mA         | High PSRR, low noise, 50 mV steps, common supply with LDO8   |
| LDO8                         | 1.2 – 3.6 V                                | 200 mA         | High PSRR, low noise, 50 mV steps, common supply with LDO7   |
| LDO9                         | 1.25 – 3.6 V<br>±1 % accuracy,<br>(Note 2) | 100 mA         | High PSRR, low noise, 50 mV steps, OTP trimmed, optional HW control from GPI12, common supply with LDO10   |
| LDO10                        | 1.2 – 3.6 V                                | 250 mA         | High PSRR, low noise, 50 mV steps, common supply with LDO9   |
| BACKUP<br>BATTERY<br>CHARGER | 1.1 – 3.1 V                                | 6 mA           | 100/200 mV steps, configurable current limit between 0.1 and 6 mA, reverse current protection  |
| LDOCORE                      | 2.5 V                                      | 4 mA           | Not for external use   |

**Note 1** Output accuracy is  $\pm 3$  % unless specified

**Note 2** At the default voltage (1 % accuracy requires VLDO9 > 1.5 V)

DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

## 6 NXP™ i.MX 6 DualLite applications processor description

The NXP™ i.MX 6 DualLite applications processor is an advanced, highly integrated platform for multimedia-centric devices.

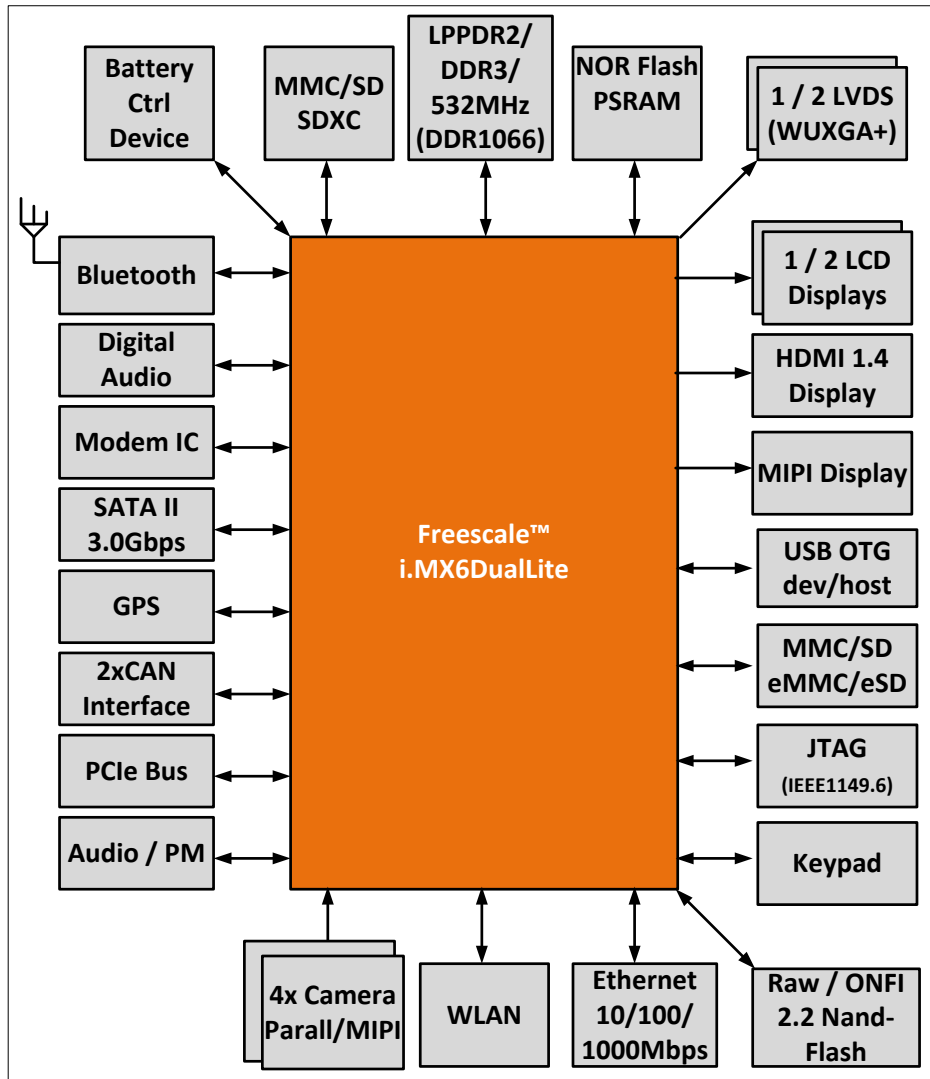


Figure 2: NXP™ i.MX 6DualLite based system

## 7 NXP™ i.MX 6 DualLite power supply rails

Table 2 shows the NXP™ i.MX 6 DualLite applications processor power supply rails as configured on the NXP™ SABRE board.

## DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

**Table 2: NXP™ i.MX 6DualLite power supply rails**

| i.MX 6DualLite Power Supply Rail  | i.MX 6DualLite SABRE Board Power Rail | DA9053                                     | DA9053 Time Slot | DA9053 Nominal Voltage |
|---|---------------------------------------|--|------------------|------------------------|
| VDDARM_IN   | VDDCORE                               | BUCKCORE                                   | TS2              | 1.375 V                |
| VDDSOC_IN, (Note 3)   | VDDSOC                                | BUCKPRO                                    | TS2              | 1.375 V                |
| VDDHIGH_IN  | VGEN5_2V8                             | LDO3                                       | TS12             | 2.8 V                  |
| VDD_SNVS_IN, (Note 4, Note 5, Note 6)   | PMIC_VSNVS                            | BBAT                                       | TS0              | 3.0 V                  |
| USB_OTG_VBUS, USB_H1_VBUS   |                                       | 4.4 V to 5.25 V From USB port              | NA               | NA                     |
| NVCC_DRAM   | DDR_1V5                               | BUCKMEM                                    | TS3              | 1.5 V                  |
| NVCC_RGMII, (Note 7)  | VGEN1_1V5                             | LDO6                                       | TS9              | 1.5 V                  |
| NVCC_LCD, NVCC_NANDE,<br>NVCC_SD2, NVCC_SD3,<br>NVCC_EIM0, NVCC_EIM1,<br>NVCC_EIM2, NVCC_JTAG | GEN_3V3                               | external DC-DC converter enabled by GP_FB2 | TS5              | 3.3 V                  |
| NVCC_ENET   | VGEN6_3V3                             | LDO7                                       | TS8              | 3.3 V                  |
| NVCC_SCI, NVCC_SD1  | GEN_1V8                               | BUCKPERI                                   | TS4              | 1.8 V                  |
| NVCC_GPIO   | NVCC_GPIO                             | LDO9                                       | TS5              | 3.3 V                  |
| NVCC_LVDS2P5, (Note 8)<br>NVCC_MIPI   | GEN2V5                                | Connected to i.MX 6Dual VDDHIGH_CAP1/2     | NA               |                        |
| VDDARM23_IN, (Note 9)   | GND                                   | GND  | NA               | GND                    |
| VREFDDR, (Note 10)  | VREFDDR                               | LDO1                                       | TS3              | 0.75 V                 |
|   | VGEN3_2V5                             | LDO5                                       | TS12             | 2.8 V                  |
|   | AUX_3V15                              | LDO8                                       | TS7              | 3.15 V                 |
|   | VGEN2_1V5                             | LDO10                                      | TS10             | 1.5 V                  |
|   | SPARE1                                | LDO2                                       | NA               |                        |
|   | SPARE2                                | LDO4                                       | NA               |                        |

**Note 3** VDDSOC\_CAP and VDDPU\_CAP must be equal

**Note 4** Care must be taken while setting VDD\_SNVS\_IN voltage with respect to Charging Currents and RTC, see Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Applications Processors (IMX6DQ6SDLHDG.pdf)

**Note 5** Must match the range of voltages that the rechargeable backup battery supports.

**Note 6** Should be supplied from the same supply as VDDHIGH\_IN, if the system does not require keeping real time and other data on OFF state.

**Note 7** All digital I/O supplies (NVCC\_XXXX) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.

**Note 8** This supply also powers the pre-drivers of the DDR I/O pins; therefore it must always be provided, even when LVDS is not used.

**Note 9** For a dual core system, may be shorted to GND together with VDDARM23\_CAP to reduce leakage

**Note 10** Care should be taken to follow the memory manufacturers recommendations for the generation of VREFDDR. In many cases a simple resistor divider positioned next to the memory devices will suffice.



DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

8 DA9053 – i.MX 6DualLite power connections

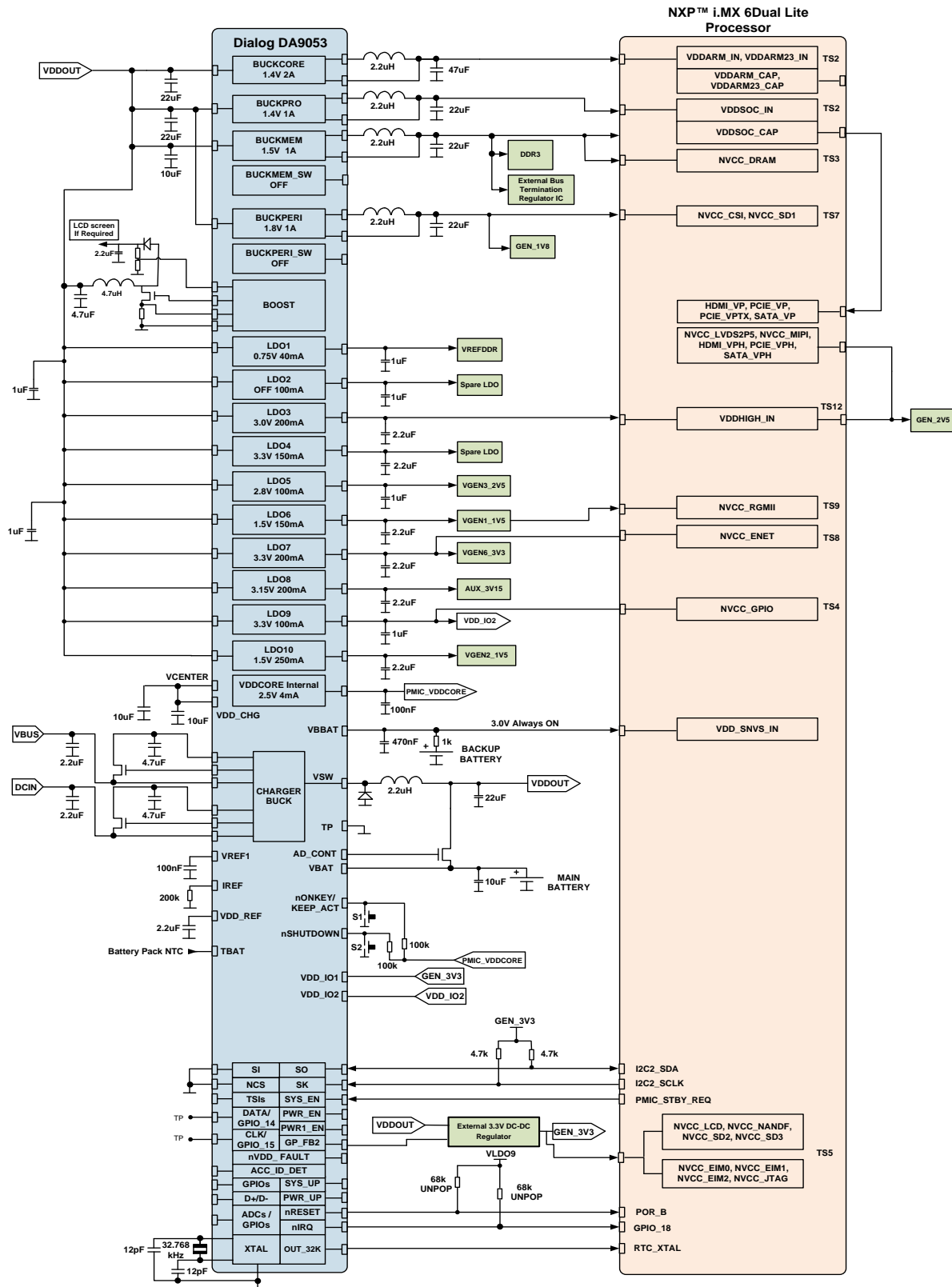


Figure 3: DA9053 / NXP™ i.MX 6DualLite applications processor example configuration

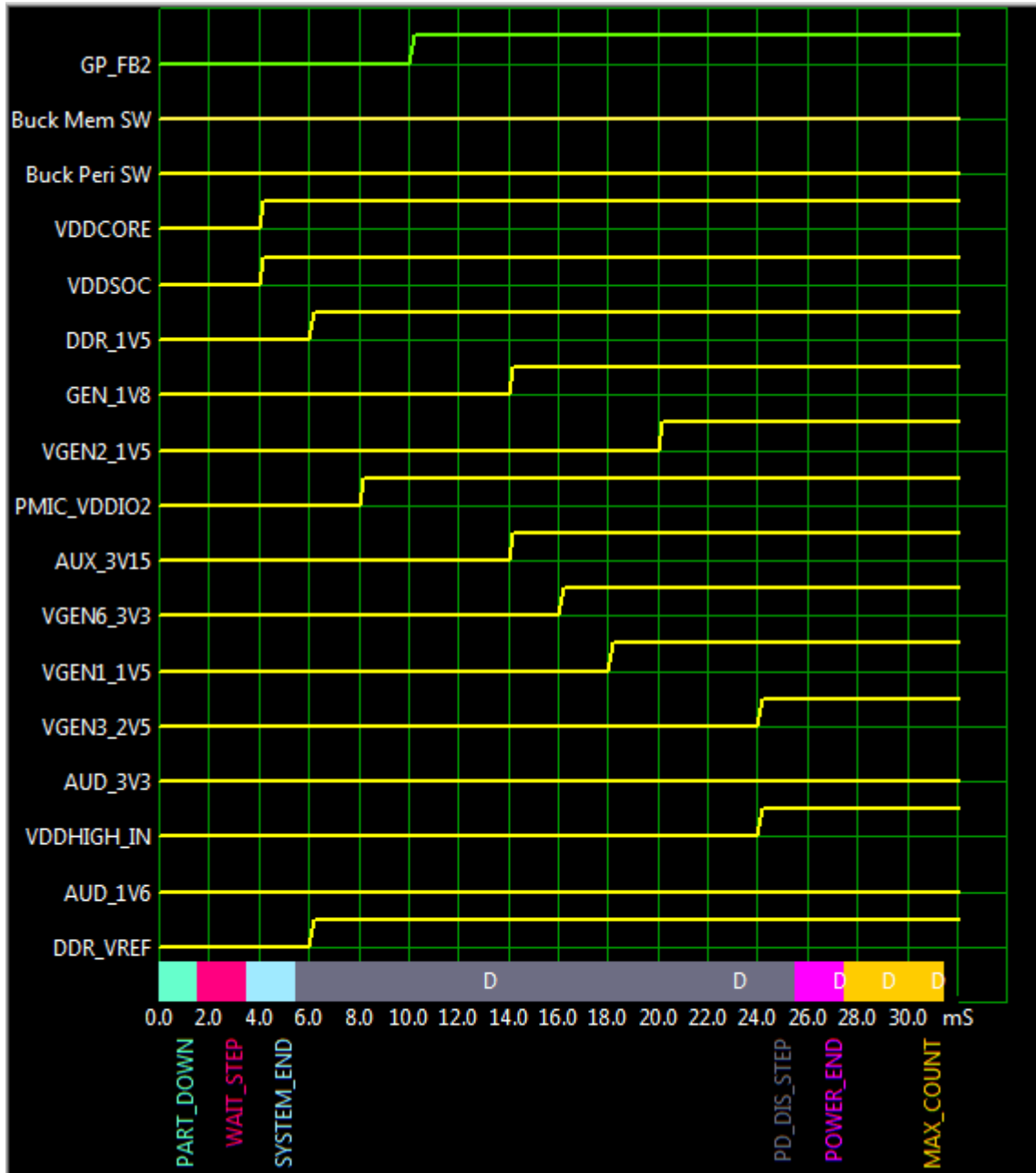
**DA9053 / NXP™ i.MX 6DualLite Applications  
Processor Example Power Connections**

**9 Power-up sequence**

The following power-up sequence is generated by the DA9053 Power Commander™ GUI.

The start-up behaviour and configuration is fully programmable in the DA9053 OTP and is therefore system agnostic.

The power-up sequence of Figure 4 is designed to meet the NXP™ iMX 6 DualLite start-up requirements as described in the i.MX 6 DualLite applications processor specification.



**Figure 4: DA9053 power-up sequence matching the NXP™ i.MX 6 DualLite applications processor power-up requirements**

## DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

### 10 Recommended external components

The following external components are used in the 'DA9053 Reference Board'[5].

**Table 3: Recommended external components**

| Ref Des | Description                                     | Manufacturer | Manufacturer's Part Number | Notes                        |
|---------|---|--------------|----------------------------|------------------------------|
| U       | DA9053-PMIC                                     | Dialog       | DA9053                     |                              |
|         | <u>DA9053 BUCKCORE – 2 A</u>                    |              |                            |                              |
| L       | 2.2 $\mu$ H SMD 2.7 A inductor                  | Taiyo Yuden  | NR4018T2R2M                | Output inductor              |
| C       | 47 $\mu$ F 0805 SMD Ceramic capacitor 4 V X5R   | MuRata       | GRM21BR60G476ME15          | Output capacitor             |
| C       | 22 $\mu$ F 0805 SMD Ceramic capacitor 6.3 V X5R | MuRata       | GRM21AR60J226UE80          | Input capacitor              |
|         | <u>DA9053 BUCKPRO – 1 A</u>                     |              |                            |                              |
| L       | 2.2 $\mu$ H SMD 1.48 A inductor                 | Taiyo Yuden  | NR3015T2R2M                | Output inductor              |
| C       | 22 $\mu$ F 0603 SMD Ceramic capacitor 6.3 V X5R | MuRata       | GRM188R60J226ME69          | Output capacitor             |
| C       | 22 $\mu$ F 0805 SMD Ceramic capacitor 6.3 V X5R | MuRata       | GRM21AR60J226UE80          | Input capacitor              |
|         | <u>DA9053 BUCKMEM – 1 A</u>                     |              |                            |                              |
| L       | 2.2 $\mu$ H SMD 1.48 A inductor                 | Taiyo Yuden  | NR3015T2R2M                | Output inductor              |
| C       | 22 $\mu$ F 0603 SMD Ceramic capacitor 6.3 V X5R | MuRata       | GRM188R60J226ME69          | Output capacitor             |
| C       | 10 $\mu$ F 0603 SMD Ceramic capacitor 10 V X5R  | MuRata       | GRM188R60J106M             | Input capacitor              |
| C       | 0.1 $\mu$ F 0402 SMD Ceramic capacitor 16 V X7R | MuRata       | GRM155R71C104KA88D         | BUCKMEM_SW Output capacitor  |
|         | <u>DA9053 BUCKPERI – 1 A</u>                    |              |                            |                              |
| L       | 2.2 $\mu$ H SMD 1.48 A inductor                 | Taiyo Yuden  | NR3015T2R2M                | inductor                     |
| C       | 22 $\mu$ F 0603 SMD Ceramic capacitor 6.3 V X5R | MuRata       | GRM188R60J226ME69          | Output capacitor             |
| C       | 0.1 $\mu$ F 0402 SMD Ceramic capacitor 16 V X7R | MuRata       | GRM155R71C104KA88D         | BUCKPERI_SW Output capacitor |
|         | <u>DA9053 CHARGER BUCK VDDOUT</u>               |              |                            |                              |
| L       | 2.2 $\mu$ H SMD 2.7A inductor                   | Taiyo Yuden  | NR4018T2R2M                | VDDOUT Output inductor       |
| C       | 22 $\mu$ F 0603 SMD Ceramic capacitor 10V X7R   | Murata       | GRM32ER71A226KE15L         | VDDOUT Output capacitor      |
| C       | 22 $\mu$ F 0603 SMD Ceramic capacitor 10V X7R   | MuRata       | GRM32ER71A226KE15L         | VDDOUT Output capacitor      |
| Q       | P-Channel SOT-23                                | Fairchild    | SI2333CDS                  | VDDOUT Output FET            |
|         | <u>DA9053 BOOST</u>                             |              |                            |                              |
| L       | 4.7 $\mu$ H SMD 1.7 A inductor                  | Taiyo Yuden  | NR3015T4R7M                | inductor                     |

## DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

| C      | 10 $\mu$ F 0603 SMD Ceramic capacitor 10 V X5R   | Panasonic    | ECJ-1VB1A106M              | Input capacitor                     |
|--------|--|--------------|----------------------------|-------------------------------------|
| C      | 2.2 $\mu$ F 1206 SMD Ceramic capacitor 25 V X5R  | MuRata       | GRM31MR71E22 5KA93L        | Output capacitor                    |
| RefDes | Description                                      | Manufacturer | Manufacturer's Part Number | Notes                               |
| C      | 100 pF 0402 SMD Ceramic capacitor 50 V COG       | MuRata       | GRM155C1H101 JD01D         | Feedback/OVP capacitor              |
| R      | 0R1 0402 SMD chip resistor                       | Panasonic    | ERJ2BSGR10x                | Current sense                       |
| R      | 1 M $\Omega$ 0402 SMD chip resistor              | Yageo        | RC0402FR-071ML             | Feedback/OVP #1                     |
| R      | 68 k $\Omega$ 0402 SMD chip resistor             | Yageo        | RC0402FR-0768KL            | Feedback/OVP #2                     |
| Q      | P-Channel SOT-23                                 | ON Semi      | NTLJF4156N                 | FET                                 |
|        | <u>DA9053 LDOs</u>                               |              |                            |                                     |
| C      | 1 $\mu$ F 0402 SMD Ceramic capacitor 16 V X7R    | MuRata       | GRM155R61A10 5KE15         | LDO Input capacitor                 |
| C      | 1 $\mu$ F 0402 SMD Ceramic capacitor 16 V X7R    | MuRata       | GRM155R61A10 5KE15         | LDO Input capacitor                 |
| C      | 1 $\mu$ F 0402 SMD Ceramic capacitor 10 V X5R    | MuRata       | GRM155R61A10 5KE15D        | LDO1 Output capacitor               |
| C      | 1 $\mu$ F 0402 SMD Ceramic capacitor 10 V X5R    | MuRata       | GRM155R61A10 5KE15D        | LDO2 Output capacitor               |
| C      | 2.2 $\mu$ F 0402 SMD Ceramic capacitor 6.3 V X5R | Kemet        | C0402C225M9P AC            | LDO3 Output capacitor               |
| C      | 2.2 $\mu$ F 0402 SMD Ceramic capacitor 6.3 V X5R | Kemet        | C0402C225M9P AC            | LDO4 Output capacitor               |
| C      | 1 $\mu$ F 0402 SMD Ceramic capacitor 10 V X5R    | MuRata       | GRM155R61A10 5KE15D        | LDO5 Output capacitor               |
| C      | 2.2 $\mu$ F 0402 SMD Ceramic capacitor 6.3 V X5R | Kemet        | C0402C225M9P AC            | LDO6 Output capacitor               |
| C      | 2.2 $\mu$ F 0402 SMD Ceramic capacitor 6.3 V X5R | Kemet        | C0402C225M9P AC            | LDO7 Output capacitor               |
| C      | 2.2 $\mu$ F 0402 SMD Ceramic capacitor 6.3 V X5R | Kemet        | C0402C225M9P AC            | LDO8 Output capacitor               |
| C      | 1 $\mu$ F 0402 SMD Ceramic capacitor 10 V X5R    | MuRata       | GRM155R61A10 5KE15D        | LDO9 Output capacitor               |
| C      | 2.2 $\mu$ F 0402 SMD Ceramic capacitor 6.3 V X5R | Kemet        | C0402C225M9P AC            | LDO10 Output capacitor              |
| C      | 0.1 $\mu$ F 0402 SMD Ceramic capacitor 16 V X7R  | MuRata       | GRM155R71C10 4KA88D        | VDDCORE                             |
|        | <u>DA9053 SYSTEM DECOUPLING</u>                  |              |                            |                                     |
| C      | 470 nF 0402 SMD Ceramic capacitor 6.3 V X5R      | MuRata       | GRM155R61A47 4KE15D        | Backup Battery Decoupling capacitor |
| C      | 4.7 $\mu$ F 0603 SMD Ceramic capacitor 6.3 V X5R | MuRata       | GRM188R60J47 5KE19D        | VBUS_PROT Decoupling                |
| C      | 2.2 $\mu$ F 0402 SMD Ceramic capacitor 6.3 V X5R | Kemet        | C0402C225M9P AC            | VBUS Decoupling                     |

## DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

|     |  |           |                       |                             |
|-----|--|-----------|-----------------------|-----------------------------|
| C   | 4.7 µF 0603 SMD Ceramic capacitor 6.3 V X5R          | MuRata    | GRM188R60J475KE19D    | DCIN_PROT Decoupling        |
| C   | 2.2 µF 0402 SMD Ceramic capacitor 6.3 V X5R          | Kemet     | C0402C225M9PAC        | DCIN Decoupling             |
| C   | 10 µF 0603 SMD Ceramic capacitor 10 V X5R            | Panasonic | ECJ-1VB1A106M         | VBAT Ball Decoupling        |
| C   | 10 µF 0603 SMD Ceramic capacitor 10 V X5R            | Panasonic | ECJ-1VB1A106M         | VCENTER Ball Decoupling     |
| C   | 2 x 10 µF 0603 SMD Ceramic capacitor 10 V X5R        | Panasonic | ECJ-1VB1A106M         | VDDOUT Decoupling           |
|     | <u>DA9053 XTAL</u>                                   |           |                       |                             |
| Y   | 32.768 kHz CC7VA SM Crystal 9 pF                     | Golledge  | CC7VA-T1A             | 32kHz XTAL                  |
| C   | 12 pF 0402 SMD Ceramic capacitor 50 V C0G            | MuRata    | GRM1555C1H120JZ01D    | 32kHz XTAL CAP              |
| C   | 12 pF 0402 SMD Ceramic capacitor 50 V C0G            | MuRata    | GRM1555C1H120JZ01D    | 32kHz XTAL CAP              |
|     | <u>DA9053 REF</u>                                    |           |                       |                             |
| C   | 0.1 µF 0402 SMD Ceramic capacitor 16 V X7R           | MuRata    | GRM155R71C104KA88D    | VREF1                       |
| C   | 2.2 µF 0402 SMD Ceramic capacitor 10 V X5R           | MuRata    | GRM155R60J225ME15     | VDD_REF                     |
| R   | 200 kΩ 0402 SMD chip resistor 1% 0.063 W             | Panasonic | ERJ2RKF2003x          | IREF                        |
|     | <u>DA9053 MISCELLANEOUS</u>                          |           |                       |                             |
| Q   | P-Channel CSP1.0 x 1.5mm                             | TI        | CSD25301W1015         | VBUS FET                    |
| Q   | P-Channel CSP1.0 x 1.5mm                             | TI        | CSD25301W1015         | DCIN FET                    |
| Q   | P-Channel SOT23                                      | Vishay    | Si2333DS              | System Load FET             |
| D   | Schottky diode 1 A 20 V SOD323                       | NXP       | BAT760                | Charger Buck Schottky Diode |
| BAT | Lithium Battery (rechargeable) ML414, 1.0 mAh, 3.1 V | Sanyo     | ML414, 1.0 mAh, 3.1 V | Backup Battery              |
| R   | 2.2 kΩ 0402 SMD chip resistor                        | Yageo     | RC0402FR-072K2L       | SO Pull-up Resistor         |
| R   | 2.2 kΩ 0402 SMD chip resistor                        | Yageo     | RC0402FR-072K2L       | SK Pull-up Resistor         |
|     |  |           |                       |                             |

## 11 Power Commander™ initialisation file for NXP™ i.MX 6 DualLite applications processor

Four standard OTP variants for the DA9053 have been produced (Table 4). These all support the configuration described in this application note. Variant DA9053-60 provides support for systems that wish to use an external wake-up event such as an nONKEY press to start the system. Variant DA9053-61 provides support for systems that wish to auto-boot as soon as power is applied. Variants DA9053-62 and -63 support the above two configurations where the system has no battery.

## DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

The initialisation files for these variants are available from the Dialog customer portal or via request to your local Dialog sales office.

The file DA9053-60\_iMX6DL\_1R2\_1D46.ini defines the DA9053 power-up sequence (Figure 4) and default configuration to power the NXP™ i.MX 6 DualLite applications processor.

**Table 4: DA9053 standard variants**

| Variant   | Battery | Autoboot |
|-----------|---------|----------|
| DA9053-60 | Y       | N        |
| DA9053-61 | Y       | Y        |
| DA9053-62 | N       | N        |
| DA9053-63 | N       | Y        |

## 12 Ordering information

To order the specific variants for this configuration, substitute the variant number (60, 61, 62 or 63) for the xx in the part numbered listed in Table 5.

Note other quantities are available through distribution channels.

**Table 5: DA9053 order codes**

| Part number  | Package                            | Shipment | Pack quantity |
|--------------|------------------------------------|----------|---------------|
| DA9053-xxC51 | 7 x 7 169-bump BGA Pb-free/green   | Tray     | 260           |
| DA9053-xxC52 | 7 x 7 169-bump BGA Pb-free/green   | T&R      | 3,000         |
| DA9053-xxHA1 | 11 x 11 169-bump BGA Pb-free/green | Tray     | 176           |
| DA9053-xxHA2 | 11 x 11 169-bump BGA Pb-free/green | T&R      | 2000          |

## 13 Suspend and Resume operation

The configuration described in this application note provides support for Suspend and Resume operation. The DA9053 uses the HW signal PMIC\_STBY\_REQ to enter a low power Suspend state. The regulators of the DA9053 can be pre-configured via SW to switch off, remain on or drop to a retention level during Suspend. The regulators are automatically reset to their power-up defaults when the Resume operation is triggered by a valid wake-up event. Application note 'AN-PM-007 Suspend and Resume.pdf' provides more details of this functionality.

## 14 Host communication

The DA9053 offers two options for communication between the host and the PMIC. The 4-wire (SPI) interface is the recommended option as it provides point to point communication without the potential for bus contention or increased latency. The DA9053 also supports a 2-wire interface that is generally compatible with I<sup>2</sup>C. For designs planning to use the 2-wire interface, especially where Suspend and Resume functionality is required, please review your implementation with a member of

## DA9053 / NXP™ i.MX 6DualLite Applications Processor Example Power Connections

the Dialog Applications Team as care must be taken with the allocation and control of the I/O rails to achieve the lowest power consumption in Suspend.

### 15 Additional supplies

The NXP™ SABRE board design utilises two additional 5 V rails. These are PMIC\_5V and AUX\_5V. These rails are provided by a boost convertor powered from the battery/input rail. These additional rails may be required depending on the system requirements. These rails need to be provided by an external boost convertor.

The DA9053 does not include a regulator capable of providing the peak current of the NXP™ SABRE board GEN\_3V3 rail. In the design described in this application note an external regulator has been used. This external regulator is sequenced by the DA9053 by using the GP\_FB2 signal to enable the external regulator. Depending on the current requirements for a particular design, it may be possible to use multiple LDOs from the DA9053 to provide the 3V3 rail. In larger designs, an external regulator may be required. For efficiency reasons it is recommended to select a suitably-sized buck regulator.

### 16 Battery-less operation

In the case of a system operating from either an external supply or from an external regulator supplied from a multi-cell battery solution, there are some additional optimisations that can be made, as follows:

- One of the two variants designed for battery-less operation should be used
- The 5 V rails should be provided directly from the input supply to eliminate the requirement of an external boost
- The DA9053 Charger Buck can supply ~1.9 A to the VDDOUT rail. Care should be taken not to overload this rail
- To reduce the load on VDDOUT and possibly improve efficiency, the external buck chosen for the GEN\_3V3 rail can be powered directly from the input supply. This regulator would still be sequenced via the use of the GP\_FB2 enable signal
- Further efficiency could be gained by supplying some of the LDOs from a buck. This could be either one of the DA9053 Bucks or the external buck providing GEN\_3V3.

### 17 Driver support

The Linux drivers for the device are provided as part of a BSP patch release from Dialog Semiconductor.

This release patches an existing Android BSP for the NXP™ MCIMX6DL-SDP platform with support for a Dialog DA9053 power management and audio IC.

The driver supports provide features of the device within the standard frameworks offered by the Linux kernel. Please refer to the MCIMX6DL-SDP DA9053 BSP documentation for more information on the requirements and dependencies.

This driver release for the MCIMX6DL-SDP DA9053 BSP was based upon an existing Linux kernel driver for the DA9052/3 PMIC. The latest version of this driver is found in the Linux kernel.

For more detailed advice on support for your particular configuration please contact your local Dialog sales office.

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### 18 Additional collateral

For a DA9053 / i.MX 6DualLite design, this document is supplemented by the following information:

- DA9053 Configuration Schematic (44-179-115-09-B1.pdf): this schematic shows the required connectivity for the DA9053 and is effectively a replacement for the PMIC page of the NXP™ SABRE board schematic. All of the required connections have been named to match the net names on the NXP™ schematic.
- DA9053 Reference Board: schematic and reference layout

These documents, along with additional application notes and design guides, are available from the Dialog customer portal which is accessible from the [Dialog web site](#). Please contact your local Dialog Applications representative for details.

### 19 Conclusions

This application note has detailed one possible configuration for the DA9053 PMIC to support the NXP™ i.MX6 DualLite applications processor. This configuration closely matches the NXP™ SABRE board design.

With its highly configurable design, the DA9053 is well suited to nearly all applications of the i.MX6 DualLite processor.



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**DA9053 / NXP™ i.MX 6DualLite Applications**  
**Processor Example Power Connections****Revision history**

| Revision | Date        | Description                                    |
|----------|-------------|--|
| 0.1      | 24-Oct-2013 | Initial version.                               |
| 1.0      | 08-Oct-2015 | Update to latest template. Minor text updates. |
| 1.1      | 18-Feb-2016 | Minor text updates.                            |
|          |             |  |

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### Status definitions

| Status                  | Definition   |
|-------------------------|--|
| DRAFT                   | The content of this document is under review and subject to formal approval, which may result in modifications or additions. |
| APPROVED<br>or unmarked | The content of this document has been approved for publication.  |

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