An Ultra Low-Power Non-Volatile Memory Design Enabled By Subquantum Conductive-Bridge RAM

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***Abstract*—Conductive-bridge RAM (CBRAM) memory cells offer speed, voltage, and energy advantages over floating gate flash cells. Here, we describe a memory design which carries these cell-level advantages up to the product level, achieving 100x lower read and write power and 10x lower standby power than typical flash-based designs.**

***Index Terms*—Non-volatile memory, resistive memory, RRAM, Conductive-bridge RAM, CBRAM, low power, ultra low-power, Internet of Things, IoT**

I. Introduction

In power-starved applications, such as Internet of Things (IoT) [1, 2] applications relying on small batteries and energy harvesters, every component of a system must take power consumption into consideration. For non-volatile memory chips, this includes all three basic modes of operation—read, write, and standby. Unfortunately, the underlying physics of flash memory cells necessitates the use of high voltages and/or long pulses (see Table I). This makes power-hungry circuits (*e.g.*, charge pumps) unavoidable and the use of some power-saving design techniques more difficult [3]. In contrast, RRAM cells operate by physical mechanisms which are inherently low-voltage, high-speed, and low-energy [4-6]. The emergence of RRAM technologies thus promises to enable power-efficient memory designs not feasible in the past [3].

We describe here an ultra low-power non-volatile memory design based on the type of RRAM called conductive-bridge RAM (CBRAM) [4, 7]. The present design, like similar designs based on CBRAM or RRAM, is ideally suited for power-starved applications, such as those of the IoT.

II. Power & Performance Advantages of CBRAM

A vast literature on RRAM technologies has been generated over the past decade (e.g., see review articles [4-6]). The innate speed, voltage, and energy advantages of RRAM cells are well documented, and commercialization efforts have been concerned largely with reliability (e.g., high-temperature retention) and manufacturability considerations (e.g., "fab friendliness" of the materials). For CBRAM, significant progress has been made on the fundamental tradeoff between reliability and power through the development of cells whose filaments comprise a semiconductor or semimetal instead of a metal [8]. By virtue of their physically thicker filaments, this new class of CBRAM cells (so-called "subquantum" CBRAM) provides improved ON-state (i.e., low-resistance state) retention characteristics compared to CBRAM cells utilizing "traditional" filament metals such as Cu or Ag, without sacrificing the advantages that CBRAM cells hold over floating gate flash cells (see Table I).

TABLE I. Representative Values of Performance and Power Parameters for CBRAM Cells vs. Flash Memory Cells

	CBRAM[a]	**Floating Gate Flash[b]**
Read voltage	~ 0.1 V	0.7 V
Program voltage	1-3 V (anode)	|6|-|9| V (word line)
Program time	0.01-0.1 µs/cell	1-10 µs/cell
Program energy	0.1-10 pJ/cell	1000 pJ/cell
Erase voltage	1-2 V (cathode)	|6|-|9| V (word line)
Erase time	0.01-0.1 µs/cell	1 ms/cell
Erase energy [pJ/cell]	0.1-10 pJ/cell	1000 pJ/cell

a. See Refs. [4, 8].
b. See, e.g., Ref. [3, 9].

III. Designing CBRAM into Power-Starved Systems

The present design utilizes subquantum CBRAM cells in a 1T1R architecture, fabricated in the back end of a 130 nm Cu logic process. Three general types of power-saving techniques are made possible, or at least facilitated, by the use of these CBRAM cells. One involves using existing system-level circuitry to eliminate redundant circuits inside the memory chip, thereby increasing overall system efficiency. The second targets a decrease in leakage current by intelligently managing the number and type of devices receiving power. The third leverages the tradeoff between speed and power, taking advantage of any relaxed timing requirements the application may allow. These techniques are applied across all operating modes of the chip, as described below.

A. Read mode

A "Thing" of the IoT [1, 2] might be viewed generically as a system comprised of a sensor (or sensors), a µ-controller, a communications module, a memory, a power control unit, and a power source or sources. The present design assumes that

three system-wide power supplies will be available, operating at voltages typically found in such systems. A power gate (Fig. 1) is used to route the three supplies to the appropriate parts of the present chip. For the read circuitry, it is assumed that a 1 V power supply (VDD_{CORE} in Fig. 1) will be available from a core digital voltage. Since the voltage required to read a 1T1R CBRAM array is no more than 1 V for the wordline (WL) and the peripheral logic circuit can operate at 1 V as well, this eliminates the need for an on-chip regulator from VDD_{IO} and saves the quiescent current that would have been lost.

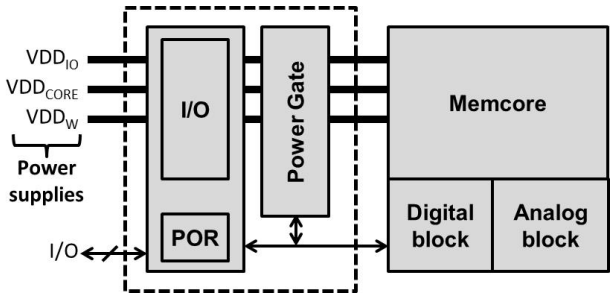

Fig. 1. Power island topology utilizing three system-wide power supplies controlled by a power gate. VDD_{CORE} (0.97-1.03V) powers the read circuitry and digital logic. VDD_{IO} (1.65-2.7V) is used for SPI communications and the POR circuit. VDD_W (3.6-4.4V) is used only for write circuitry, and draws nearly zero current during read and ultra-deep power-down (UDPD) standby mode. Dashed line encloses portion of chip left powered while in UDPD standby.

With an ON-state (i.e., low-R) resistance of 100 kΩ or less, a current sufficient for a fast read (e.g., less than 100 ns) can be generated from a CBRAM cell using a bitline voltage on the order of just 0.1 V. Such a low bitline voltage, combined with a low wordline voltage, results in a low bias current for read, which enables the read bias circuits to be turned on and off quickly. The present design exploits this characteristic by powering down the read bias circuitry in between read bursts. As shown in Fig. 2, a 128-bit block of data is read into a buffer. Most of the internal circuitry is then disabled as the data is shifted out to the SPI bus. In doing so, clock gating is utilized to limit the switching of the circuits in the read path. Through these techniques, the current drawn by VDD_{CORE} was measured to be just 4-5 µA for a read bandwidth of 500 kbit/s, or 8-10 µA/Mbps.

B. Write mode

The write circuitry of the present design is driven by a 3.6-4.4 V power supply (VDD_W in Fig. 1). The voltage requirement of CBRAM cells is low enough that a write operation can be performed without having to boost the write power supply. As with read, this avoids the area and power penalties of the charge pumps required by flash memory.

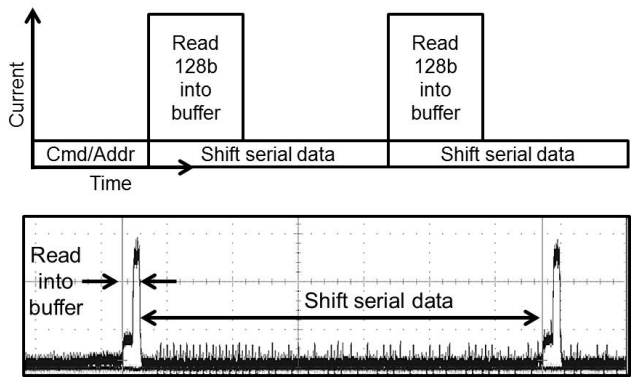

Fig. 2. Timing diagram of the read operation, and an example measurement of the core supply current during read.

In addition, the fast write speed of CBRAM cells allows active regulation of a write voltage to be eliminated. Instead, a small on-chip capacitance is charged up to the desired voltage prior to a program operation (i.e., high to low resistance), then exposed to the cell by the access transistor (see Fig. 3). The fast write speed of the cell allows the program operation to be completed within the time constant of the capacitive discharge, avoiding the need to continuously pump the capacitor. An erase operation (i.e., low to high resistance) is performed in an analogous way.

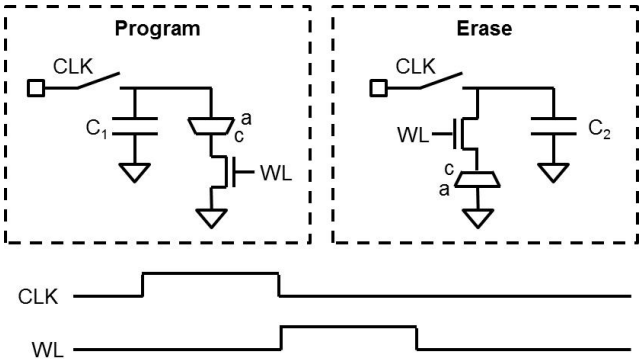

Fig. 3. Circuit diagrams depicting the capacitive write technique in which a cell is programmed/erased by the transient discharge of a small on-chip capacitance. The anode and cathode of the CBRAM cell are denoted "a" and "c," respectively.

This capacitive write technique is carried out within a write-sleep-write scheme wherein the write circuit is powered down in between write bursts (see Fig. 4). The average power and current consumed during write is then determined by the write frequency. Such a scheme is made more efficient by the use of CBRAM cells, as their fast write minimizes the portion of a write-sleep cycle that must be spent writing. For a write bandwidth of 10 kbit/s, these techniques combine to yield a write current (on VDD_W) measured to be just 1-5 µA, or 100-500 µA/Mbps.

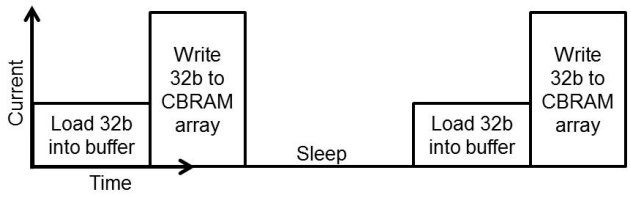

Fig. 4. Timing diagram of write operation.

C. Ultra-deep power-down (UDPD) standby mode

Power consumption due to leakage current is of particular concern for applications in which a system must sit idle for extended periods of time, as may be true in many IoT sensing applications. To combat this, the present design utilizes the power island topology shown in Fig. 1. Besides providing for efficient control of the power supplies during read and write, the power gate makes an ultra-deep power-down (UDPD) standby mode possible by allowing the entire memory core (including peripheral digital and analog blocks) to be powered down.

While in UDPD standby mode, only the minimal circuitry of the power-on reset (POR) circuit remains active. The POR circuit uses a power supply available from the system (VDD_{IO}), again avoiding the power loss due to the quiescent current of "redundant" regulating circuitry. The current consumed by each of the three power supplies while in UDPD standby mode was measured to be on the order of nanoamps, as shown in Fig. 5.

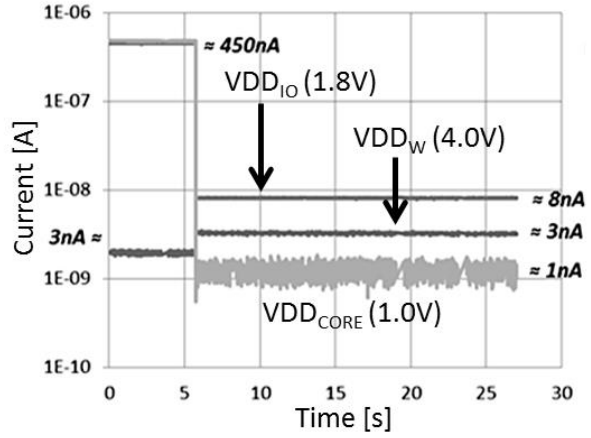

Fig. 5. Current profiles of supplies as chip enters ultra-deep power-down (UDPD) standby from regular standby (450 nA). In UDPD standby, none of the power supplies draws more than a few nanoamps of current.

Though the UDPD standby mode can be used with any memory technology, including flash, it is made even more effective by the use of CBRAM, as the low voltage requirements of CBRAM reduce the time delay and power consumption associated with wake-up. To minimize the in-rush current during wake-up, the power gate of the present design turns on the three power supplies one at a time. The impact on the input power is short-lived, averaging 2.8 mA over the first 500 ns, as shown for VDD_{IO} for example in Fig. 6. This causes just a small drop in the voltage ($I_{ave}\Delta t/C$=14 mV) across the 100 nF stabilizing capacitor at the supply input. The corresponding voltage drops for VDD_{CORE} and VDD_W are 130 mV and 5 mV respectively.

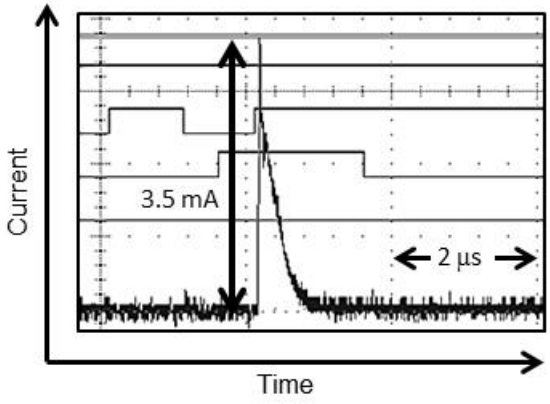

Fig. 6. In-rush profile of VDD_{IO} measured during wake-up from UDPD standby. The in-rush current was measured by monitoring the voltage drop across a 220 Ω resistor placed between the 100 nF stabilizing capacitor and the chip input of VDD_{IO}. The 220 Ω resistor is not present during normal operation.

As summarized in Table II, the low voltages and high speeds at which CBRAM cells can be read and written gives the present design a 100x reduction read/write power compared to typical flash-based designs. Likewise, the ultra-deep power-down mode, facilitated by the low voltage requirements of CBRAM, provides a 10x reduction in power consumption compared to typical standby modes in flash-based designs.

TABLE II. AVERAGE POWER CONSUMPTION OF PRESENT CBRAM-BASED DESIGN COMPARED TO TYPICAL FLASH-BASED DESIGNS

Mode	CBRAM (present design)	Flash (typical)
Read (500 kbit/s)	VDD_{IO} (1.8V): 1-2 µA VDD_{CORE} (1.0V): 4-5 µA VDD_W (4.0V): < 35nA **Total Power: 6-9 µW**	VCC (1.8V): 1.0 mA **Total Power: 1.8 mW**
Write (10 kbit/s)	VDD_{IO} (1.8V): 1 µA VDD_{CORE} (1.0V): 3 µA VDD_W (4.0V): 1-5 µA **Total Power: 9-25 µW**	VCC (1.8V): 12 mA **Total Power: 20-25 mW**
UDPD Standby	VDD_{IO} (1.8V): 8 nA VDD_{CORE} (1.0V): 1 nA VDD_W (4.0V): 3 nA **Total Power: 27 nW**	VCC (1.8V): 150-200 nA **Flash: 270-360 nW**

IV. Conclusions

The present design illustrates how the use of CBRAM, coupled with appropriate low-power design techniques [10], can yield memory chips ideal for applications with strict power budgets. Though relatively few reports of ultra low-power circuit design for CBRAM- or RRAM-based systems have been published to date (e.g., [11]), the authors expect such reports to increase in frequency in the coming years due to the increasing maturity and availability of CBRAM and other RRAM technologies.

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