

# **Application Note**

## **CCE4502**

### **IO-Link Functionality**

## IO-Link Functionality

### 1 Overview

The CCE4502 comprises a versatile frame handler for the IO-Link™ protocol as specified in the „IO-Link Interface and System“ Specification Version 1.1.2, July 2013.

The frame handler's functions include

- Status signaling via the STAT register and the SPI status byte
- Automatic CRC checking of the master message with indication via STAT register and the SPI status byte
- Automatic CRC generation and replacement in the CKS byte at the end of each device message
- Maskable interrupt flags for different timeouts, start of transmission, start of receiving, framebuffer level, and completed reception of a master message (see registers INT\_EN\_FH and INT\_SRC\_FH)
- Maskable interrupt flag for automatic wake-up request detection in SIO mode (see registers INT\_EN\_SIO and INT\_SRC\_SIO)
- Device message transmission with automatic timing based on COM mode configuration

### 2 Example flow

In the following example a flow is presented which uses the functionalities of the CCE4502 to reduce the complexity of the microcontroller unit (MCU) software. The flow can be altered to meet the needs of the application. We assume that the MCU is connected to the CCE4502 via SPI and is also connected to the INTX pin of the CCE4502.

After powering on the system the MCU should configure the CCE4502:

- Register CONF1: SIO mode, push-pull
- Registers FHC, TRSH: adapt to your requirements
- Register INT\_EN\_SIO: Enable WURQ detection interrupt by setting WURQ\_EN

This will allow the CCE4502 to send an interrupt request (IRQ) when a wake-up request is detected. The configuration of the registers ODL, MPDL and DPDL are ignored for messages of type 0. Since the first messages from the master will be of type 0 the registers can be configured later during the configuration phase.

If a wake-up request is detected the interrupt service routine (ISR) of the MCU has to

- Re-configure the CONF1 register to the frame handler mode and the desired COM mode, and
- Enable the frame handler interrupts in register INT\_EN\_FH.

The device is now ready to receive and transmit messages using the frame handler. The message type registers (ODL, MPDL, DPDL) have to be configured during the configuration phase of the IO-Link communication to match the desired message type.

According to the M-sequence control (MC) octet and the message type registers the CCE4502 will automatically detect the start of receiving a master message and will indicate its end using the interrupt INT\_SRC\_FH.MSG. This should trigger an ISR in the MCU which reads the message from the buffer FHD and writes a proper device message to the buffer FHD, including the device CKS byte. The six least significant bits of the CKS byte are automatically replaced with the compressed checksum. Optionally, the frame handler state can be read from the STAT register or the SPI status byte to determine the results of the CRC check.

The example flow is depicted in Figure 1.

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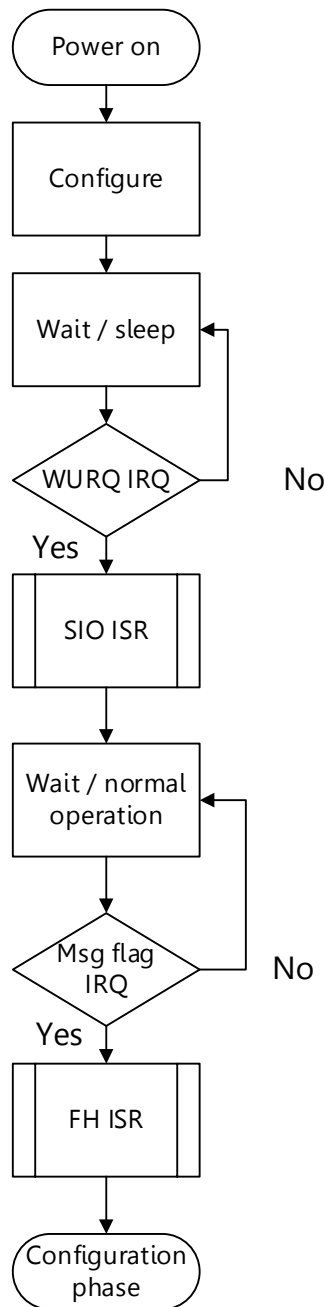


Figure 1: Example MCU flow in combination with the CCE4502

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### 3 Revision History

| Revision | Date        | Description   |
|----------|-------------|---|
| 1.2      | 1-Nov-2019  | Updated Template  |
| 1.1      | 09-Aug-2017 | Clarified transition to configuration phase, message type configuration and CKS byte substitution |
| 1.0      | 27-Jul-2017 | Initial version   |

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