Application Note

CCE4502

General Application Note

1 Preface

The CCE4502 transceiver is suitable for I/O Link Device applications and is compliant with the IO-Link Interface and System specification Version 1.1.2 from July 2013 accessible via www.io-link.org. This application note contains information complementary to the CCE4502 product specification and is subject of permanent improvement. Please consult the CCE4502 product specification for most recent and detailed information.

2 Typical Application

Typical applications of the CCE4502 include IO-Link enabled sensors or actors.

The IO-Link interface can provide power for the CCE4502 and other circuitry of the application, such as microcontrollers and sensor or actuator controlling circuit.

The first channel of the CCE4502 controls the IO-Link CQ line. A second channel is available to drive an optional in- or output for compatibility with a wide range of communication interfaces.

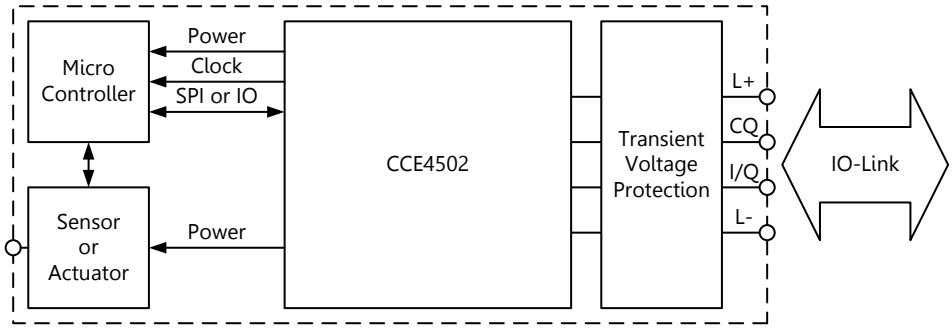

Figure 1: Typical Application – I/Q optional

In general, a microcontroller is required for IO-Link Device applications, albeit the IO-Link Framehandler of CCE4502 reduces the MCU load of the external microcontroller. The microcontroller needs to interface the sensor or actuator and provide data requested by the IO-Link interface of the CCE4502.

3 Power supply

The IC is supplied by 9V to 36V between L+ and L- pins. An internal protection circuit prevents damage to the CCE4502 if power is applied in reverse polarity. Thus, the pin VSS serves as the reference ground for all pins except L+ and L-. Connecting L- and VSS will tamper the reverse polarity protection function.

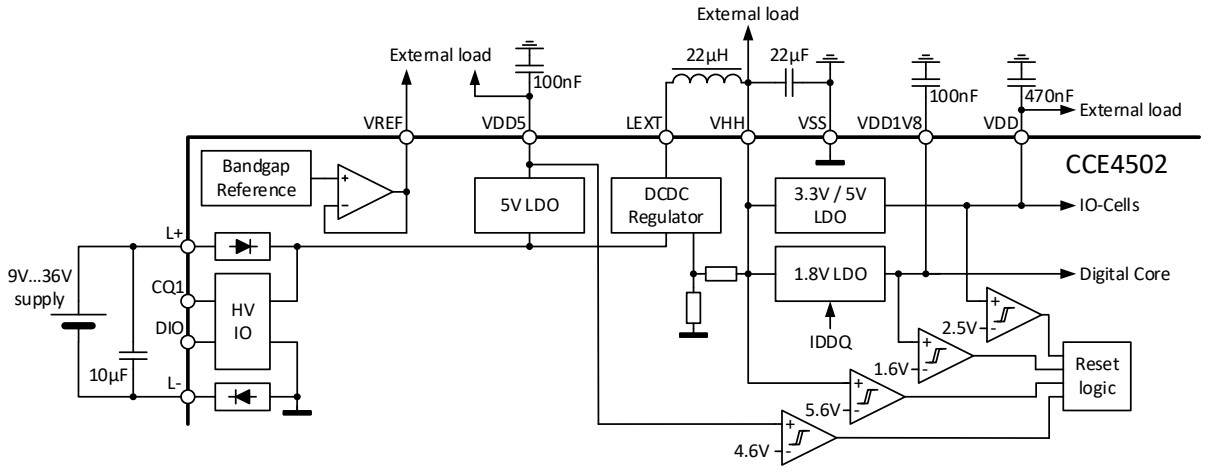

Figure 2: CCE4502 power supply block diagram

The CCE4502 integrates several regulators to provide internal and external supply voltages:

1. A 5V output voltage LDO at pin VDD5 providing up to 10mA.
2. DC/DC regulator provides 7V at pin LEXT providing up to 50mA.
3. A factory programmed regulator, which provides 3.3V or 5V up to 50mA.
4. A 1.8V LDO to supply internal logic, no external load allowed.
5. A 1.2V reference voltage output can provide up to 100uA load current.

The DC/DC regulator also provides the input voltage for the 3.3V/5V LDO, do not draw more than 50mA from both regulators together.

Thermal capabilities of the device and PCB limit the current driving capability of the regulators.

3.1 VDD5 – 5V LDO

A constant 5V is available at VDD5. This pin can drive a maximum load current of 10mA. A 100nF capacitor to VSS is required at this pin, even if no external load is connected.

3.2 DC/DC regulator

A DC/DC regulator is available to generate a 7V output voltage at VHH from the supply. The voltage at VHH serves as input to the 3.3V/5V and 1.8V LDO.

The DC/DC regulator runs in either linear regulation or buck regulation mode. The regulation mode of the DC/DC regulator is factory programmed into the CCE4502. Consult the product specification for corresponding order codes!

Always check the power budget to select the DC/DC regulator option suitable to your design.

3.2.1 Buck Mode

The buck regulation mode improves the efficiency of the CCE4502 and allows limiting the on chip power dissipation at the cost of additional external components. In buck regulation mode, the following external components are required:

1. 22µH inductor from LEXT to VHH.
2. 22µF low ESR capacitor from VHH to VSS.
3. 10µF capacitor from L+ to L-.

In buck mode, the DC/DC regulator switches at a frequency of 2.0MHz (±500kHz). This clock is generated internally.

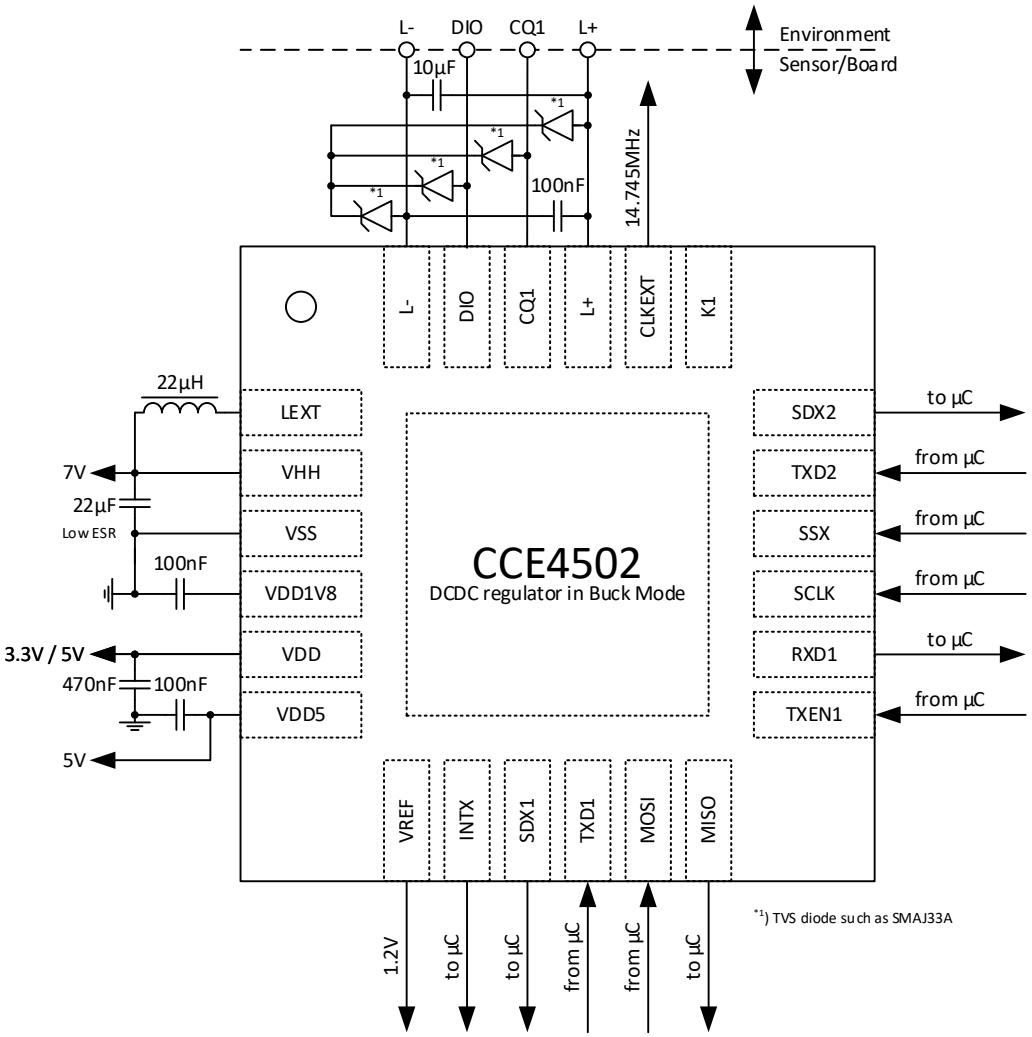

Figure 3: Application schematic with DC/DC in Buck Mode

3.2.2 Linear Mode

In linear regulation mode, the pins LEXT and VHH have to be connected externally. A 100nF capacitor from VHH to VSS is required for a stable 7V output voltage.

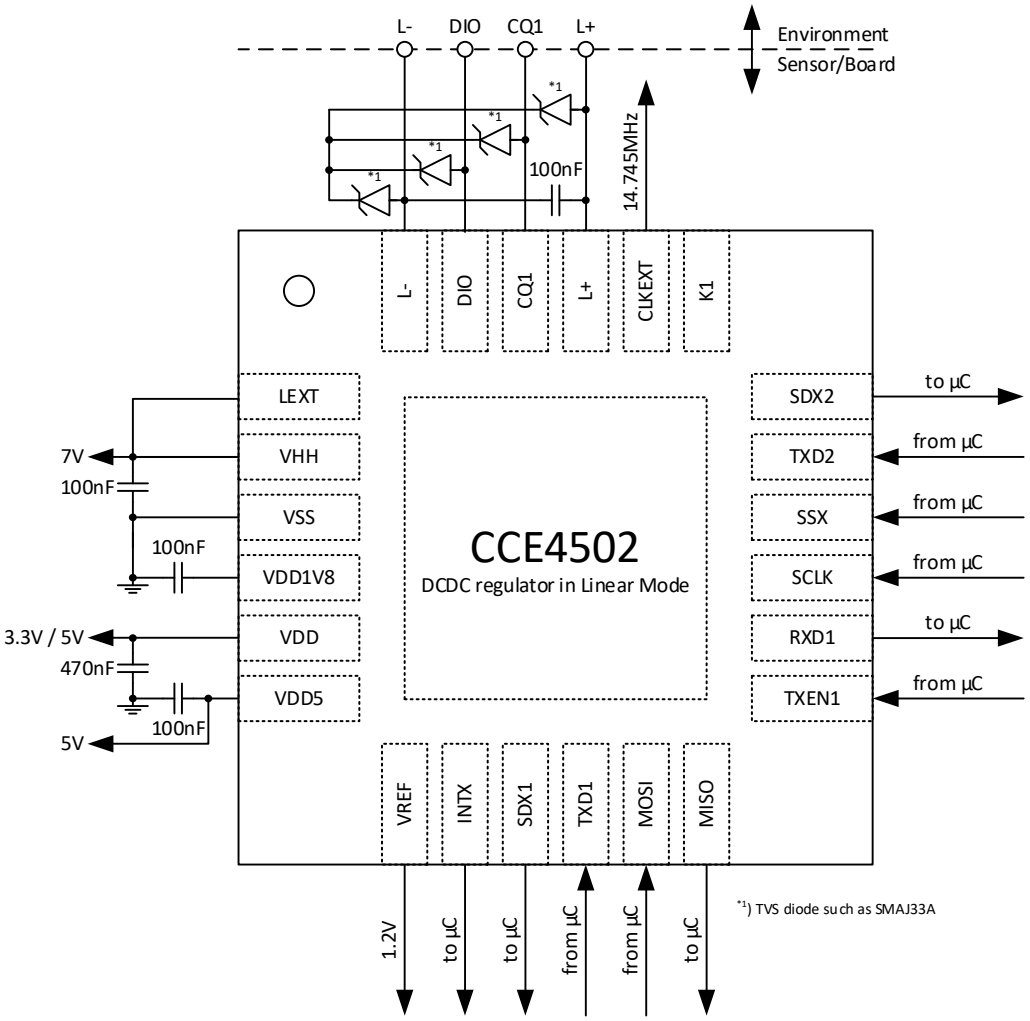

Figure 4: Application schematic with DC/DC in Linear Mode

3.2.3 External Supply

If neither the buck regulator mode nor the linear regulator mode can be used, an external 6V to 36V supply must be connected to VHH. A 100nF capacitor is recommended from VHH to VSS. Leave LEXT unconnected.

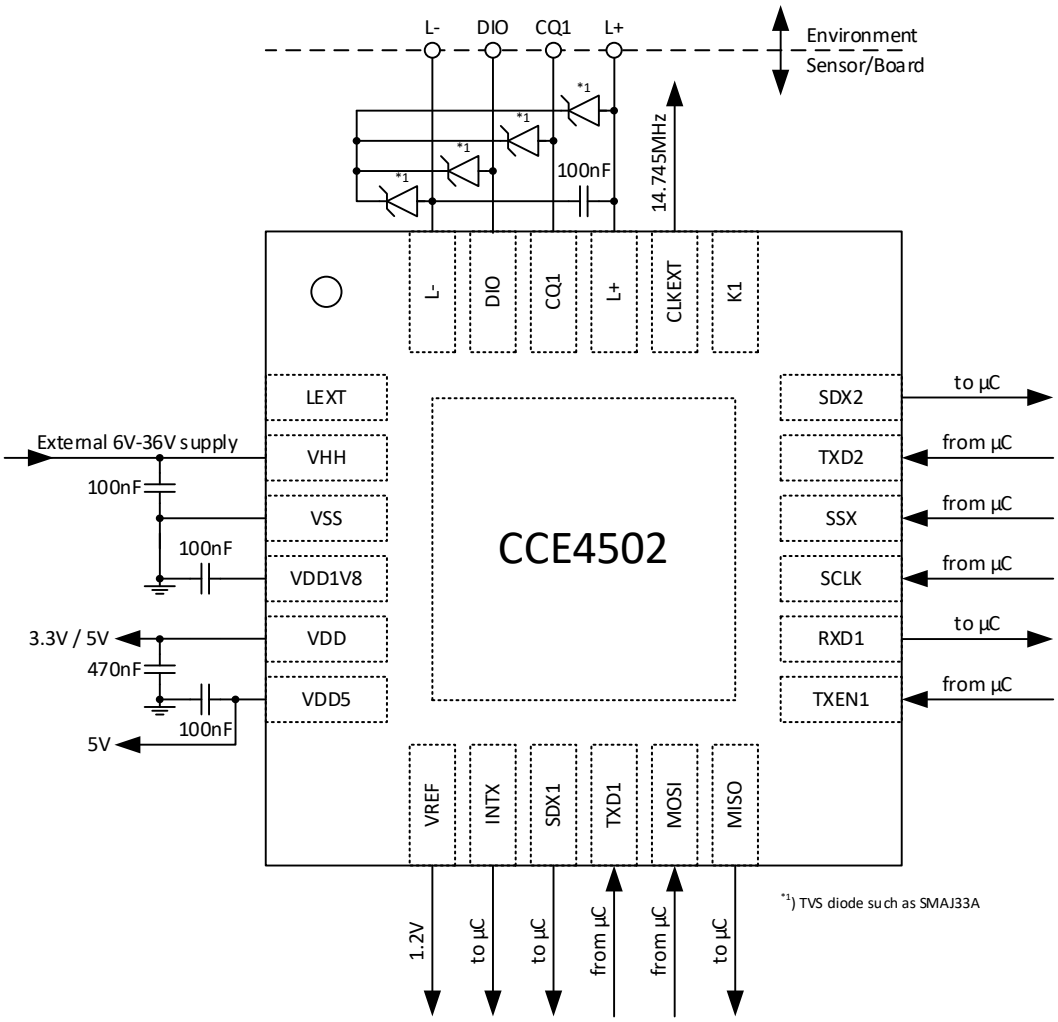

Figure 5: Application schematic with DC/DC bypassed

3.3 VDD – 3.3V/5V LDO

The output voltage of the LDO at pin VDD is factory programmed. Consult the product specification for corresponding order codes! A 470nF capacitor is required between VDD and VSS for a stable output voltage. All digital IOs (INTX, SDX1, TXD1, MOSI, MISO, TXEN1, RXD1, SCLK, SSX, TXD2, SDX2, K1, CLK_EXT) are supplied by this voltage, thus defining their input threshold and output voltage.

External circuitry can be supplied by this LDO. Up to 50mA can be drawn. Keep in mind, that the maximum load current at VHH and VDD must not exceed 50mA in total.

3.4 VDD1V8 – 1.8V LDO

This output voltage is fixed to 1.8V and is used by internal logic of the IC. A 100nF capacitor is required between VDD1V8 and VSS.

4 Clock

A calibrated internal 14.7456MHz (±2%) oscillator provides the system clock used by the core logic. This clock signal is available at the CLK_EXT pin of the IC if the pin K1 is connected to VSS or left open.

If an external clock is required, connect a 14.7456MHz clock source to CLK_EXT and connect K1 to VDD. An absolute accuracy of ±3% or better is required for proper IO-Link communication. If VDD is programmed for 3.3V output voltage, a 3.3V CMOS clock signal is required at CLK_EXT. Hence, a 5V CMOS clock signal is required at CLK_EXT, if VDD is programmed for 5V output voltage.

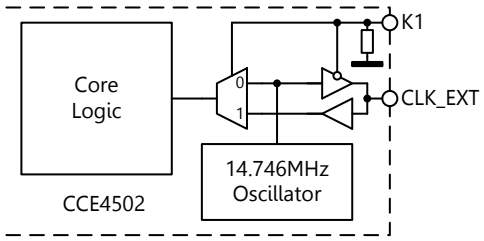

Figure 6: Clock system

5 µC Interface

Two interfaces are available to control the CCE4502, depending on the target application

5.1 Logic IO-Interface

The pins TXEN1, SDX1, TXD1, RXD1, TXD2, SDX2 allow direct access to the channel1 (CQ1) in/output and the channel2 (DIO) output. By using these pins only, all IO-Link protocol handling has to be implemented in the externally connected MCU. However, this allows using the CCE4502 as a simple levelshifter from 3.3V/5V logic signals to IO-Link compliant levels.

5.2 SPI

The SPI (SSX, SCLK, MOSI, MISO and INTX) interface can be used to control the channel1 (CQ1) and channel2 (DIO) in and outputs. It allows to access internal supervisor circuitry, such as the over temperature, overvoltage detector and output overcurrent protection.

Furthermore IO-Link communication is eased by the on chip logic (Framehandler, Wakeup detect). So the computation overhead for the external MCU is reduced.

6 Power Budget

The ability of conducting heat from the chips core to the environment (thermal resistance) and highest allowable chip (junction) temperature limit the maximum power dissipation the CCE4502 can handle.

To minimize the temperature gradients at the chip, the total power dissipation is limited to 1W, see Absolute Maximum section of the product specification.

Keep in mind, that the internal temperature detection will flag over temperature at Tj=(120±10) °C.

System assembly, PCB layout and package determine the thermal resistance (R_{thj-a}) from junction to ambient of the IC measured in K/W. For the QFN24 package, by connecting the exposed pad to a copper plane at the backside of the PCB using thermal vias, good thermal coupling is possible. A junction to ambient thermal resistance of 40K/W can be achieved for the QFN24 4x4 package. System assembly will influence the R_{thj-a}, like free airflow at the PCB vs. thermal isolation of the PCB when assembled in the final product.

Calculate the junction temperature as follows:

$$T_j = T_a + R_{thj-a} \cdot P_D$$

Assuming ambient temperature (T_a) of 105°C, an R_{thj-a} of 40K/W and 1W of dissipated power (P_D) inside the chip, the junction temperature (T_j) will rise to 145°C.

The on-chip power dissipation of the CCE4502, hence the junction temperature, is influenced by:

1. Input voltage.
2. External load currents at the regulator outputs and digital IOs.
3. Operation mode of the DC/DC regulator.
4. Output current at CQ1 and DIO.
5. Internal power consumption.

Use the “CCE4502 Power Budget” Excel sheet to calculate the total on chip power dissipation:

CCE4502 Power Budget				
Supply Voltage				
Supply Voltage	24,0 V			
Static output current at CQ1	200,0 mA		Power at channel 1	80,0 mW
Static output current at CQ2	200,0 mA		Power at channel 2	80,0 mW
Internal current at supply	3,0 mA		Internal circuitry at supply	72,0 mW
VDD5 (5V) Regulator				
VDD5 external current	0,0 mA		VDD5 regulator	17,1 mW
VDD5 internal current	0,9 mA		Internal at VDD5	4,5 mW
DC/DC Regulator				
DC/DC Operation mode	Buck		DC/DC-Regulator	0,9 mW
DC/DC Buck Mode efficency	90%			
External Voltage at VHH	36,0 V			
External current at VHH	0,00 mA			
VDD (3.3V/5V) regulator				
VDD output voltage	5,0 V		VDD regulator	0,2 mW
External current at VDD	0,0 mA			
Internal current at VDD	0,1 mA		Internal circuitry at VDD	0,5 mW
VDD1V8 (1.8V) Regulator				
VDD1V8 external current	0,0 mA		VDD1V8 regulator	5,2 mW
VDD1V8 internal current	1,0 mA		Internal at VDD1V8	1,8 mW
Total				
Ambient Temperature	105 °C		On-Chip power dissipation	262,2 mW
Thermal Resistance (j-a)	40,0 K/W		Junction Temperature	115 °C

Figure 7: Screenshot of Power Budget Calculator

7 Reference Schematic

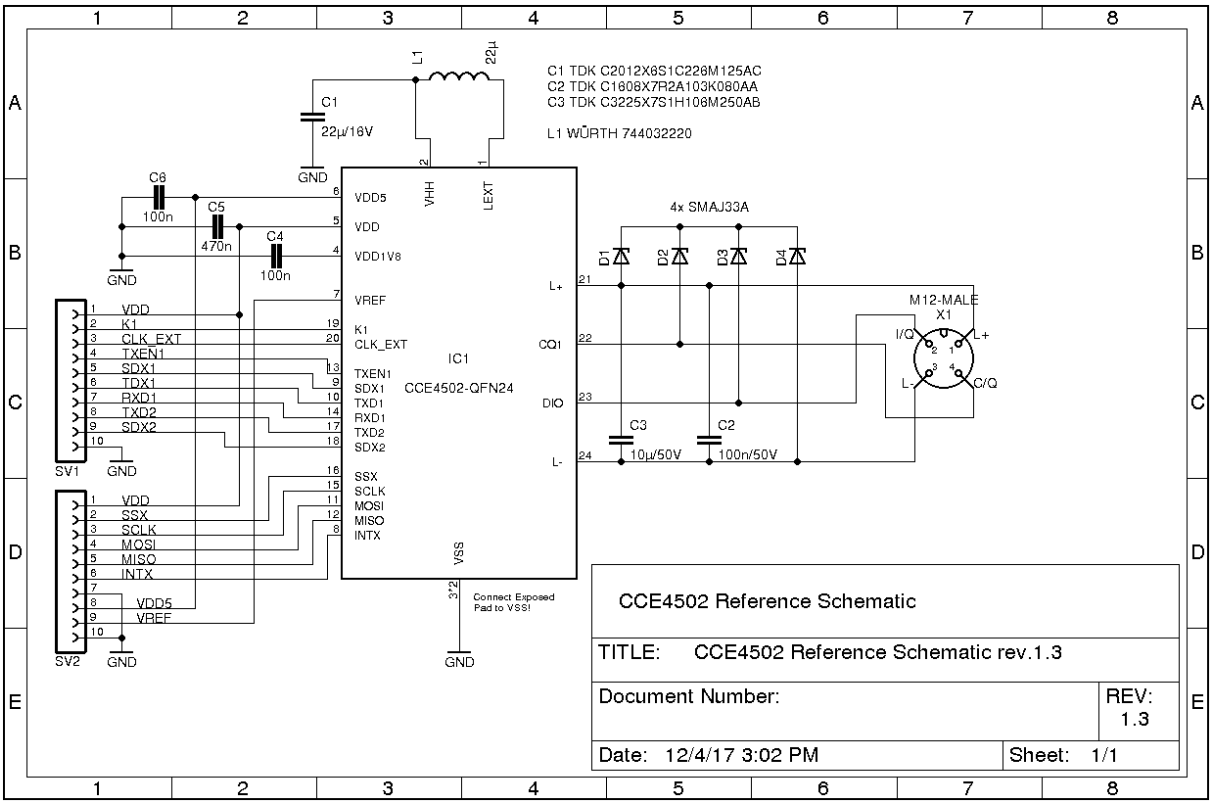

Figure 8: CCE4502 IO-Link Device Reference Schematic

8 Revision History

Revision	Date	Description
1.5	01-Nov-2019	Updated Template
1.4	04-Dec-2017	Update of application schematics
		Replaced capacitor LP/VSS with LP/LM
		Removed Reference PCB layout
1.3	15-Nov-2016	In line with spec
1.2	17-Oct-2016	Fixed PCB layout view
1.1	12-Sep-2016	Fixed VHH input voltage in bypass mode
1.0	07-Sep-2016	Initial revision

Content

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