DA7212 stereo CODEC with enhanced automatic level controller and 1.2W speaker driver

GENERAL DESCRIPTION

DA7212 is a high performance, low-power audio codec with an enhanced hybrid ALC and a powerful speaker driver targeting portable and embedded applications. The audio front-end simultaneously supports stereo FM line input with four analogue (or two analogue and two digital) microphones with two independent microphone biases. Comprehensive analogue mixing and bypass paths to the output drivers are available.

The headphone output is true-ground Class-G with integrated charge pump. There is also a differential Class AB speaker driver that can serve as a mono lineout.

Digital audio transfer to/from the external processor is via a bidirectional I2S interface that supports all common sample rates. The device may be operated in slave or master modes using the internal PLL which may be bypassed if not required.

To fully optimise each customer application, a range of built-in filtering, equalisation and audio enhancements are available. These are accessible by the processor over the I2C serial interface and can be used to minimise latency and power consumption.

DA7212 chip: WLCSP34, with a staggered 0.5mm pitch

KEY FEATURES

- 100dB stereo audio playback into 16-32 ohm headphones
- 67mW headphone driver into 16Ω at 2.5V;
    - Minimal external components: a capless, true-ground driver eliminates bulky headphone coupling capacitors
- 1.2W mono speaker driver
- 3.1mW quiescent power consumption for DAC to headphone playback
- Single supply operation
- Stereo digital microphone support
- Supports up to four microphones with two separate low-noise microphone-bias outputs
- Low-power PLL provides system clocking and audio sample rate flexibility
- Built-in 5-band equaliser, ALC and noise-gate functions
- Built-in beep generator that outputs all DTMF keypad values, as well as mixing two independently configurable sine waves between 10Hz and 12kHz
- 34-ball WLCSP (4.54mm x 1.66mm) package
- Staggered 0.5mm pitch for easy PCB routing

APPLICATIONS

- Personal Media Players
- Audio headphone/headsets
- Wearables
- Embedded applications
- Arduino compatible development systems

SYSTEM OVERVIEW

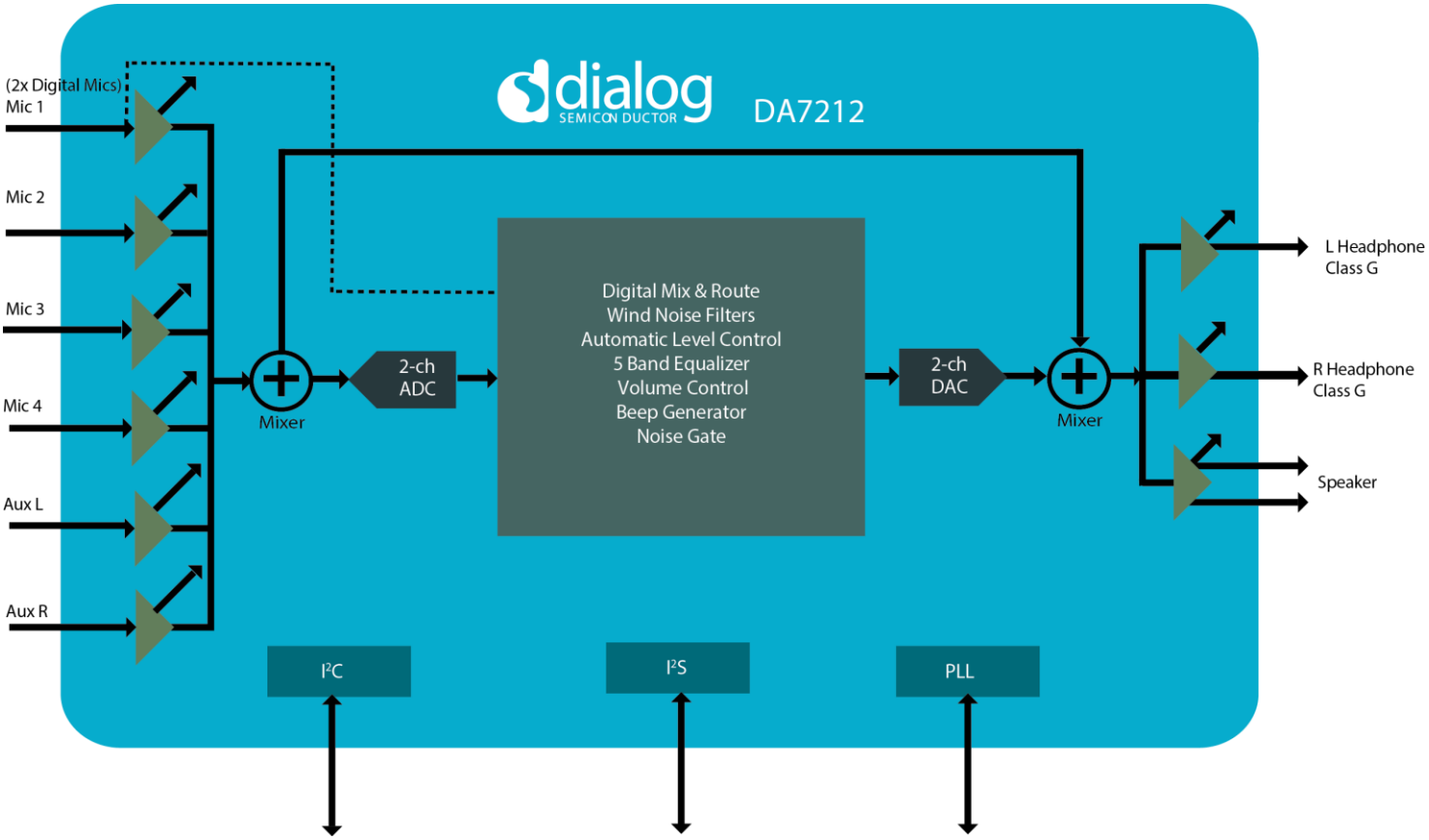

Figure 1: Component values shown for a typical application

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POWER SUPPLY BLOCKS

Audio Parametrics

Analogue to Digital Converter (ADC)

PARAMETER	SYMBOL	TEST CONDITIONS	Min	Typ	Max	UNIT
Full-scale input signal	V_{MAX}	Digital output level = 0dBFS		1.6 × VDDA		V_{PP}
Signal to Noise Ratio	SNR[2]	A-weighted no input selected		90		dB
Total Harmonic Distortion plus Noise	THD+N[3]	-1dBFS 44.1kHz slave mode		-85		dB
		-1dBFS 32kHz PLL mode		-80		dB
In-band Spurious		Analog input level = 0dBFS		-85		dB
Channel separation				90		dB
Pass band	B_{PASS}				0.45*Fs	Hz
Stop band	B_{STOP}	Fs ≤ 48kHz Fs = 88.2/96kHz	0.56*Fs		7*Fs 3.5*Fs	Hz
Pass band Ripple		Voice mode Music mode			±0.3 ±0.1	dB
Stop band Attenuation		Voice mode Music mode	70 55			dB
Group delay		Voice mode Music mode Fs = 88.2/96kHz		4.3/Fs 18/Fs 9/Fs	600	µs
Group delay mismatch		Between left and right channels			2	µs
Power Supply Rejection Ratio	PSRR[4] with respect to VDDA	20Hz – 2kHz 20kHz	70 50			dB

[2] SNR (signal-to-noise ratio) is a ratio of the full-scale output signal level to the noise level with no signal applied.
[3] THD+N (total harmonic distortion plus noise) is a ratio of the level of the harmonics and noise to the output signal.
[4] PSRR (power supply rejection ratio) is a measure of the attenuation of a signal on the supply to the signal at the output.

Microphone Bias

MICBIAS1 and MICBIAS2						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Bias Voltage	$V_{MICBIAS}$	No load, VDD_MIC > $V_{MICBIAS}$ + 200mV	1.52	1.57	1.62	V
			2.18	2.25	2.32	
			2.41	2.48	2.56	
			2.91	3.00	3.10	
Maximum Current	I_{BIAS}	Voltage drop < 50mV		2		mA
Power Supply Rejection Ratio	PSRR with respect to VDD_MIC	20Hz – 200Hz >2kHz	70 50			dB
Output Noise Voltage	V_{NOISE}	VMICBIAS ≤ 2.2V		5		μV_{RMS}
Capacitive Load		I_{BIAS} < 100uA 100uA < I_{BIAS} < 2mA		100 200		pF

Input Mixing Units

(MIC1_P/MIC1_N/MIC2_P/MIC2_N/AUX_L/AUX_R) to ADC_L/ADC_R						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Full-scale input signal	VMAX	Single-ended Differential MICn_PGA = AUXx_PGA = INx_PGA = 0dB		0.8 × VDD_A 1.6 × VDD_A		V_{PP}
Input resistance	RIN	MIC, single-ended AUX	12 6	15	18 40	kΩ
Input capacitance	CIN			1		pF
Amplitude ripple		20Hz to 20kHz	-0.5		+0.5	dB
Programmable gain		MIC1_PGA and MIC2_PGA AUXL_PGA and AUXR_PGA INL_PGA and INR_PGA	-6 -54 -4.5		36 15 18	dB
Programmable gain step size		MIC1_PGA and MIC2_PGA AUXL_PGA and AUXR_PGA INL_PGA and INR_PGA		6 1.5 1.5		dB
Absolute gain accuracy		0dB @ 1kHz	-1.0		+1.0	dB
Left/Right gain mismatch		20Hz to 20kHz	-0.1		+0.1	dB

Gain step error		20Hz to 20kHz	-0.1		+0.1	dB
Input noise level		Inputs connected to GND, A-weighted, input-referred, measured @ ADC output MIC1/2_PGA = 24dB AUXL/R_PGA = 15dB		 5 6.5		μV_{RMS}
Input Amplifier SNR		Differential, A-weighted, input-referenced.		110		dB
Power supply rejection ratio	PSRR with respect to VDDA	Single-ended input 20Hz to 2kHz 20kHz	 70 50			dB
		Differential input 20Hz to 2kHz 20kHz	 90 70			dB

Audio Outputs

Digital to Analogue Converter (DAC)

PARAMETER	SYMBOL	TEST CONDITIONS	Min	Typ	Max	UNIT
Full-scale output signal	V_{MAX}	Digital input level = 0dBFS		1.6×VDDA		V_{PP}
Signal to Noise Ratio	SNR	A-weighted		100		dB
Total Harmonic Distortion Plus Noise	THD+N	-1dBFS 44.1kHz slave mode		-90		dB
		-1dBFS 32kHz PLL mode		-80		dB
Channel separation				90		dB
Pass band	B_{PASS}				0.45×Fs	kHz
Stop band	B_{STOP}	Fs ≤ 48kHz Fs = 88.2/96kHz	0.56×Fs		7×Fs 3.5×Fs	kHz
Pass band Ripple		Voice mode Music mode			±0.15 ±0.1	dB
Stop band Attenuation		Voice mode Music mode	70 55			dB
Group delay		Voice mode Music mode Fs = 88.2/96kHz		4.8/Fs 18.5/Fs 9/Fs	650	µs
Group delay variation		20Hz to 20kHz			1	µs
Group delay mismatch		Between left and right channels			2	µs
Power Supply Rejection Ratio	PSRR with respect to VDDA	20Hz to 2kHz 20kHz	70 50			dB

Class AB Lineout Amplifier / Speaker Driver

From DAC_L/DAC_R to (SP_P, SP_N)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Full-scale output signal	V_{MAX}	No load		1.8×VDD_SP		V_{PP}
Maximum output power	P_{MAX}	VDD_SP = 1.2V THD < 10% R_{LOAD} = 8Ω, 1kHz		65		mW_{RMS}
		VDD_SP = 1.5V THD < 10% R_{LOAD} = 8Ω, 1kHz		115		mW_{RMS}
		VDD_SP = 3.7V THD < 10% R_{LOAD} = 8Ω, 1kHz		745		mW_{RMS}
		VDD_SP = 5.0V THD < 10% R_{LOAD} = 8Ω, 1kHz		1200		mW_{RMS}
Load impedance	R_{LOAD}		6.4	8	 1 200	Ω µH pF
Frequency response		±0.5dB	20		20k	Hz
Amplitude ripple		20Hz to 20kHz	-0.5		0.5	dB
Programmable gain			-48		+15	dB
Mute attenuation				100		dB
Programmable gain step size				1		dB
Absolute gain accuracy		0dB @ 1kHz	-0.8		+0.8	dB
Gain step error		20Hz to 20kHz	-0.1		+0.1	dB
Signal to noise ratio	SNR	A-weighted gain = 0dB VDD_SP = 1.6V		96.5		dB
Output Noise Level	V_{NOISE}	Non A-weighted Gain ≤ -15dB 20Hz to 20kHz		6		µV
Total Harmonic Distortion Plus Noise	THD+N	VDD_SP = 1.6V -1dBFS 44.1kHz slave mode R_{LOAD} > 2kΩ		-86		dB
		VDD_SP = 1.6V -1dBFS 32kHz PLL mode R_{LOAD} > 2kΩ		-80		dB
Power Supply Rejection Ratio	PSRR with respect to VDD_SP	20Hz to 2kHz 20kHz	90 70			dB

True Ground Charge Pump

HPCSP and HPCSN						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Positive rail output	VDDCSP	CP_MOD = 11 CP_MOD = 10		VDD_A VDD_A / 2		V
Negative rail output	VDDCSN	CP_MOD = 11 CP_MOD = 10		-VDD_A -(VDD_A / 2)		V
Flyback capacitor		One capacitor		1.0		µF
Reservoir capacitors		Two capacitors		1.0		µF

True Ground Headphone Amplifier

From DAC_L/DAC_R to (HP_L/HP_R)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**Min**	**Typ**	**Max**	**UNIT**
Full-scale Output Signal	V_{MAX}	No load		1.6×VDD_A		V_{PP}
DC output offset		HP Gain < -30dB			100	µV
Maximum power per channel	P_{MAX}	VDD_A = 1.6V THD < 0.1% R_{LOAD}=16Ω, 1kHz		L = 23 R = 23		mW_{RMS}
		VDD_A = 1.8V THD < 0.1% R_{LOAD}=16Ω, 1kHz		L = 29 R = 29		mW_{RMS}
		VDD_A = 2.5V THD < 0.1% R_{LOAD}=16Ω, 1kHz		L = 67 R = 67		mW_{RMS}
Load Impedance	R_{LOAD} L_{LOAD} C_{LOAD}		13	16	 400 500	Ω µH pF
Frequency Response		±0.5dB	20		20k	Hz
Amplitude Ripple		20Hz to 20kHz	-0.5		+0.5	dB
Programmable Gain			-56		+6	dB
Mute Attenuation				70		dB
Programmable Gain Step Size				1.0		dB
Absolute Gain Accuracy		0dB @ 1kHz	-0.8		+0.8	dB
Input Gain L/R-Mismatch		20Hz to 20kHz	-0.1		+0.1	dB
Input Gain Step Error		20Hz to 20kHz	-0.1		+0.1	dB
Signal to Noise Ratio	SNR	A-weighted gain = 0dB VDD_A = 2.5V VDD_A = 1.8V		 100 98		dB

Output Noise Level	V_{NOISE}	20 to 20kHz, non A-weighted gain < -20dB			*2.5*	*uVrms*
Total Harmonic Distortion Plus Noise	THD+N	VDD_A = 1.6V -5dBFS R_{LOAD}=16Ω		-87		dB
Power Supply Rejection Ratio	PSRR with respect to VDD_A	20Hz to 2kHz 20kHz	70 50			dB

Clock Generation

MCLK Input

PARAMETER	SYMBOL	TEST CONDITIONS	Min	Typ	Max	UNIT
Input Amplitude		MCLK squarer enabled MCLK squarer disabled	0.3 0.9×VDD_IO		VDD_IO VDD_IO	V
Input Impedance		DC impedance > 10 MΩ	300 0.5	1	2	Ω pF
MCLK rise time					8ns	

Phase Locked Loop (PLL)

PLL Mode

PARAMETER	SYMBOL	TEST CONDITIONS	Min	Typ	Max	UNIT
MCLK Input Jitter	J_C J_A	Cycle jitter (rms) Absolute jitter (rms)			50 100	ps ps
Input frequency	F_{IN}	Normal mode 32kHz mode	5	32.768	50	MHz kHz
SRM Tracking Range		DAI slave mode WCLK frequency variation	-4		4	%
SRM Tracking Rate		DAI slave mode WCLK drift rate			50	ppm/s

Bypass Mode

PARAMETER	SYMBOL	TEST CONDITIONS	Min	Typ	Max	UNIT
Input Jitter	J_C J_A	Cycle jitter (rms) Absolute jitter (rms)			TBD TBD	ps ps
Input frequency	F_{IN}	Sample frequency: 11.025, 22.05, 44.1, 88.2kHz 8, 12, 16, 24, 32, 48, 96kHz		11.2896 12.288		MHz

SIGNALS AND PACKAGING

Pad Description

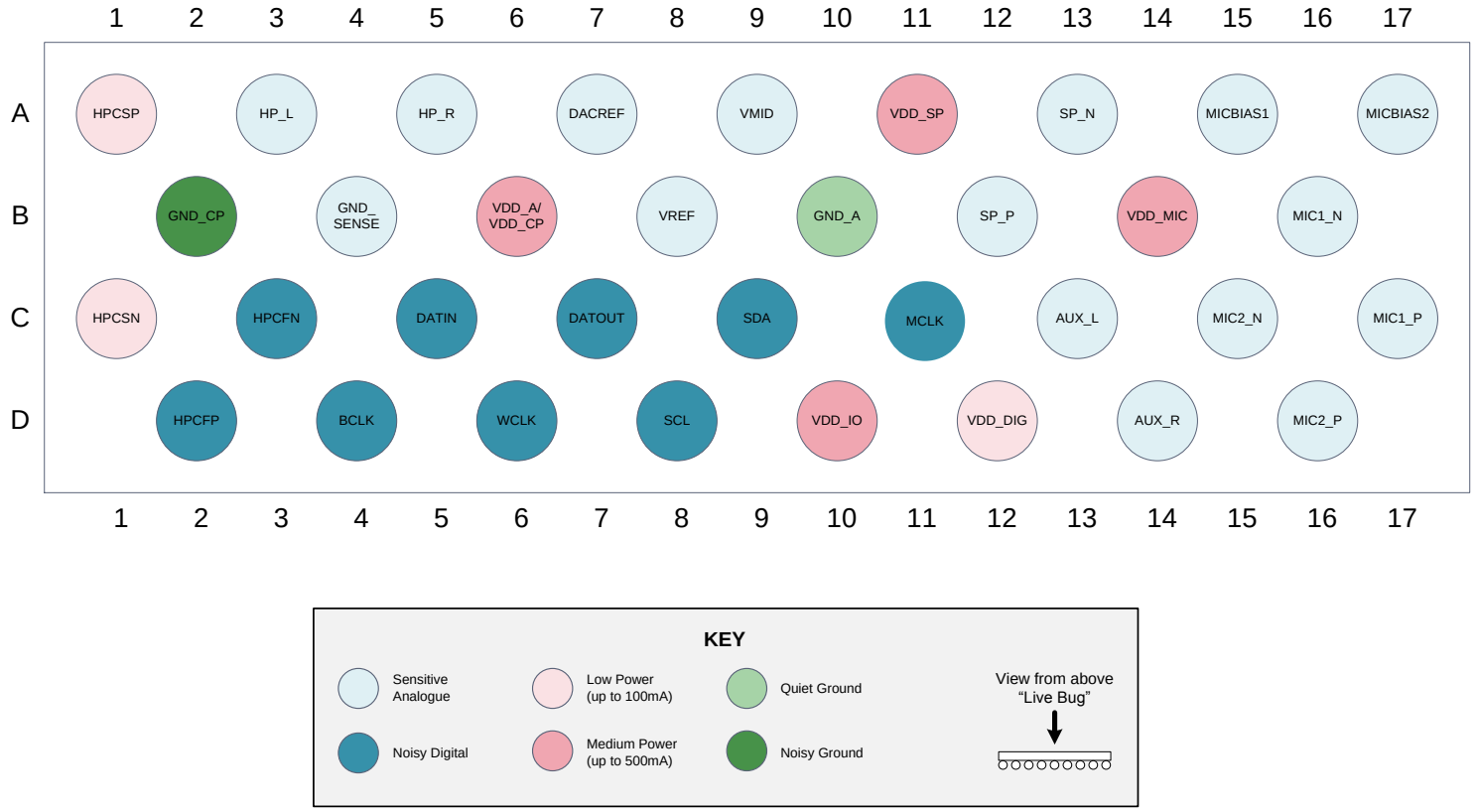


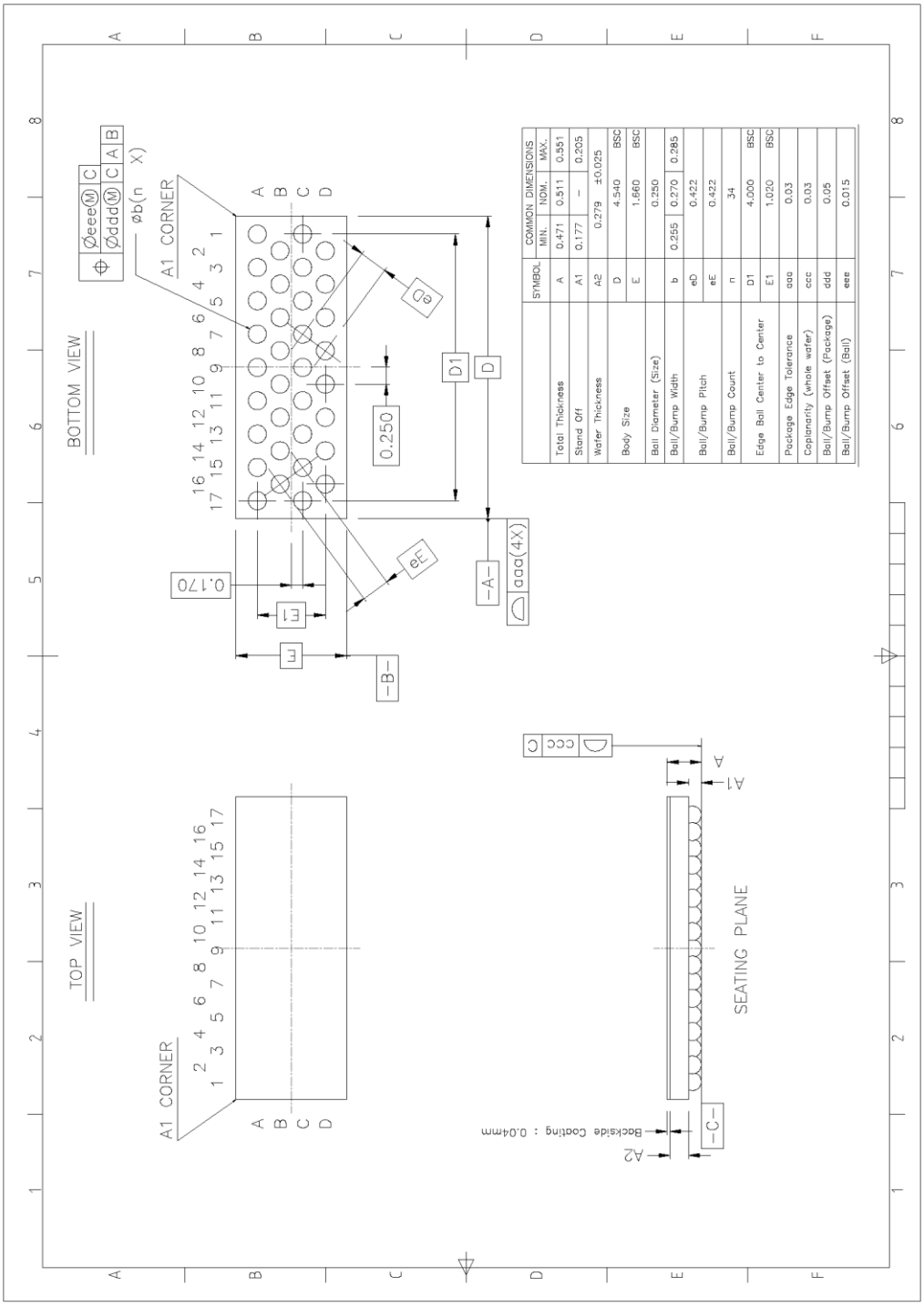
Figure 2: DA7213 ball layout

Pin Descriptions

PIN NAME	BUMP / PIN	FUNCTION	ALTERNATE FUNCTION	CLASS
Audio Inputs				
MIC1_P	C17	Differential mic. input 1 (pos) / Single-ended mic. input 1 (left)	Digital mic. clock (DMICCLK)	AI/DO
MIC1_N	B16	Differential mic. input 1 (neg) / Single-ended mic. input 2 (left)	Digital Mic. data (DMICIN)	AI/DI
MIC2_P	D16	Differential mic. input 2 (pos) / Single-ended mic. input 1 (right)		AI
MIC2_N	C15	Differential mic. input 2 (neg) / Single-ended mic. input 2 (right)		AI
AUX_L	C13	Single-ended auxiliary input left		AI
AUX_R	D14	Single-ended auxiliary input right		AI
MICBIAS1	A15	Microphone bias output 1		AO
MICBIAS2	A17	Microphone bias output 2		AO
Audio Outputs				
HP_L	A3	True-ground headphone output left		AO
HP_R	A5	True-ground headphone output right		AO
SP_P	B12	Differential speaker output (pos)		AO
SP_N	A13	Differential speaker output (neg)		AO
Audio Chargepump				
HPCSP	A1	Chargepump reservoir capacitor (pos)		AIO
HPCSN	C1	Chargepump reservoir capacitor (neg)		AIO
HPCFP	D2	Chargepump flyback capacitor (pos)		AIO
HPCFN	C3	Chargepump flyback capacitor (neg)		AIO
Digital Interfaces				
SDA	C9	I2C bidirectional data		DIO
SCL	D8	I2C clock input		DI
DATIN	C5	DAI data input		DIO
DATOUT	C7	DAI data output		DIO
BCLK	D4	DAI bit clock		DIO
WCLK	D6	DAI word clock (L/R select)		DIO
MCLK	C11	Master clock		DI
References				
DACREF	A7	Audio DAC reference capacitor		AIO
VMID	A9	Audio mid-rail reference capacitor		AIO
GND_SENSE	B4	Ground reference for headphone output		AI
VREF	B8	Bandgap reference capacitor		AIO
Supplies				
VDD_A	B6	Supply for analogue circuits / headphone charge pump		PS
VDD_IO	D10	Supply for digital interfaces		PS
VDD_SP	A11	Supply for speaker driver		PS
VDD_MIC	B14	Supply for microphone bias circuits		PS
VDIG	D12			PS
Grounds				
GND_A	B10	Analogue ground		PG
GND_CP	B2	Chargepump/digital ground		PG

PACKAGE

Package Physical Dimensions



ORDERING INFORMATION

Part Number	Package	Shipment Form	Pack quantity
DA7212-00UM2	34-bump CSP Pb-free/green	T & R	4500

Data Sheet Status Definitions

The Data Sheet version consists of two characters, a numeral followed by a lower-case alphabetic character. The numeral indicates Product Status (see table below), and the alphabetic character indicates the document revision level.
Notes:

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