DA9021/2

System Core PMIC with high efficiency USB power manager

The DA9021/2 family is a highly integrated PMIC subsystem with supply domains to support a wide range of application processors, associated peripherals and user interface functions. Combined with a single input USB compatible charger and multiple sleep modes the device offers an energy-optimised solution suitable for portable handheld, wireless and infotainment applications.

DA9021/2 comes in a small 4x4mm 64 bump WL-CSP package making it ideal for space constrained applications.

Interfacing directly to a Li-Ion/Polymer battery pack the high efficiency switching charger supports precise current/voltage charging as well as pre charge and USB modes without processor interaction. During charging the die temperature is thermally regulated enabling higher capacity batteries to be rapidly charged at currents up to 1.26A with minimum thermal impact to space-constrained PCB's.

DA9022 offers a higher voltage capability on one DC-DC buck converter which is ideal for peripherals and memory running up to 3.6V. USB suspend mode operation is supported and for robustness the USB power inputs are protected against over-voltage conditions.

The internally-generated system power rail supports power scenarios such as instant-on with a full discharged battery. The power efficiency and flexibility of the switching DC-DC bucks is maintained to generate the various supply domains.

Controlled by a programmable digital power manager the 8 user- programmable switching/linear regulators may be configured for a variety of start up sequences, levels and timings.

For optimal processor energy-per-task performance dynamic voltage scaling is permissible on up to four supply domains. Dialog's patented Smart Mirror ™ dynamic biasing is implemented on all linear regulators.

Available in a 64 WL-CSP 4x4mm, 0.5mm package

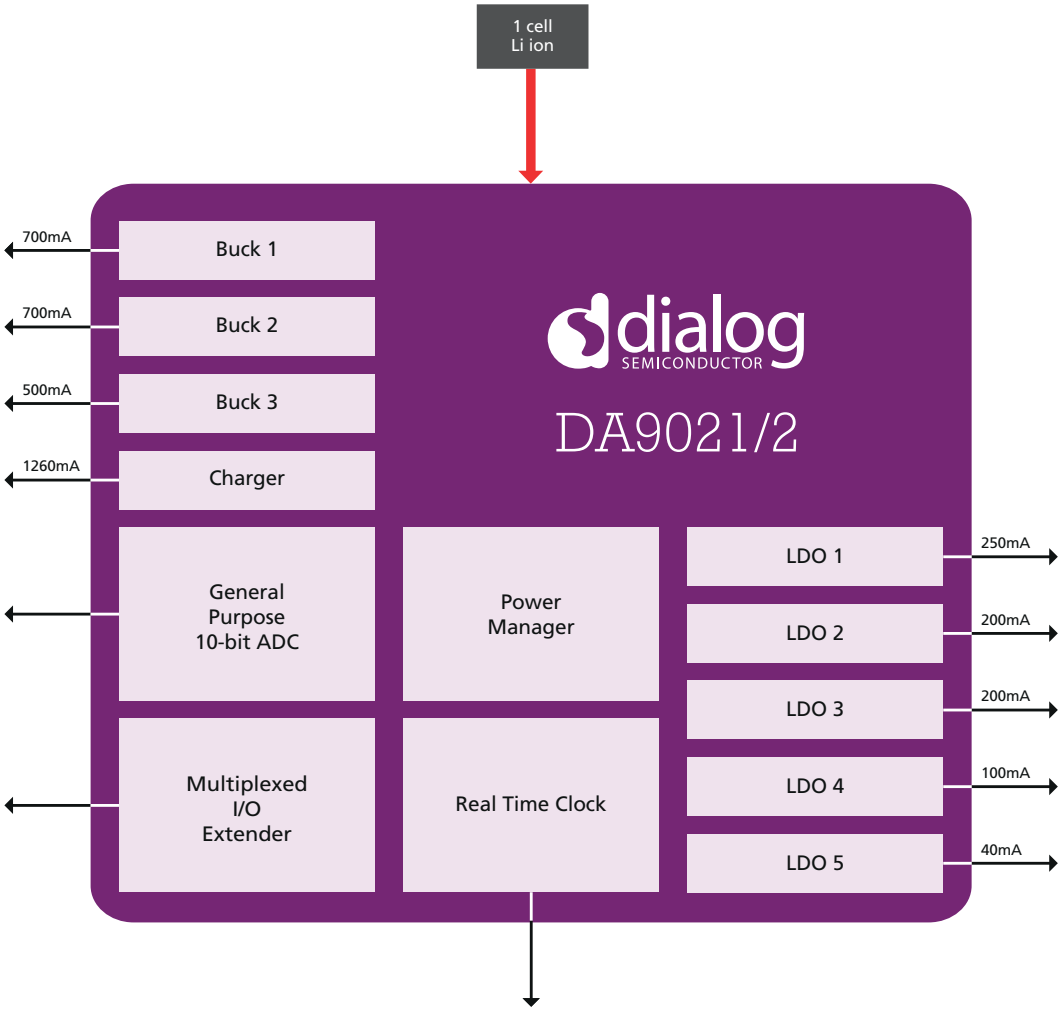
Features

- Single Input USB Charger
- 3 DVS Buck Converters 0.5V-3.6V up to 1Amp
- 5 Programmable LDO's High PSRR.
- 32kHz RTC Oscillator
- 9 bit GPIO bus for enhanced wakeup and peripheral control
- HS2-wire & 4-wire control interfaces

Target Applications

- Personal Media Players
- Smart phone Headsets
- Personal Navigation devices
- Consumer Infotainment devices

Block Diagram



Generated Supply Domains

Regulator	Supplied Voltage	Supplied max. current	External Component	Notes
BUCK A	0.5 – 2.075V ±3% accuracy default 1.8V	800mA 1000mA peak (5us)	2.2 - 4.7uH	DVC, 2MHzr, 25mV steps, DVC ramp with controlled slew rate; pull-down resistor switch off
BUCK B*	0.5 – 2.075V Mbr ±3% accuracy default 1.2V	800mA 1000mA peak (5us)	2.2 - 4.7uH	DA9021 only, DVC, 2MHz, 25mV steps, DVC ramp with controlled slew rate, pull-down resistor switch off
	1.8 – 3.6V ±3% accuracy default 3.3V	800mA 1000mA peak (5us)	2.2 - 4.7uH	DA9022 Only, 2MHz, 50_100mV steps
BUCK C	0.925 – 2.5V ±3% accuracy default 2.0V	650mA 750mA peak (5us)	2.2 - 4.7uH	DVC, 2MHz, 25mV steps, DVC ramp with controlled slew rate, pull-down resistor switch off
LDO A	0.6 – 1.8V ±3% accuracydefault 1.2V	40mA	1.0uF	High PSSR, low noise LDO, 50mV steps, pull-down resistor switch off
LDO B	1.725 – 3.3V ±3% accuracy default 2.85V	200mA	2.2uF	DVC, digital LDO, 25mV steps, DVC with controlled slew rate
LDOC	1.2 – 3.6V ±3% accuracy default 3.1V	200mA	2.2uF	High PSRR, low noise, 50mV steps
LDOD	1.25 – 3.6V ±1% accuracy default 2.5V	100mA	1.0uF	High PSRR, low noise, 50mV steps, OTP trimmed, optional HW control, common supply with LDOE
LDOE	1.2 – 3.6V ±3% accuracy default 1.8V	250mA	2.2uF	High PSRR, low noise, 50mV steps, common supply with LDOD
LDOCORE	2.5V ±2% accuracy	4mA	100uF	Not for external use

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