DA9066

System Power Management IC (PMIC) and Audio CODEC for Dual- and Quad-Core Application Processors

DA9066 combines an ultra-low-power audio CODEC with core power management functions targeting standalone application processors and mobile devices.

The PMIC features single-phase, dual-phase, and RF buck converters. High efficiency is achieved over a wide load range. All power switches are integrated and a high switching frequency allows low-profile inductors to be used.

DA9066 also includes additional modules such as real time clock (RTC), general purpose 12-bit ADC (GPADC), and general purpose I/O pins (GPIO). These support different functions such as battery voltage supervision and device over-temperature protection. All DA9066 features can be accessed by software via the host processor, allowing high flexibility of applications.

Controlled by a programmable digital power manager, the user-programmable switched/linear regulators may be configured to meet the start-up sequence, voltage, and timing requirements for most applications. Dynamic Voltage Scaling (DVS) is available to achieve optimal processor energy-per-task performance. Dialog's patented **SmartMirror™** dynamic biasing is implemented on all linear regulators.

Power mode transitions can be triggered with software control, by dedicated hardware inputs, or with button control. Several types of button press can be used to trigger different power mode transitions.

The DA9066 CODEC supports stereo line input and up to three microphone inputs with dual switchable bias. Three output stages are available, Class G true-ground headphone drivers, a mono Class G earpiece driver, and a 1 W mono Class D amplifier. Comprehensive analog mixing and bypass paths to the output drivers are available.

Digital audio transfer to and from the external processor is via a bidirectional interface which supports sample rates from 8 kHz to 96 kHz and I2S, TDM, LJ, RJ, and DSP modes. The device can operate in slave or master modes using the internal phase-locked loop (PLL), which may be powered down.

A range of built-in filtering, equalization, and audio DSP enhancements are available. These are configured by the processor over the 2-wire serial interface and can be tailored to minimize latency and power consumption.

Available in WLCSP, 5.8 mm x 4.8 mm. 0.4 mm pitch

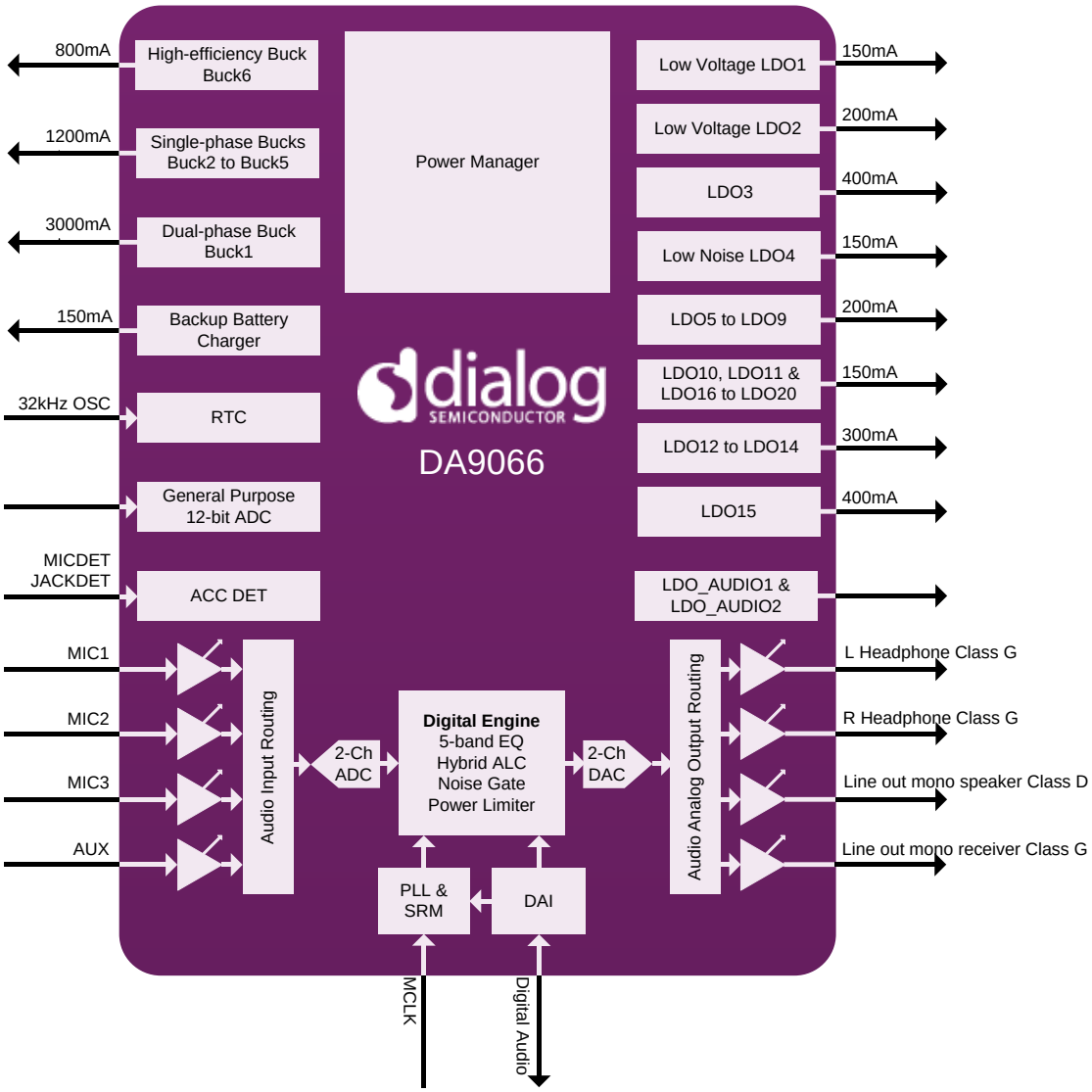
Features

- Operating range 2.5 V to 4.4 V
- 20 programmable LDO regulators
- One dual-phase 3 A buck converter
- Four single-phase buck converters
- One high-efficiency RF buck converter
- Low-power backup battery charger
- 32 kHz real-time clock (RTC) with alarm capability
- 12-bit general purpose ADC with auto-mode controller
- Temperature to voltage supervision
- High-speed I^2C interface
- OTP memory
- Full low-power audio codec
- 98 dB stereo output into 16 Ω to 32 Ω headphones
- Minimum external components; capless, true-ground driver eliminates bulky headphone coupling capacitors
- Supports three microphones with separate low-noise microphone bias outputs
- Low-power PLL provides system clocking and audio sample rate flexibility
- Built-in five-band EQ, ALC, and noise gate DSP functions
- WLCSP 5.8 mm x 4.8 mm, 0.4 mm pitch

Applications

- Smartphones and mobile phones
- Ultrabooks, tablet PCs and eBook readers
- Portable navigation devices
- TV and media players

Block Diagram



Generated Supply Domains

Regulator	Supplied Voltage (V)	Supplied Max. Current (A)	External Components	Notes
Buck1 Dual-Phase	0.6 to 1.4	3.0	$L_1 = L_2 = 1.0$ µH $C_{1OUT} = C_{2OUT} = 22$ µF	3 MHz, DVS, 6.25 mV steps
Buck2	0.725 to 2.075	1.2	L = 2.2 µH $C_{OUT} = 10$ µF	3 MHz, DVS, 25 mV steps
Buck3	0.725 to 2.075	1.0	L = 2.2 µH $C_{OUT} = 10$ µF	3 MHz, DVS, 25 mV steps
Buck4	0.725 to 2.075	0.6	L = 2.2 µH $C_{OUT} = 10$ µF	3 MHz, DVS, 25 mV steps
Buck5	0.725 to 2.075	0.6	L = 2.2 µH $C_{OUT} = 10$ µF	3 MHz, DVS, 25 mV steps
Buck6 RF Buck	0.4 to 3.5	0.8	L = 0.5 µH or 1 µH $C_{OUT} = 4.7$ µF	Voltage control input Integrated bypass switch Fast voltage transient response
LDO1	1.0 to 3.1	0.15	$C_{OUT} = 1.0$ µF	Low voltage, step size 50 mV
LDO2	1.0 to 3.1	0.2	$C_{OUT} = 1.0$ µF	Low voltage, step size 50 mV
LDO3	1.2 to 3.3	0.4	$C_{OUT} = 2.2$ µF	Step size 50 mV
LDO4	1.2 to 3.3	0.15	$C_{OUT} = 2.2$ µF	Low noise, step size 50 mV
LDO5	1.2 to 3.3	0.2	$C_{OUT} = 1.0$ µF	Step size 50 mV
LDO6	1.2 to 3.3	0.2	$C_{OUT} = 1.0$ µF	Step size 50 mV
LDO7	1.2 to 3.3	0.2	$C_{OUT} = 1.0$ µF	Step size 50 mV
LDO8	1.2 to 3.3	0.2	$C_{OUT} = 1.0$ µF	Step size 50 mV
LDO9	1.2 to 3.3	0.2	$C_{OUT} = 1.0$ µF	Step size 50 mV
LDO10	1.2 to 3.3	0.15	$C_{OUT} = 1.0$ µF	Step size 50 mV
LDO11	1.2 to 3.3	0.15	COUT = 1.0 µF	Step size 50 mV
LDO12	1.2 to 3.3	0.3	$C_{OUT} = 2.2$ µF	Step size 50 mV

Regulator	Supplied Voltage (V)	Supplied Max. Current (A)	External Components	Notes
LDO13	1.2 to 3.3	0.3	C_{OUT} = 2.2 µF	Step size 50 mV
LDO14	1.2 to 3.3	0.3	C_{OUT} = 2.2 µF	Step size 50 mV
LDO15	1.2 to 3.3	0.4	C_{OUT} = 2.2 µF	Step size 50 mV
LDO16	1.2 to 3.3	0.15	C_{OUT} = 1.0 µF	Step size 50 mV
LDO17	1.2 to 3.3	0.15	C_{OUT} = 1.0 µF	Step size 50 mV
LDO18	1.2 to 3.3	0.15	C_{OUT} = 1.0 µF	Step size 50 mV
LDO19	1.2 to 3.3	0.15	C_{OUT} = 1.0 µF	Step size 50 mV
LDO20	1.2 to 3.3	0.15	C_{OUT} = 1.0 µF	Step size 50 mV
LDO_AUD1	1.2 to 3.3	0.05	C_{OUT} = 1.0 µF	Internal audio LDO
LDO_AUD2	1.2 to 3.3	0.05	C_{OUT} = 1.0 µF	Internal audio LDO
BACKUP	1.8 to 3.3	0.006	470 nF	Step size 100 mV or 200 mV Configurable current limit between 100 µA and 6000 µA Reverse current protection

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