Application Note

PV88090 Voltage Rail Sequencing

AN-PV-009

Abstract

The application note describes control of the power rail sequencing of the PV88090 PMIC.

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1 Introduction

PV88090 integrated three-channel PMIC incorporates advanced power sequencing that can be used to control the power up and power down sequence of its buck converters. It contains on-board OTP that is used to store the sequencing and this sequencing can also be controlled by an I²C command issued via the GUI or from the host processor. In applications requiring multiple PV88090s, GPIO and STBY pins can be used to control cascaded devices.

2 Sequencing

In the PV88090 digital system, there are 15 time slots used for sequencing. The system runs the time slots from 1 to 15 during the power on sequence, and runs back from 15 to 1 during the power down sequence. The available bucks should be assigned to slots between 1 and 15. The power on sequence, once arranged, can use the SYSTEM_END parameter to separate the Standby mode and the Active mode operation. When STBY is pulled high, the system runs the sequence before the SYSTEM_END slot. The system is now in the standby mode. When STBY is pulled low, all the slots run in sequence, the system is then in active mode, see Figure 1.

Note 1 If the standby pin is not used in your application, then SYSTEM_END is not available.

A slot0 assignment means that function will not follow the power on or power off sequence. The buck assigned to slot0 will not be enabled in the power on sequence but can manually be turned on by I²C.

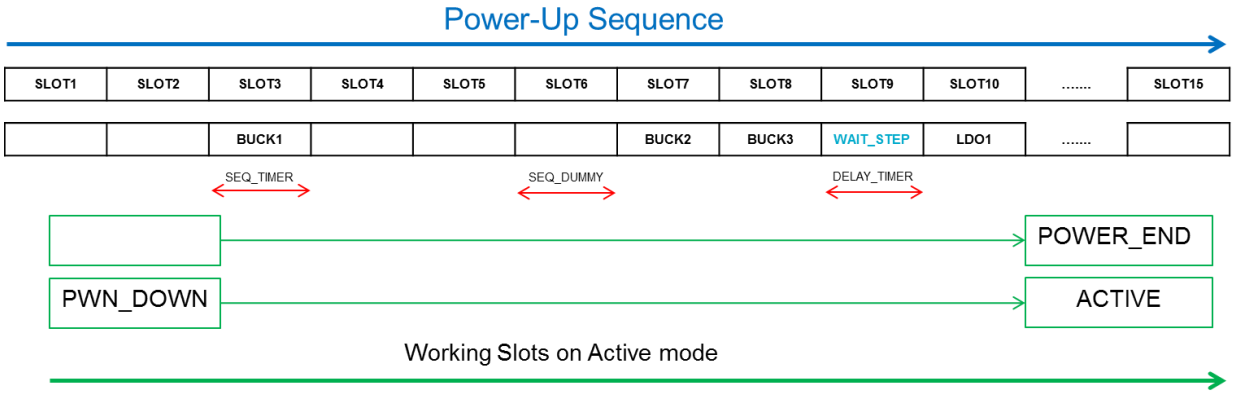

Figure 1: Sequencing Slots Model

There are two types of time slots, a normal slot which can be put in the sequence, like bucks or LDOs, and empty or "dummy slots". The time length can be set using SEQ_DUMMY register bits. For example, slot1, slot2, slot4, and slot6 in Figure 1 are empty and are, therefore, dummy slots. The time length of both normal and dummy slots can be programed in register 0x17.

2.1 General Power Sequencing Setting

For general purpose sequencing, every buck converter should be assigned to a slot. Figure 2 shows an example of power sequencing. The power sequence follows the order assigned in the example, Buck1 [3], Buck2 [7], Buck3 [8], and LDO1 [10]. Every power rail can have its own slot number, two different power rails are allowed to be set to the same slot if they need to be turned on together. Set the SEQ_TIME and SET_DUMMY to adjust the slot time length, the delay time between the two different slots can be controlled.

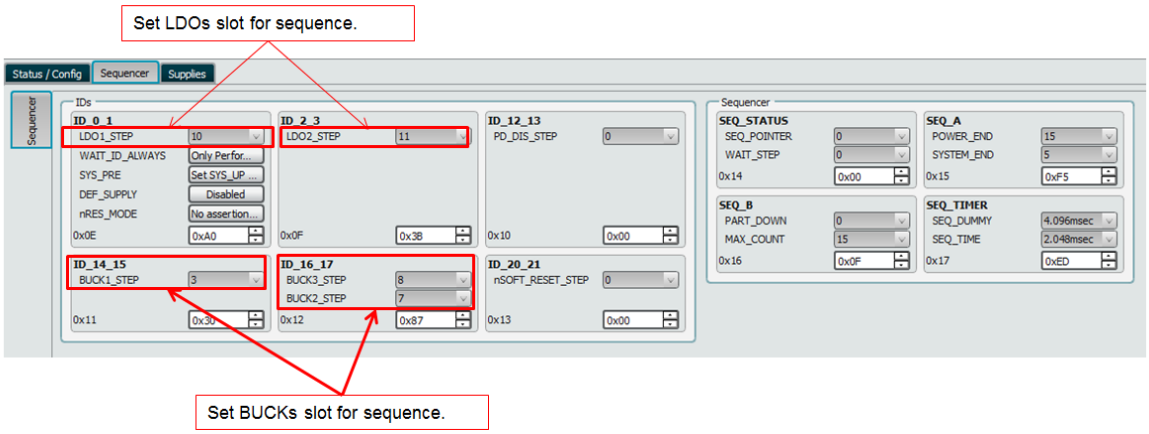

Figure 2: Sequencing Example and GUI Setting

By way of example, assume that a system requires Buck1 to turn on 14 ms earlier than Buck2 and Buck1 → <14 ms delay> →Buck2 →<2 ms delay> → Buck3.

Set SEQ_TIME = 2.048 ms, Buck1 set in slot3, Buck2 set in slot7, and Buck3 is in slot8, the delay time between Buck2 and Buck3 would be a normal sequence time so the result is 2 ms. Set the SET_DUMMY = 4.096 ms, the delay time from Buck1 to Buck2 is a normal sequence time + 3 x dummy sequence time to gain the 14 ms delay time. The resulting sequence is shown in Figure 3.

The user can assign different combinations of slots and slot times to achieve the system requirement.

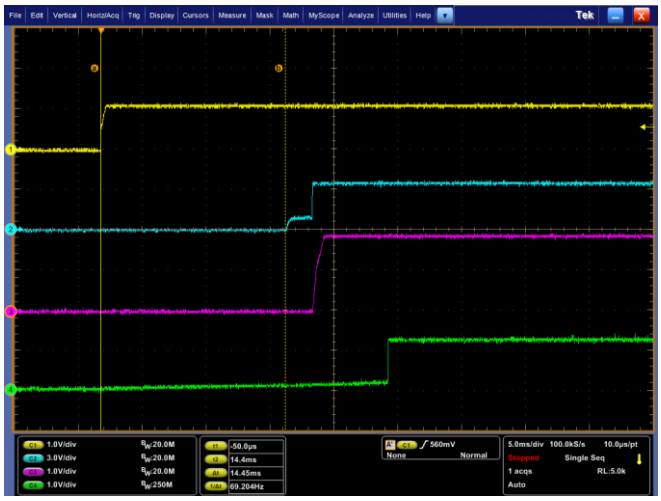

Figure 3: Sequencing Waveform

2.2 Specific Delay Time between Power Sequences

In certain circumstances, a system may need a longer sequence than supported by the standard 15 slots + dummy slots.

For this situation, the PV88090 WAIT_ID function can be used to insert a time slot to add a specific delay time.

ID_0 ((0x14[4:0]) is used to set the WAIT_ID slot, it can be programmed to work for power up and power down sequences, or alternatively it can be programmed to operate on the first power on sequence.

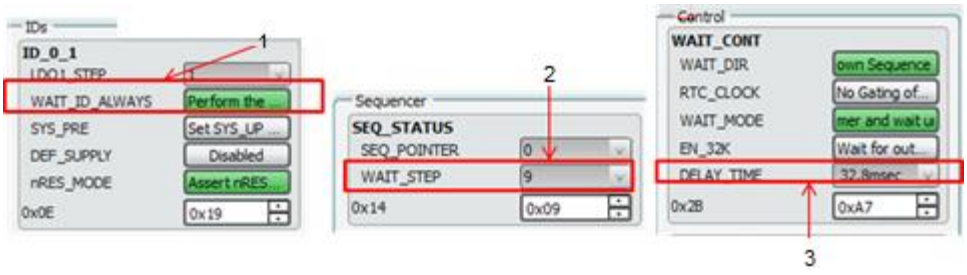

Figure 4: WAIT_ID Behavior and Slot Setting

Note 1 Choose when the WAIT_ID function is to be performed. This can be set to be only for the first power on or always.

Note 2 Set which slot this WAIT_STEP is to be performed, in this example slot9.

Note 3 Set the period for DELAY_TIME, which is 32.8 ms in this example.

WAIT_STEP can insert a specific delay time in the slot, the time length is set by DELAY_TIME 0x39[0] with a range from 0 to 8.4 s. To illustrate the use of the WAIT_ID function consider a system that needs a 34 ms delay between Buck3 and LDO1, keeping the original sequence time between Buck1, Buck2, and Buck3 as shown in Figure 3.

Set DELAY_TIME = 32.8 ms and set WAIT_ID in slot9. The delay time between Buck3 and LDO1 increases to 34.8 ms (typ). Figure 5 shows the result with an additional delay time in slot9 between Buck2 and Buck3.

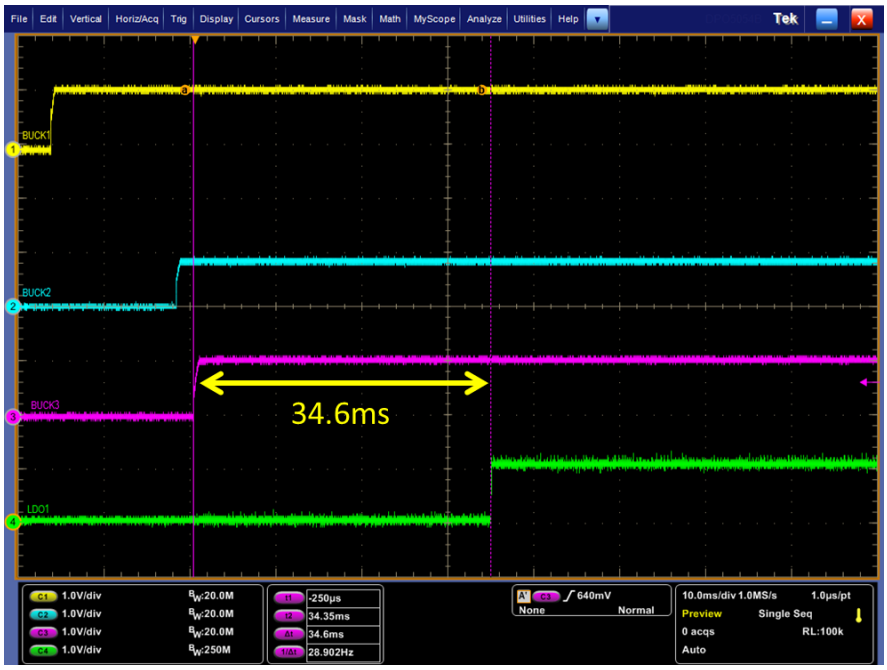

Figure 5: Example Sequencing with an Additional WAIT_STEP Slot

Depending on the system requirement, the WAIT_ID slot can be set up to run during first time power up or every time the sequence is initiated:

- Turning off the WAIT_ID _ALWAYS, will set WAIT_ID to **First use**, the WAIT_ID delay time runs once at power on reset. Afterwards it becomes a normal slot. When this field is off the background color is gray.
- Turning on the WAIT_ID _ALWAYS, will set WAIT_ID to **Always**, the WAIT_ID performs a delay every time the system runs the sequence (when coming out of standby). Afterwards it becomes a normal slot. When this field is on the background color is green.

3 Conclusion

PV88090 provides a flexible sequencing control via OTP and I^2C setup and commands. This eases the burden on the BoM and PC space, provides a reduction in host GPIOs, and results in an improved reliability through the reduced component count.

Revision History

Revision	Date	Description
1.0	29-Dec-2017	Updated Wait_ID_Always description
0.3	20-Dec-2017	Reviewed throughout and updated details on the last page
0.2	12-Dec-2017	Initial version

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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