PCN / EOL Notification

Product Change Notification Number: SC120701 **Notification Date*:** March 6, 2012

Title: 8-Mbit Serial Flash (AT25DF081, 1.65V to 1.95V) Process Geometry Shrink and Discontinuance of 11-Ball dBGA (WLCSP) Package Offering

Product Identification:

All package options of the Industrial Temperature Grade (-40°C to +85°C) AT25DF081

Replacement parts numbers are shown in Table 1.

Reason for Change:

- ☒ Material / Composition
- ☒ Processing / Manufacturing
- ☒ Design / Firmware
- ☐ Logistics
- ☐ Manufacturing Location
- ☐ Quality / Reliability

Change Description:

Atmel has performed a geometric process shrink of the AT25DF081 Serial Flash (8-Mbit density, 1,65V to 1.95V) from **130nm to 110nm**. The catalog part number AT25***DF***081 will be replaced by AT25***DL***081.

The new devices are pin-to-pin and backward compatible with the current 25DF081 devices.

The 11-ball dBGA (WLCSP) is being replaced with an 8-ball dBGA (WLCSP), since the 8-ball utilizes the same active ball matrix layout (the center 8 balls) as the 11-ball package. Please contact Atmel for the Package Outline Drawings for the 11-ball and 8-ball dBGA packages.

Table 1 below cross references the current and new part numbers.

Table 1

Current Part Number	New Part Number
AT25DF081-MHN-T	AT25DL081-MHN-T
AT25DF081-MHN-Y	AT25DL081-MHN-Y
AT25DF081-SSHN-B	AT25DL081-SSHN-B
AT25DF081-SSHN-T	AT25DL081-SSHN-T
AT25DF081-UUN-T	AT25DL081-UUN-T

Attachment A provides a basic key feature comparison between the current and new devices.

Datasheets for both the old and new devices can be found @

http://www.atmel.com/products/memories/sflash/default.aspx?tab=documents&Asset_Type=010 Datasheet

<CLICK OR SCAN HERE>

www.atmel.com

Identification Method to Distinguish Change: New catalog part numbers will be identifiable by the root part number code (AT25***DF***081 changes to AT25***DL***081). Please refer to Table 1 for catalog part number changes.			
Qualification Data:	☒ Available	☐ Will be available (mm/dd/yr):	☐ Not Applicable
Samples:	☒ Available	☐ Will be available (mm/dd/yr):	☐ Not Applicable
Quantifiable Impact on Quality & Reliability: The new devices are form, fit and functionally equivalent to the current devices, which meet all datasheet specifications.			
Forecasted Availability Date: Now **Last Time Buy Date:** August 31, 2012 **Last Ship Date:** February 28, 2013 **All orders placed after the notification date are non-cancellable and non-returnable (NCNR).*			
Atmel Contact: pcnadm@atmel.com			
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CUSTOMER ACKNOWLEDGEMENT OF RECEIPT: Atmel requests you acknowledge receipt of this PCN / EOL. Please complete and email to the Atmel Contact listed above. In your acknowledgement, you can grant approval or request additional information. **Atmel will deem this change accepted unless specific conditions of acceptance are provided in writing within 30 days from the date of this notice.**	
Company:	
Name:	
Title:	
Date:	
Email Address:	
Location:	
Comments:	

Attachment A

Key Feature Set Comparison		
	AT25DF081	**AT25DL081**
VCC Range	1.65V to 1.95V	1.65V to 1.95V
Maximum CLK Frequency	66MHz SPI	85Mhz SPI
		100Mhz RapidS™
Interface Options	SPI	SPI, RapidS™, Dual I/O
OTP Protection Register (e-S/N)	N/A	128Byte = (64Byte factory + 64Byte User)
Flexible Erase Architecture	– Uniform 4KB block erase	– Uniform 4KB block erase
	– Uniform 32KB block erase	– Uniform 32KB block erase
	– Uniform 64KB block erase	– Uniform 64KB block erase
	– Full chip erase	– Full chip erase
Individual Sector Protection	– 16 sectors of 64KB each	– 16 sectors of 64KB each
Sector Lockdown	N/A	– Any combination of 64KB sectors permanently read-only
Fast Program Erase Times	– 1.0ms typical page program (256 bytes)	– 1.0ms typical page program (256 bytes)
	– 50ms typical 4KB block erase time	– 50ms typical 4KB block erase time
	– 350ms typical 32KB block erase time	– 250ms typical 32KB block erase time
	– 600ms typical 64KB block erase time	– 550ms typical 64KB block erase time
Program Erase Suspend Resume	N/A	YES
Low Power Operation	– 7mA active read current (@ 20MHz)	– 10mA active read current (@ 20MHz)
	– 8µA deep power-down current (typical)	– 8µA deep power-down current (typical)
Software RESET	N/A	YES
JEDEC Device / Manufacturer ID	1Fh	1F
JEDEC Device ID (Byte 1)	45h	45h
JEDEC Device ID (Byte 2)	02h	02H
JEDEC Extended Device Information	00h	01h
	N/A	00h
Endurance	100K cycles	100K Cycles
Data Retention	20years	20Years
Operating Temperature Range	-40°C to +85°C	-40°C to +85°C
Package Options	– 8-lead SOIC (0.150" Wide Body)	– 8-lead SOIC (0.150" Wide Body)
	– 8-pad ultra thin DFN (5 x 6 x 0.6mm)	– 8-pad ultra thin DFN (5 x 6 x 0.6mm)
	– 11-ball dBGA (WLCSP)	– 8-ball dBGA (WLCSP)
This is a basic comparison of key features. Please refer the product datasheets for a full specification comparison		