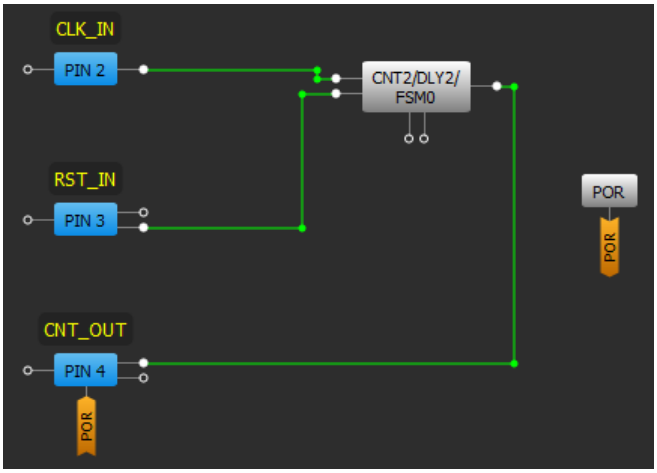
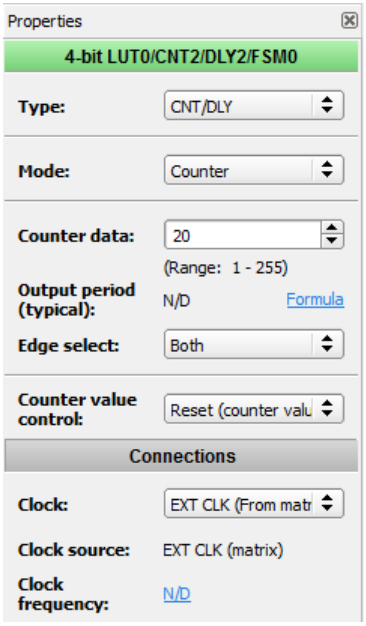
SLG46108

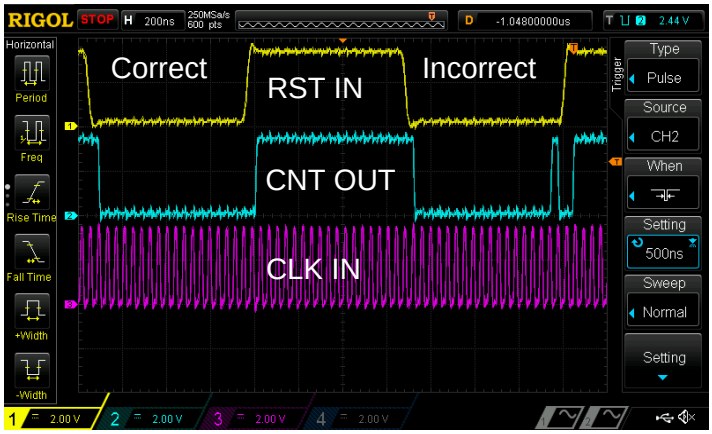
ISSUE 1: Incorrect Counter Operation after the Reset
Functional Block Affected: Counter

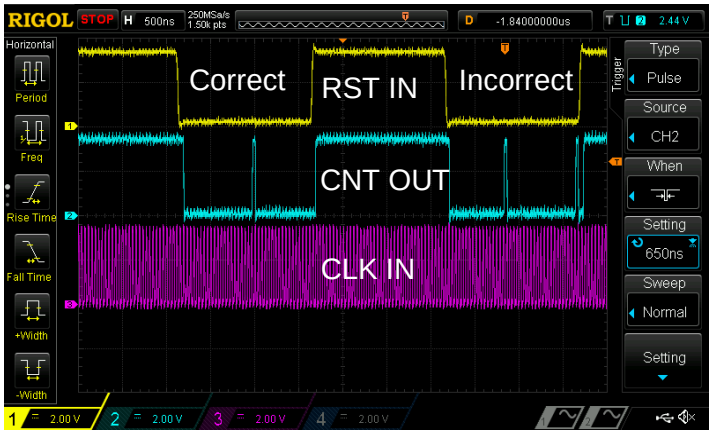
Description:

If the Counter Reset is asserted at the same time as a rising clock edge, it is possible that the Counter Data will be reset incorrectly and the counter output may appear faster than expected. This phenomenon appears more often as the clock frequency increases.



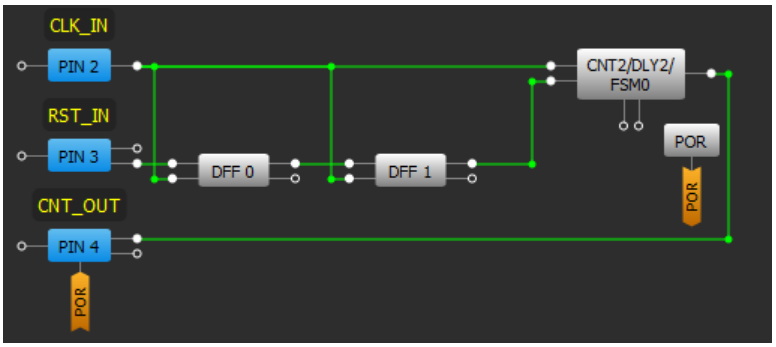






Workaround:

- Synchronize the RESET input of the Counter with its CLK using 2 DFF cells as shown in the image below.



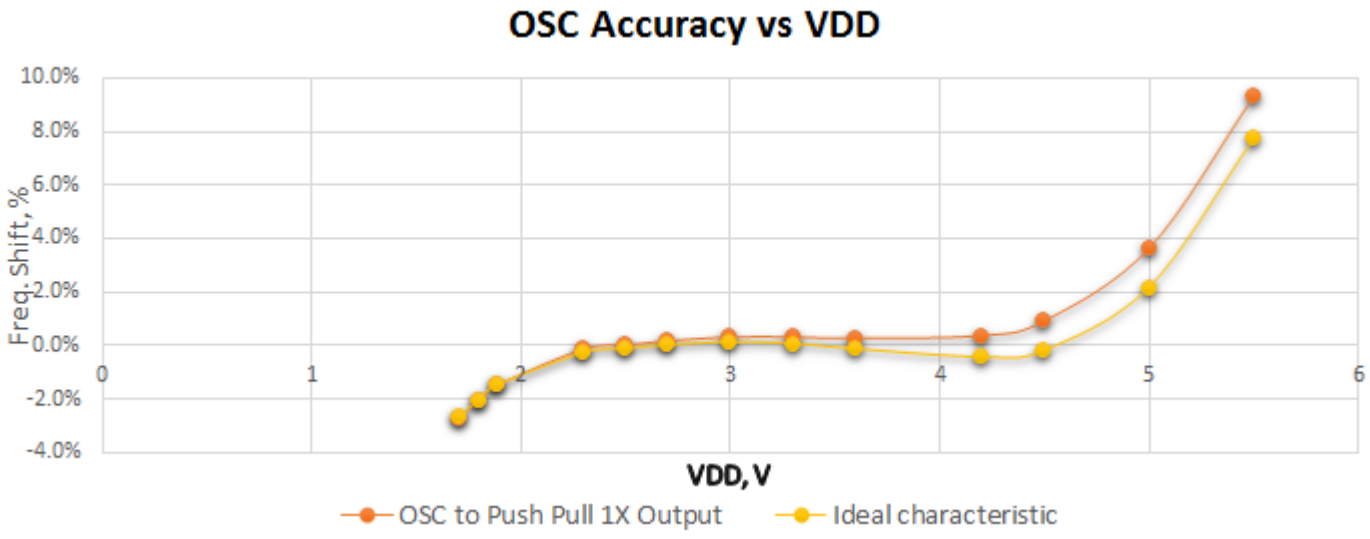
ISSUE 2: VDD Noise Influences OSC Variation
Functional Blocks Affected: OSC, Counter/Delay

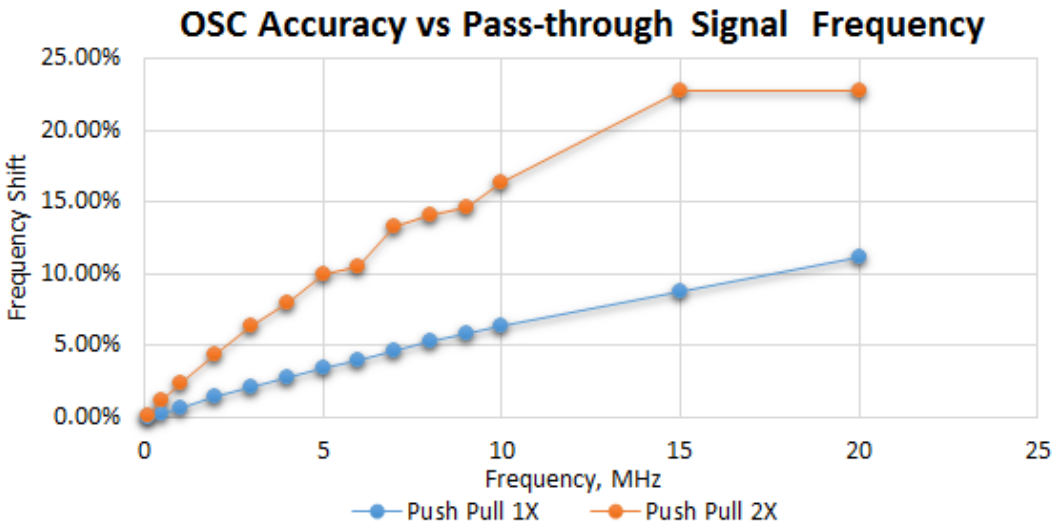
Description:

White applying some high frequency noise to the VDD, OSC inaccuracy may increase. The same behavior is also present in cases where high frequency switches are outputted from the chip using the Push Pull type driver. See, test results below.

Additional frequency Shift by different PINs

VDD =5V Trim VDD = 3.3V	Push Pull 1X	Push Pull 2X	Push Pull 1X	Push Pull 2X
OUT PIN #	f shifted, %	f shifted, %	average	average
4	1.42%	3.63%	1.52%	3.81%
6	1.67%	4.03%		
7	1.62%	3.98%		
8	1.38%	3.59%		
4 … 8	6.73%	11.98%		





Workaround:

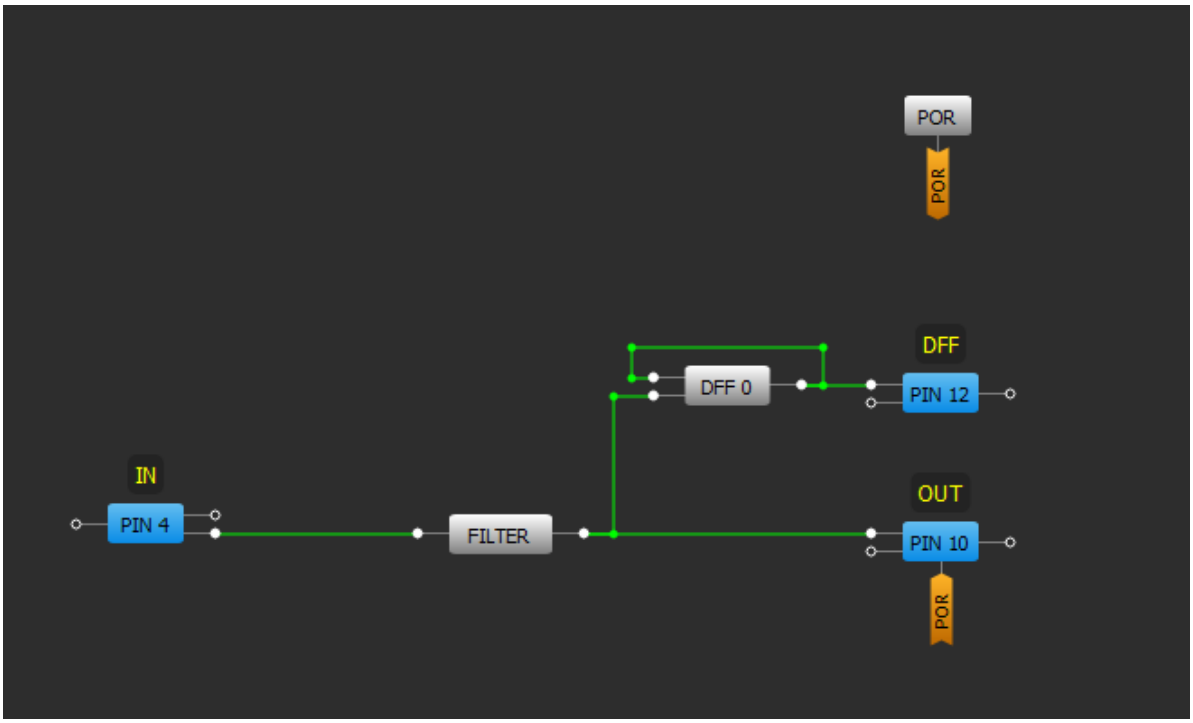
Currently there are no viable workarounds for this issue.
However, the issue can be minimized by doing the following:

- Only use frequencies lower than 2 MHz when switching the output
- Do not use parallel PIN connections to output high speed switching signals.

ISSUE 3: FILTER cell does not filter out glitches
Functional Block Affected: FILTER

Description:

If clock type high frequency input comes in, the FILTER cell may not filter out it. There are several factors like input frequency, duty cycle and LOW duration in such signal that may lead to its passing through FILTER block.



Channel 1 (yellow/top line) – PIN#4 (IN)
Channel 2 (light blue/2nd line) – PIN#10 (OUT)
Channel 3 (magenta /3rd line) – PIN#12 (DFF)

1. Period is 60ns. Pulse width is 10ns DC=16.7% (Correct functionality)

2. Period is 60ns. Pulse width is 20ns DC = 33.3% (Incorrect functionality)

3. Period is 60ns. Pulse width is 30ns DC=50% (Incorrect functionality)

4. Period is 60ns. Pulse width is 40ns DC=66.67% (Correct functionality)

Workaround:

Currently there is no workaround for this issue. Filter block is good at filtering short spontaneous glitches. It is intended to be used in series connection before the delay cell to avoid its latching (see issue #3).

Disclaimer

Information in this document is believed to be accurate and reliable. However, Dialog Semiconductor does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information. Dialog Semiconductor furthermore takes no responsibility whatsoever for the content in this document if provided by any information source outside of Dialog Semiconductor.

Dialog Semiconductor reserves the right to change without notice the information published in this document, including without limitation the specification and design of the related semiconductor products, software and applications.

Applications, software, and semiconductor products described in this document are for illustrative purposes only. Dialog Semiconductor makes no representation or warranty that such applications, software and semiconductor products will be suitable for the specified use without further testing or modification. Unless otherwise agreed in writing, such testing or modification is the sole responsibility of the customer and Dialog Semiconductor excludes all liability in this respect.

Customer notes that nothing in this document may be construed as a license for customer to use the Dialog Semi-conductor products, software and applications referred to in this document. Such license must be separately sought by customer with Dialog Semiconductor.

All use of Dialog Semiconductor products, software and applications referred to in this document are subject to Dialog Semiconductor's Standard Terms and Conditions of Sale, available on the company website (www.dialog-semiconductor.com) unless otherwise stated.

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

Contacting Dialog Semiconductor

United Kingdom (Headquarters)
Dialog Semiconductor (UK) LTD
Phone: +44 1793 757700

Germany
Dialog Semiconductor GmbH
Phone: +49 7021 805-0

The Netherlands
Dialog Semiconductor B.V.
Phone: +31 73 640 8822

Email:
enquiry@diasemi.com

North America
Dialog Semiconductor Inc.
Phone: +1 408 845 8500

Japan
Dialog Semiconductor K. K.
Phone: +81 3 5769 5100

Taiwan
Dialog Semiconductor Taiwan
Phone: +886 281 786 222

Web site:
www.dialog-semiconductor.com

Hong Kong
Dialog Semiconductor Hong Kong
Phone: +852 2607 4271

Korea
Dialog Semiconductor Korea
Phone: +82 2 3469 8200

China (Shenzhen)
Dialog Semiconductor China
Phone: +86 755 2981 3669

China (Shanghai)
Dialog Semiconductor China
Phone: +86 21 5424 9058