SLG46826

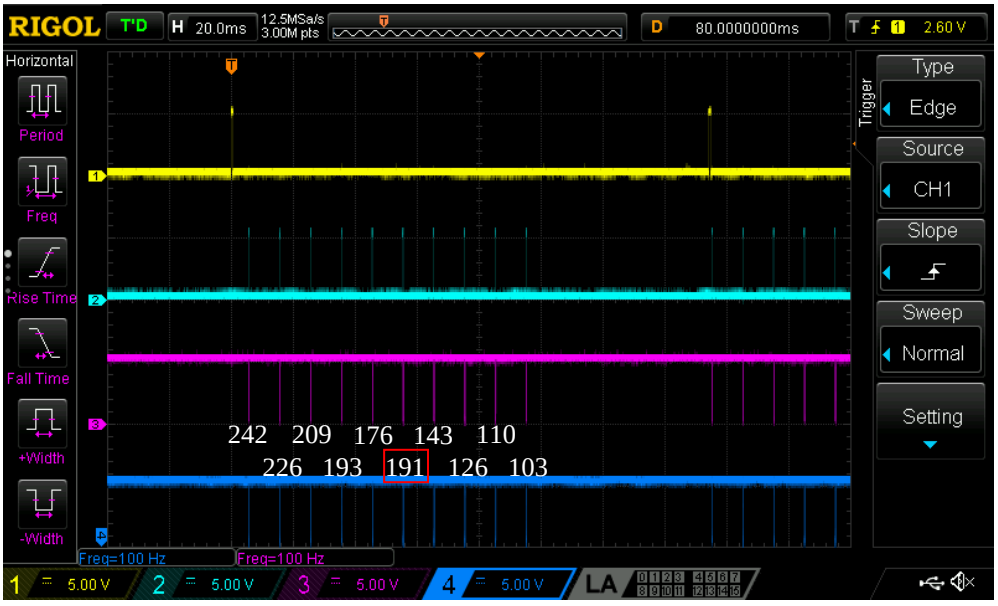
ISSUE 1: Incorrect I²C Reads of the 8-bit Counter Registers
Functional Blocks Affected: CNT2/DLY2 and CNT4/DLY4

Description:

Asynchronous interaction between the CNT/DLY clock input and the I²C latch signal (generated by an I²C read command of the CNT/DLY block's count value) can result in an incorrect I²C data read. The CNT/DLY block will count accurately, but the count value transferred into the block's I²C read register might be loaded incompletely if the I²C latch signal and the clock input occur at about the same time.

The example data capture below shows ten periodic I²C reads of CNT2/DLY2 configured to count down at about 16 clocks per read. The sixth read sample erroneously shows a value greater than that of the fifth. The seventh sample reads as if the previous I²C error never occurred - the difference from the fifth sample (176) to the seventh (143) is 33 clocks or 16 clocks + 17 clocks as expected.

Channel 1 (yellow/1st line) – PIN2 (CNT2/DLY2 Out)
Channel 2 (light blue/2nd line) – PIN1 (I²C Read Triggers)
Channel 3 (magenta /3rd line) – PIN8 (I²C SCL)
Channel 3 (dark blue /4th line) – PIN9 (I²C SDA)



Workaround:

If the possibility of incorrect I²C data reads can't be accommodated for by external software checks, one can guarantee proper operation by stopping the CNT/DLY block's clock during I²C reads through one of the following methods: by disabling the oscillator block, by reconfiguring the CNT/DLY block's clock source, or by gating an external clock using a LUT (Look-up Table) in the signal matrix. After disabling the CNT/DLY block's clock, the count registers can be read without error. Please note that this workaround will add the I²C read and processing time to the counter's overall clock period.

The best workaround depends on the resource constraints of the application. If the oscillator block doesn't clock other logic elements within the design, a matrix output can be used to manually power down the oscillators for the I²C read. When the CNT/DLY block's clock source is routed internally from the oscillator block, I²C commands can temporarily reconfigure the CNT/DLY block's clock source registers to select "Ext. CLK. (From Matrix)." This action will disable the clock by connecting it to ground. If the CNT/DLY block is clocked from the signal matrix, a LUT can be used to gate the clock during an I²C read.

ISSUE 2: Non-I²C Compliant ACK Behavior for the NVM and EEPROM Page Erase Byte

Description:

To erase the NVM and the EEPROM, one must perform an I²C write to the "Page Erase Byte" located at 0xE3. The ACK bit which follows the "Data" portion of Figure 1 won't comply with standard I²C specifications. Please see the ACK bit circled in RED below.

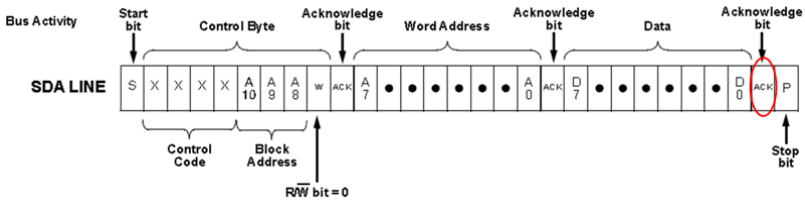
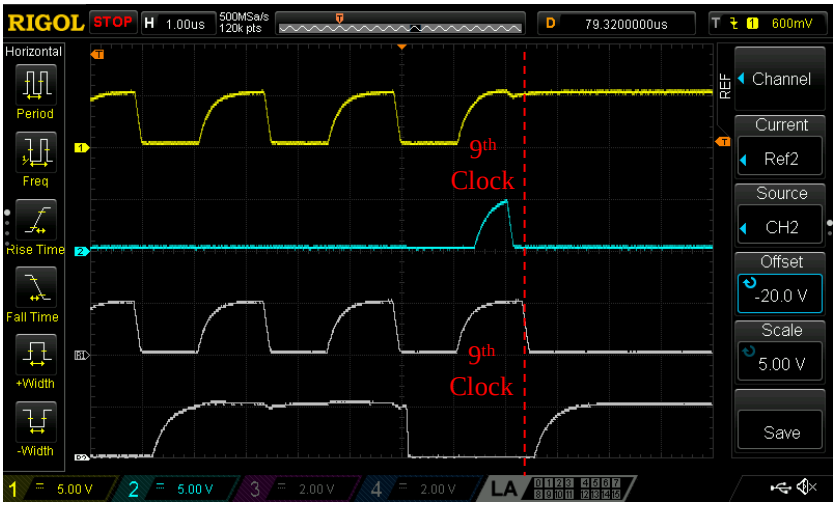


Figure 1: GreenPAK I²C Write Frame for Page Erase

The following waveform compares the regular I²C ACK behavior (Ref 1 - SCL and Ref 2 - SDA) with the non-compliant ACK behavior (Channel 1 - SCL and Channel 2 - SDA) generated by an I²C write to the "Page Erase Byte." During the 9th clock cycle, the SLG46826 does not adhere to the "data hold time" specification by releasing SDA (Channel 2) before the falling edge of the clock pulse on SCL (Channel 1).

Channel 1 (yellow/1st line) – SCL ~ *Non- I²C Compliant ACK Behavior (After Data byte)*
Channel 2 (light blue/2nd line) – SDA ~ *Non- I²C Compliant ACK Behavior (After Data byte)*
Ref 1 (grey/3rd line) – SCL ~ *Regular I²C ACK behavior (Before Data byte) – (5V / div)*
Ref 2 (grey/4th line) – SDA ~ *Regular I²C ACK behavior (Before Data byte) – (5V / div)*



Note: It should be noted that the NVM and EEPROM erases will execute properly inside the GreenPAK device despite a potential I²C NACK. In addition, this behavior only applies to the "Page Erase Byte." All other I²C writes won't exhibit this behavior.

On a system level, other I²C devices might interpret this non-compliant ACK as an additional STOP and START condition. By definition, a START condition occurs when SCL is HIGH and SDA transitions from HIGH to LOW. A STOP condition occurs when SCL is HIGH and SDA goes from LOW to HIGH. After the 9th clock cycle, the MCU should generate the final STOP condition to indicate the end of transmission to all I²C slaves on the bus.

Workaround:

No workaround is required for the GreenPAK device as the NVM and EEPROM erase operations will execute properly. For verification, one can perform an I²C read of the erased pages. Excluding protected pages, all erased NVM and EEPROM registers should be cleared.

Adjust the MCU's I²C firmware to catch and ignore a "NACK" from the GreenPAK device when the "Page Erase Byte" is addressed. In light of the additional STOP and START conditions, the behavior of other I²C slaves on the same bus should be evaluated.

ISSUE 3: Leakage from ACMP IN+ to Analog Input Pins
Functional Blocks Affected: IO11/12/13/14, ACMP0/1H, ACMP2/3L

Description:

When configured in "Analog IO" mode, IO11/12/13/14 can experience abnormal leakage behavior. This behavior occurs when multiple input sources are simultaneously connected to the ACMP IN+ port. Each of the 4 ACMPs has an input MUX which selects the IN+ source for the comparator. The MUX options are shown in the table below.

Table 1: ACMP Input Options

ACMP IN+ MUX Options	
ACMP0H	IO14 Buffered IO14 V_{DD}
ACMP1H	IO13 Buffered IO13 ACMP0H IN+ source
ACMP2L	IO12 ACMP0H IN+ source ACMP1H IN+ source
ACMP3L	IO11 ACMP2L IN+ source Vref0 output

In the GreenPAK Designer, the input source is selected by the IN+ source dropdown within the ACMP's properties window. When an input source is selected and the ACMP is enabled, an analog switch connects the source to the ACMP's IN+ port. If multiple sources are connected to the ACMP's IN+ port, there will be leakage between the sources.

The IOs shown above can be repurposed as Digital IOs if the ACMPs are disabled or if another input source is selected for the ACMP by the IN+ input MUX. Whenever an IO input mode is configured as an "Analog IO" in accordance with the register definition below, the IO will be connected to the ACMP's IN+ port through an internal switch. This can create a leakage scenario if the ACMP is enabled and connected to another input source.

Table 2: IO Input Mode Configurations

Byte	Register Bit	Signal Function	Register Bit Definition
IO11			
70	896 897	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
IO12			
71	904 905	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
IO13			
72	912 913	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
IO14			
73	920 921	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO

There are 3 standard IO settings that use the “Analog IO” configuration: Analog input/output, Digital input/output (with “Input mode” set to Analog input), and Digital output (with “Output mode” set to 1/2/4x 3-State Output). The first setting is reserved for use with the ACMP, but the other two settings use the “Analog IO” configuration as a high-impedance input. It is important to note that these input modes won’t be high impedance if the ACMP is enabled and connected to another input source. When two signals are connected to the ACMP’s IN+ source, the voltage level at the ACMP’s input depends upon the drive strength of the competing sources.

Figure 2 shows the GreenPAK configured with IO14 as a Digital IO with a 1 MΩ pull down resistor. Since the OE pin is connected to 0 V, this pin is acting as an “Analog IO.” As seen in Table 1, IO14 and V_{DD} are both input options for ACMP0H. In this example, IO0 is being used as a digital input to enable and disable the ACMP.

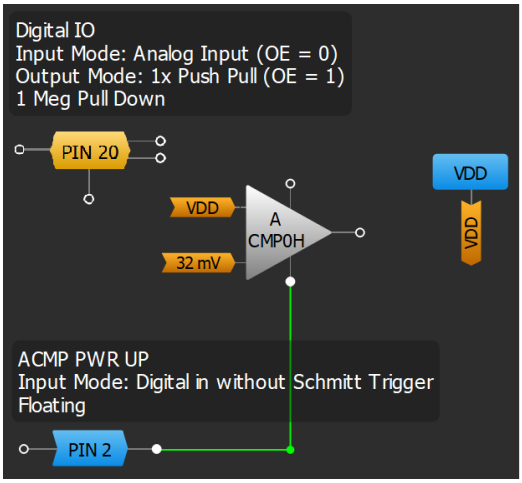


Figure 2: GreenPAK Input Structure Test Schematic

Figure 3 shows that IO14 in analog input mode is pulled HIGH by the V_{DD} signal whenever the ACMP is enabled despite having an internal pull down resistor. This behavior is caused by an internal connection between V_{DD} and IO14. Similar behavior can be reproduced when one ACMP’s IN+ port is connected to another ACMP’s IN+ port.

CH1 (Yellow): ACMP PWR UP (IO0)
CH3 (Light Blue): Digital IO w/ Analog Input Mode Configuration (IO14)

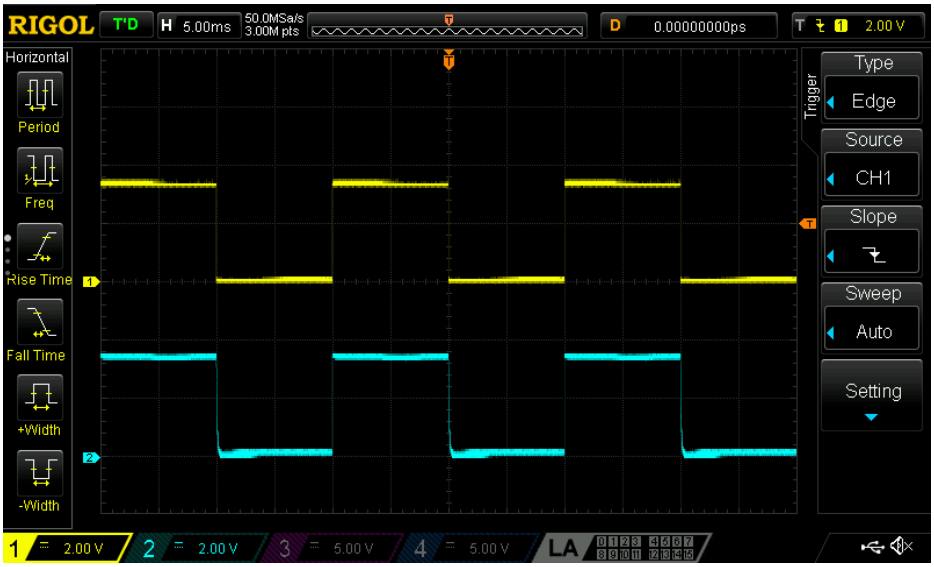


Figure 3: ACMP Input Structure Behavior

Workaround:

If an ACMP is disabled, the IO associated with that ACMP will operate as expected under any configuration. Please reference Table 1 for more information regarding which IOs are associated with which ACMPs.

When the ACMPs are enabled, it is possible to inadvertently connect multiple ACMP sources together through the input structure. This is possible when the ACMP input is connected to a source other than its analog IO and that IO's input mode is set to "Analog IO".

There is no workaround for this behavior. With this in mind, the IOs should not be used as digital IOs (with "Input mode" set to Analog input) or as digital outputs (with "Output mode" set to 1/2/4x 3-State Output) if the respective ACMP is enabled and connected to another input source.

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