

## SLG46880

### ISSUE 1: Incorrect I<sup>2</sup>C Reads of the 8-bit Counter Registers

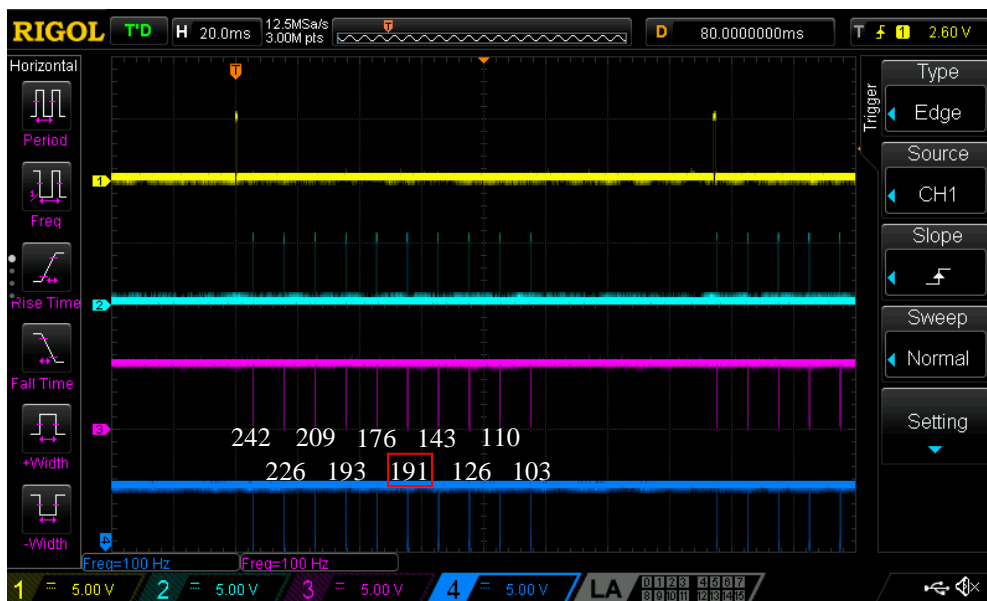
#### Functional Blocks Affected: CNT2/DLY2 and CNT4/DLY4

##### Description:

Asynchronous interaction between the CNT/DLY clock input and the I<sup>2</sup>C latch signal (generated by an I<sup>2</sup>C read command of the CNT/DLY block's count value) can result in an incorrect I<sup>2</sup>C data read. The CNT/DLY block will count accurately, but the count value transferred into the block's I<sup>2</sup>C read register might be loaded incompletely if the I<sup>2</sup>C latch signal and the clock input occur at about the same time.

The example data capture below shows ten periodic I<sup>2</sup>C reads of CNT2/DLY2 configured to count down at about 16 clocks per read. The sixth read sample erroneously shows a value greater than that of the fifth. The seventh sample reads as if the previous I<sup>2</sup>C error never occurred - the difference from the fifth sample (176) to the seventh (143) is 33 clocks or 16 clocks + 17 clocks as expected.

- Channel 1 (yellow/top line) – PIN#2 (CNT2/DLY2 Out)
- Channel 2 (light blue/2nd line) – PIN#1 (I<sup>2</sup>C Read Triggers)
- Channel 3 (magenta /3rd line) – PIN#8 (I<sup>2</sup>C SCL)
- Channel 3 (dark blue /4th line) – PIN#9 (I<sup>2</sup>C SDA)



##### Workaround:

If the possibility of incorrect I<sup>2</sup>C data reads can't be accommodated for by external software checks, one can guarantee proper operation by stopping the CNT/DLY block's clock during I<sup>2</sup>C reads through one of the following methods: by disabling the oscillator block, by reconfiguring the CNT/DLY block's clock source, or by gating an external clock using a LUT (Look-up Table) in the signal matrix. After disabling the CNT/DLY block's clock, the count registers can be read without error. Please note that this workaround will add the I<sup>2</sup>C read and processing time to the counter's overall clock period.

The best workaround depends on the resource constraints of the application. If the oscillator block doesn't clock other logic elements within the design, a matrix output can be used to manually power down the oscillators for the I<sup>2</sup>C read. When the CNT/DLY block's clock source is routed internally from the oscillator block, I<sup>2</sup>C commands can temporarily reconfigure the CNT/DLY block's clock source registers to select "Ext. CLK. (From Matrix)." This action will disable the clock by connecting it to ground. If the CNT/DLY block is clocked from the signal matrix, a LUT can be used to gate the clock during an I<sup>2</sup>C read.

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### ISSUE 2: Noise Coupling from Vref0 to Low-Power Bandgap

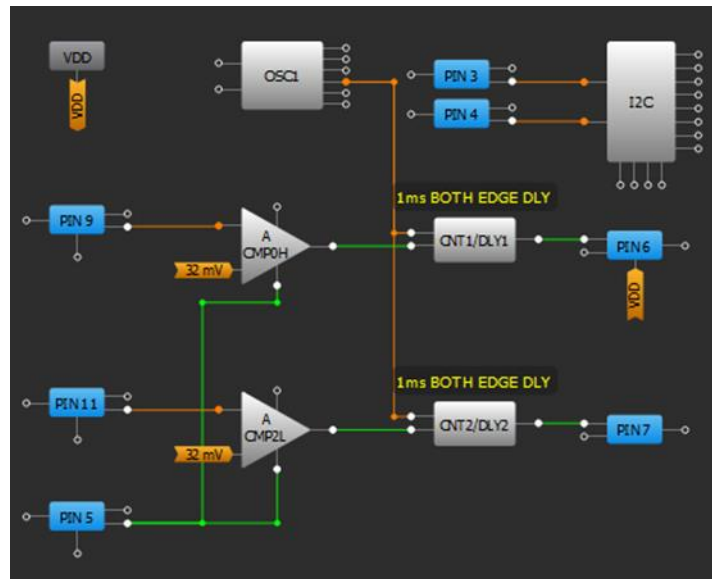
#### Functional Blocks Affected: All ACMPs

##### Description:

There is some noise coupling from the Vrefs of high-speed ACMPs to the low-power bandgap (BG) while the high-speed ACMPs Vref is turning on and off.

##### Workaround:

There is no issue with manually powering up the low-speed ACMPs. If you are manually powering up the high-speed ACMPs via the "PWR UP" connector, you should add a 1 ms delay to the output of all of the ACMPs used in the design.



### ISSUE 3: Unstable Vref Output Buffer

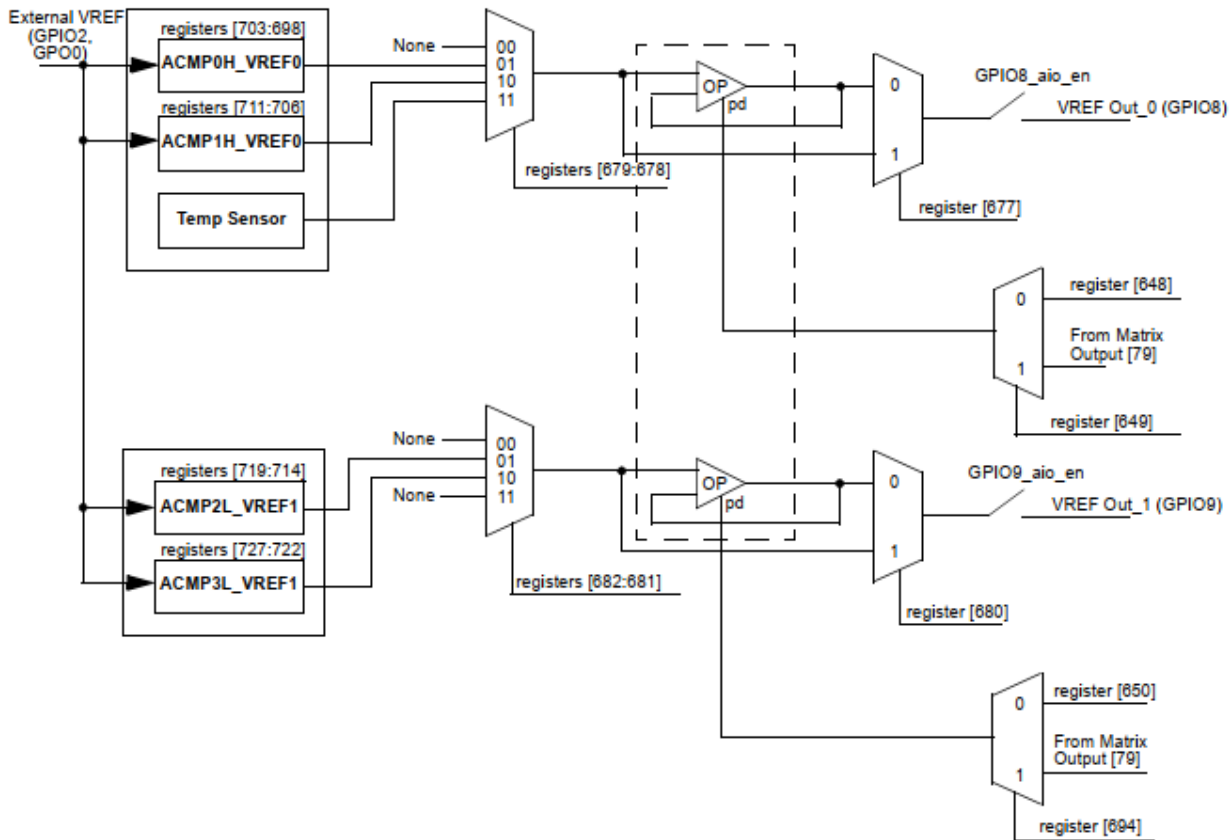
#### Functional Blocks Affected: Both Vref Output

##### Description:

For systems where  $V_{DD} = 2.5\text{ V}$ , the Vref output buffer will be unstable if the output voltage is around  $0.5 \times V_{DD}$ .

##### Workaround:

For a system where  $V_{DD} = 2.5\text{ V}$ , bypass the buffer if the output voltage of the Vref buffer is within  $(0.5 \times V_{DD}) \pm 0.4$ . Check the Vref section of the device datasheet to see which registers need to be modified.



### ISSUE 4: Incorrect Data Write Functional Blocks Affected: I<sup>2</sup>C

#### Description:

When performing a masked I<sup>2</sup>C write, unchanged bits in the 8-bit I<sup>2</sup>C bus may be coupled to the changed bits due to the large coupling capacitor between the I<sup>2</sup>C bus bits, leading to incorrect data being written.

#### Workaround:

There is no workaround, but this will be fixed in the next silicon revision.

### ISSUE 5: Leakage from ACMP IN+ to Analog Input Pins Functional Blocks Affected: GPIO10/11, GPO5/6, ACMP0/1H, ACMP2/3L

#### Description:

When configured in “Analog IO” mode, GPIO10/11 and GPO5/6 can experience abnormal leakage behavior. This behavior occurs when multiple input sources are simultaneously connected to the ACMP IN+ port. Each of the 4 ACMPs has an input MUX which selects the IN+ source for the comparator. The MUX options are shown in the table below.

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Table 1: ACMP Input Options

ACMP IN+ MUX Options	
ACMP0H	GPIO10 Buffered GPIO10 V <sub>DD</sub>
ACMP1H	GPIO11 Buffered GPIO11 ACMP0H IN+ source
ACMP2L	GPO5 ACMP0H IN+ source ACMP1H IN+ source
ACMP3L	GPO6 ACMP2L IN+ source VREF0 OUT

In the GreenPAK Designer, the input source is selected by the IN+ source dropdown within the ACMP's properties window. When an input source is selected and the ACMP is enabled, an analog switch connects the source to the ACMP's IN+ port. If multiple sources are connected to the ACMP's IN+ port, there will be leakage between the sources.

The GPIOs shown above can be repurposed as Digital IOs if the ACMPs are disabled or if another input source is selected for the ACMP by the IN+ input MUX. Whenever a GPIO input mode is configured as an "Analog IO" in accordance with the register definition below, the GPIO will be connected to the ACMP's IN+ port through an internal switch.

Table 2: GPIO Input Mode Configurations

Byte	Register Bit	Signal Function	Register Bit Definition
<b>GPIO10</b>			
6B	863	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
6C	864		
<b>GPIO11</b>			
6C	871	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
6D	872		

Some Analog IOs can only be repurposed as Digital Outputs. For these GPOs, the PIN will be connected to the ACMP's IN+ port through an internal switch if the output mode configuration is disabled as shown in the table below.

Table 3: GPO Input Mode Configuration

Byte	Register Bit	Signal Function	Register Bit Definition
<b>GPO5</b>			
6E	885	Output Mode Configuration	0: Disable (Analog IO) 1: Enable (Digital Output)
<b>GPO6</b>			
6F	892	Output Mode Configuration	0: Disable (Analog IO) 1: Enable (Digital Output)

There are 3 GPIO settings and 2 GPO settings that use the "Analog IO" configuration. The GPIO settings include Analog input/output, Digital input/output (with "Input mode" set to Analog input), and Digital output (with "Output mode" set to 1/2/4x 3-State Output). The first setting is reserved for use with the ACMP, but the other two settings use the "Analog IO" configuration as a high-impedance input. The GPO settings include Analog input/output and Pin not used. As one would expect, the first configuration is used with the ACMP, but when the GPO is not being used, the PIN is also configured as an "Analog IO".

It is important to note that these input modes won't be high impedance if the ACMP is enabled and connected to another input source. When two signals are connected to the ACMP's IN+ source, the voltage level at the ACMP's input depends upon the drive strength of the competing sources.

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Figure 1 shows the GreenPAK configured with GPIO10 as a Digital IO with a 1 MΩ pull down resistor. Since the OE pin is connected to 0 V, this pin is acting as an “Analog IO.” As seen in Table 1, GPIO10 and V<sub>DD</sub> are both input options for ACMP0H. In this example, GPIO0 is being used as a digital input to enable and disable the ACMP.

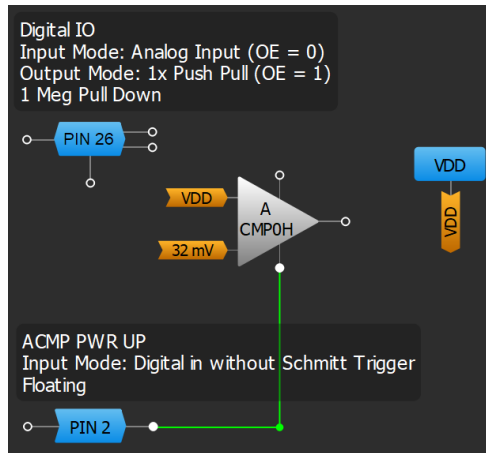


Figure 1: GreenPAK Input Structure Test Schematic

Figure 2 shows that GPIO10 in analog input mode is pulled HIGH by the V<sub>DD</sub> signal whenever the ACMP is enabled despite having an internal pull down resistor. This behavior is caused by an internal connection between V<sub>DD</sub> and GPIO10. Similar behavior can be reproduced when one ACMP’s IN+ port is connected to another ACMP’s IN+ port.

CH1 (Yellow): ACMP PWR UP (GPIO0)  
 CH3 (Light Blue): Digital IO w/ Analog Input Mode Configuration (GPIO10)

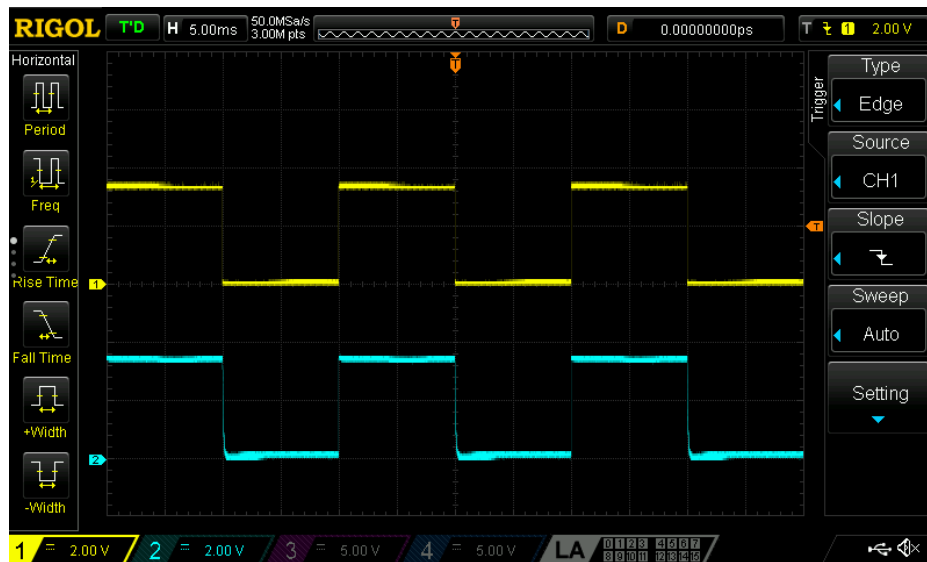


Figure 2: ACMP Input Structure Behavior

**Workaround:**

If an ACMP is disabled, the PIN associated with that ACMP will operate as expected under any configuration. Please reference Table 1 for more information regarding which GPIOs and GPOs are associated with which ACMPs.

When the ACMPs are enabled, it is possible to inadvertently connect multiple ACMP sources together through the input structure. This is possible when the ACMP input is connected to a source other than its analog PIN, but that PIN is still set as an “Analog IO”.

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There is no workaround for this behavior. With this in mind, the GPIOs should not be used as digital IOs (with “Input mode” set to Analog input) or as digital outputs (with “Output mode” set to 1/2/4x 3-State Output) if the respective ACMP is enabled and connected to another input source. Under these same ACMP conditions, the system designer should be aware that the GPOs listed in [Table 1](#) will be connected to their respective ACMP IN+ sources if configured as “PIN not used.”

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