SLG4X42522-A

GreenPAK ™

Voltage Monitor

General Description

Dialog SLG4X42522-A is a low power and small form device. The SoC is housed in a 6.5mm x 6.4mm TSSOP package which is optimal for using with small devices.

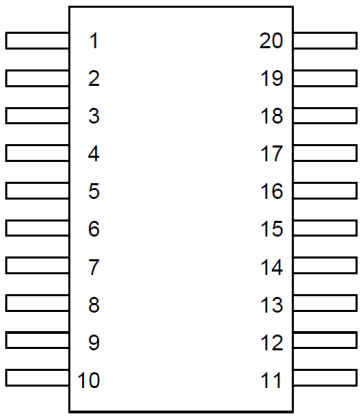
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- TSSOP - 20 Package

Output Summary

5 Outputs - Open Drain NMOS 1X
2 Outputs - Push Pull 1X

Pin Configuration



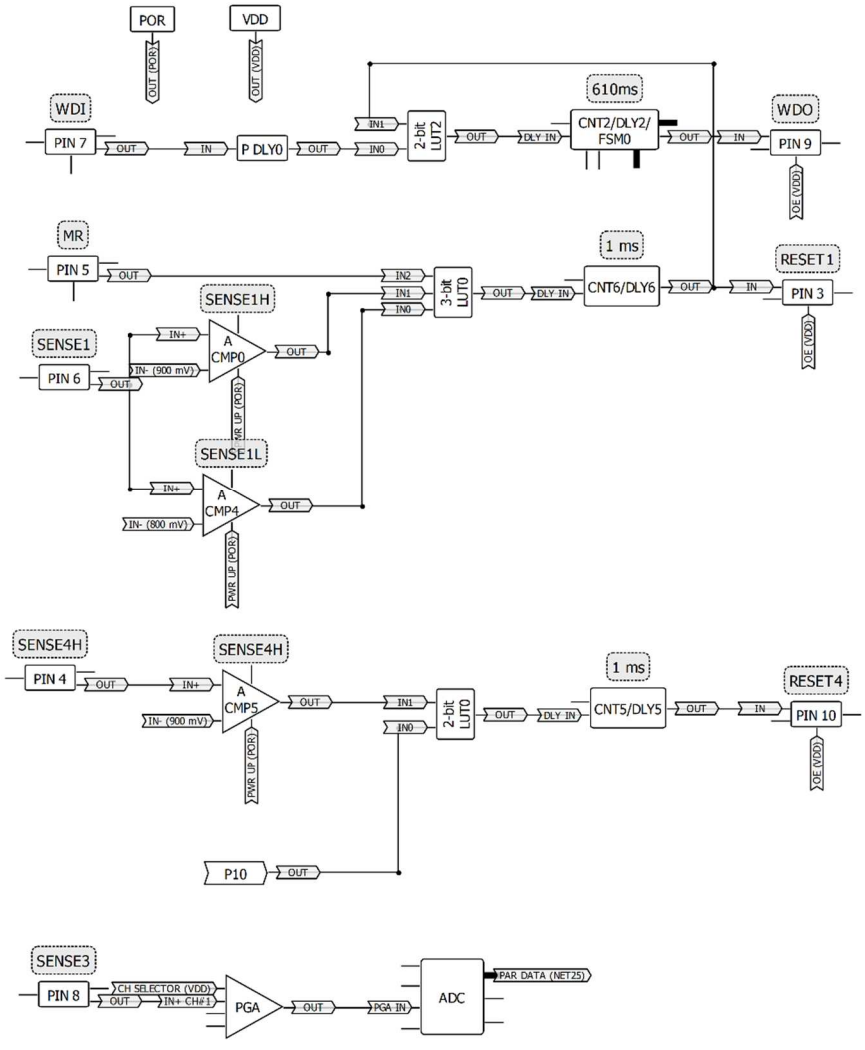
TSSOP-20
(Top View)

Pin name

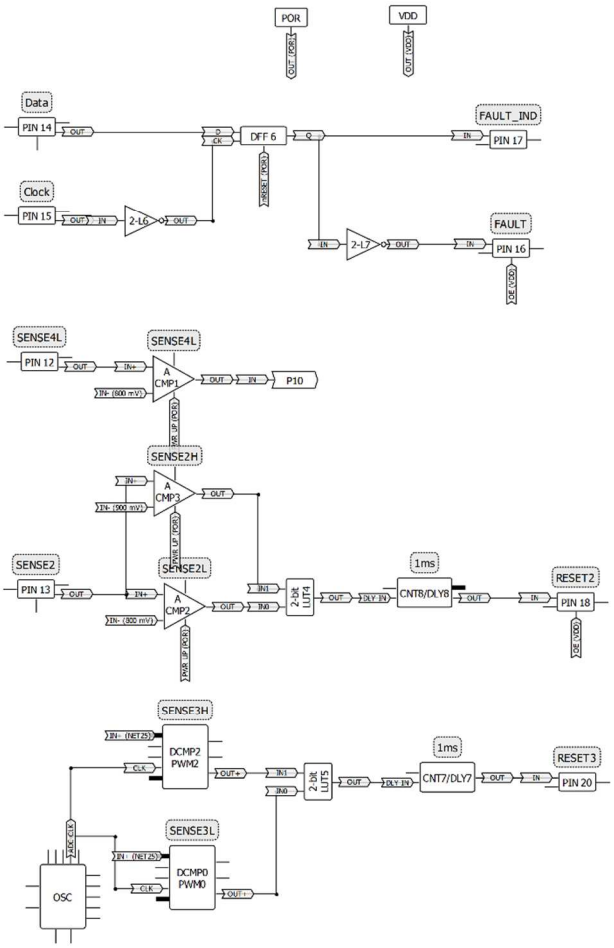
Pin #	Pin name	Pin #	Pin name
1	VDD	11	GND
2	NC	12	SENSE4L
3	RESET1	13	SENSE2
4	SENSE4H	14	Data
5	MR	15	Clock
6	SENSE1	16	FAULT
7	WDI	17	FAULT_IND
8	SENSE3	18	RESET2
9	WDO	19	NC
10	RESET4	20	RESET3

Block Diagram

Matrix0



Matrix1


POR
VDD
Data
PIN 14
DFF 6
FAULT_IND
PIN 17
Clock
PIN 15
2-LG
2-L7
FAULT
PIN 16
SENSE4L
PIN 12
CMP1
P10
SENSE2H
CMP3
SENSE2
PIN 13
SENSE2L
CMP2
2-bit LUT4
1ms
CNTR/DLY8
RESET2
PIN 18
SENSE3H
DCMP2 PWM2
2-bit LUT5
CNT7/DLY7
RESET3
PIN 20
SENSE3L
DCMP0 PWM0
OSC

Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	NC	--	Keep Floating or Connect to GND	--
3	RESET1	Digital Output	Open Drain NMOS 1X	floating
4	SENSE4H	Analog Input/Output	Analog Input/Output	floating
5	MR	Digital Input	Digital Input without Schmitt trigger	floating
6	SENSE1	Analog Input/Output	Analog Input/Output	floating
7	WDI	Digital Input	Digital Input without Schmitt trigger	floating
8	SENSE3	Analog Input/Output	Analog Input/Output	floating
9	WDO	Digital Output	Open Drain NMOS 1X	floating
10	RESET4	Digital Output	Open Drain NMOS 1X	floating
11	GND	GND	Ground	--
12	SENSE4L	Analog Input/Output	Analog Input/Output	floating
13	SENSE2	Analog Input/Output	Analog Input/Output	floating
14	Data	Digital Input	Digital Input without Schmitt trigger	floating
15	Clock	Digital Input	Digital Input without Schmitt trigger	floating
16	FAULT	Digital Output	Push Pull 1X	floating
17	FAULT_IND	Digital Output	Push Pull 1X	floating
18	RESET2	Digital Output	Open Drain NMOS 1X	floating
19	NC	--	Keep Floating or Connect to GND	--
20	RESET3	Digital Output	Open Drain NMOS 1X	floating

Ordering Information

Part Number	Package Type
SLG4X42522-AG	20-pin TSSOP
SLG4X42522-AGTR	20-pin TSSOP - Tape and Reel (4k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5V	VDD + 0.5V	V
PGA Input voltage	Single-ended	--	1.98/G	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	10	mA
	OD 1x	--	14	
Current at Input Pin		-1.0	1.0	mA
ACMP Input Leakage	Vin = 0 V	--	0.29	nA
	Vin = VDD	--	0.92	
PGA Input Leakage	Vin = 0 V	--	0.13	nA
	Vin = VDD	--	0.49	
Logic Input without Schmitt Trigger(Floating) Leakage	Vin = 0 V	--	0.39	nA
	Vin = VDD	--	142.92	
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

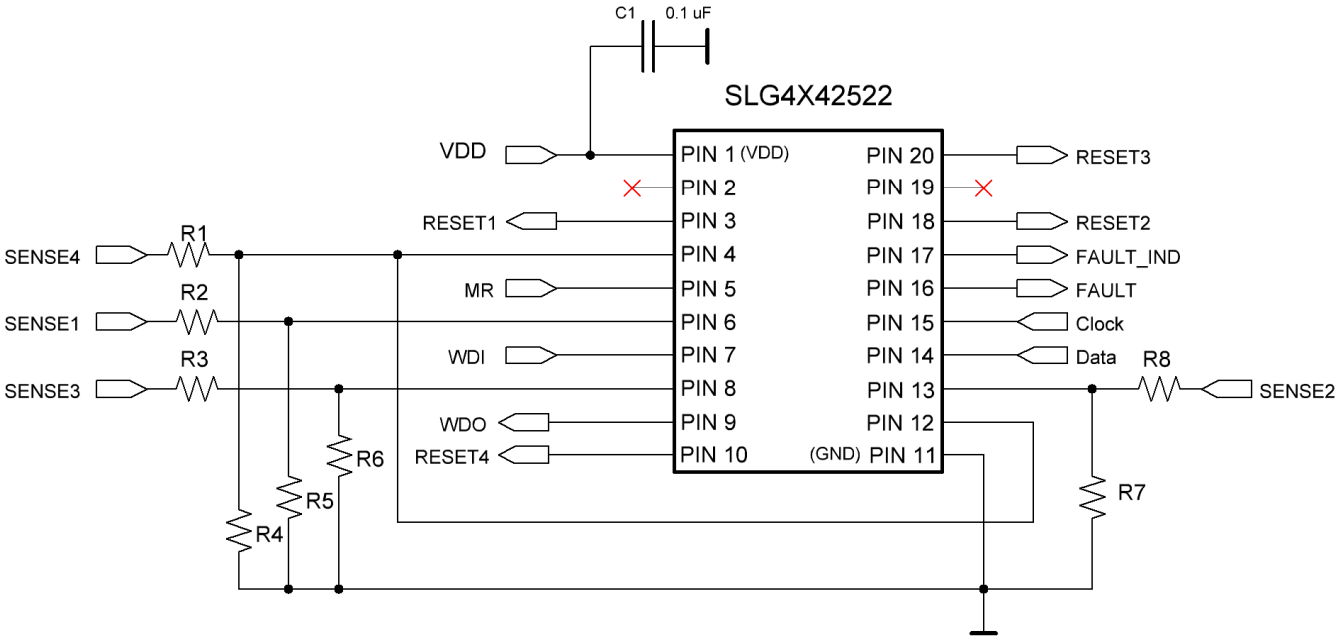
Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	3.3	3.6	V
T_A	Operating Temperature		-40	25	105	°C
I_Q	Quiescent Current	Static inputs and floating outputs	--	200	--	µA
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	21	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	69	mA
		T_J = 110°C	--	--	33	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=1.8V	1.087	--	VDD	V
		Logic Input at VDD=3.3V	1.949	--	VDD	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=1.8V	0	--	0.759	V
		Logic Input at VDD=3.3V	0	--	1.286	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, IOH=100µA at VDD=1.8V	1.680	1.788	--	V
		Push-Pull 1X, IOH=3mA at VDD=3.3V	2.713	3.095	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=100µA, at VDD=1.8V	--	0.010	0.015	V

		Push-Pull 1X, I_{OL}=3mA, at VDD=3.3V	--	0.148	0.228	V
		Open Drain NMOS 1X, I_{OL}=100µA, at VDD=1.8V	--	0.007	0.010	V
		Open Drain NMOS 1X, I_{OL}=3mA, at VDD=3.3V	--	0.080	0.147	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, VOH=VDD-0.2V at VDD=1.8V	1.027	1.703	--	mA
		Push-Pull 1X, VOH=2.4V at VDD=3.3V	5.608	10.774	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL}=0.15V, at VDD=1.8V	0.917	1.660	--	mA
		Push-Pull 1X, V_{OL}=0.4V, at VDD=3.3V	4.875	7.795	--	mA
		Open Drain NMOS 1X, V_{OL}=0.15V, at VDD=1.8V	1.375	2.534	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V	7.313	12.370	--	mA
T_{DLY2}	Delay2 Time	At temperature 25°C	518	621	725	ms
		At temperature -40 +105°C	381	670	960	
T_{DLY5}	Delay5 Time	At temperature 25°C	816	1002	1188	µs
		At temperature -40 +105°C	600	1087	1574	
T_{DLY6}	Delay6 Time	At temperature 25°C	816	1002	1188	µs
		At temperature -40 +105°C	600	1087	1574	
T_{DLY7}	Delay7 Time	At temperature 25°C	816	1002	1188	µs
		At temperature -40 +105°C	600	1087	1574	
T_{DLY8}	Delay8 Time	At temperature 25°C	816	1002	1188	µs
		At temperature -40 +105°C	600	1087	1574	
V_{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature 25°C	891	900	914	mV
		Low to High transition, at temperature -40 +105°C	888	900	917	mV
		High to Low transition, at temperature 25°C	890	900	914	mV
		High to Low transition, at temperature -40 +105°C	887	900	915	mV
V_{ACMP1}	Analog Comparator1 Threshold Voltage	Low to High transition, at temperature 25°C	791	800	813	mV
		Low to High transition, at temperature-40 +105°C	789	800	816	mV
		High to Low transition, at temperature 25°C	790	800	813	mV
		High to Low transition, at temperature-40 +105°C	788	800	814	mV
V_{ACMP2}	Analog Comparator2 Threshold Voltage	Low to High transition, at temperature 25°C	791	800	813	mV
		Low to High transition, at temperature-40 +105°C	789	800	816	mV
		High to Low transition, at temperature 25°C	790	800	813	mV
		High to Low transition, at temperature-40 +105°C	788	800	814	mV

V_{ACMP3}	Analog Comparator3 Threshold Voltage	Low to High transition, at temperature 25°C	891	900	914	mV
		Low to High transition, at temperature-40 +105°C	888	900	917	mV
		High to Low transition, at temperature 25°C	890	900	914	mV
		High to Low transition, at temperature -40 +105°C	887	900	915	mV
V_{ACMP4}	Analog Comparator4 Threshold Voltage	Low to High transition, at temperature 25°C	791	800	813	mV
		Low to High transition, at temperature-40 +105°C	789	800	816	mV
		High to Low transition, at temperature 25°C	790	800	813	mV
		High to Low transition, at temperature-40 +105°C	788	800	814	mV
V_{ACMP5}	Analog Comparator5 Threshold Voltage	Low to High transition, at temperature 25°C	891	900	914	mV
		Low to High transition, at temperature-40 +105°C	888	900	917	mV
		High to Low transition, at temperature 25°C	890	900	914	mV
		High to Low transition, at temperature-40 +105°C	887	900	915	mV
V_{DCMP0}	DCMP0 Threshold Voltage	Low to High transition	--	--	819	mV
		High to Low transition	782	--	--	
V_{DCMP2}	DCMP2 Threshold Voltage	Low to High transition	--	--	917	mV
		High to Low transition	884	--	--	
T_{SU}	Startup Time (see Note 3)	From VDD rising past PON_{THR}	0.660	1.4	3.740	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	0.953	1.462	1.707	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.935	1.103	1.281	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, pins 12, 13, 14, 15, 16, 17, 18, 19 and 20 to another.
3. VDD ramp rising speed must be less than 0.6 V/µs after power on. Violating this specification may cause chip to restart.

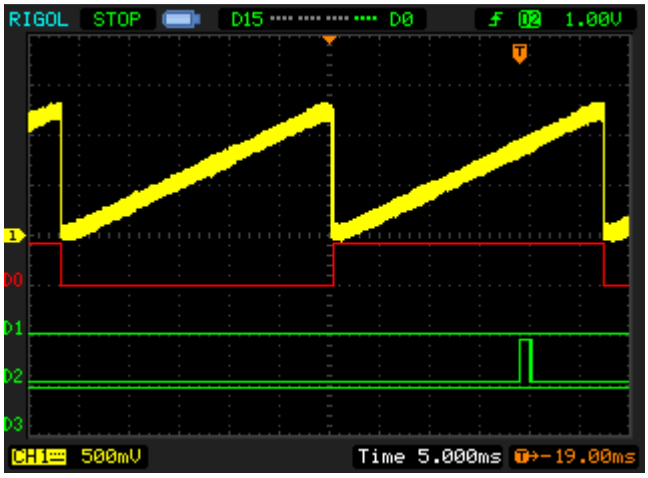
Typical Application Circuit



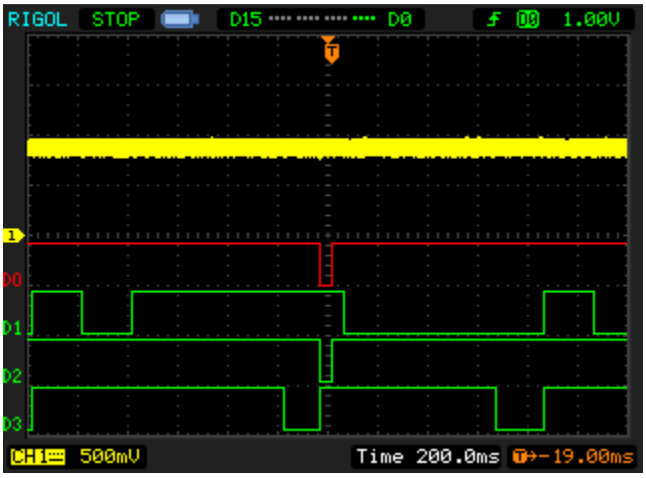
Functionality Waveforms

Channel 1 (yellow/top line) – PIN#6 (SENSE1)
D0 – PIN#5 (MR)
D1 – PIN#7 (WDI)
D2 – PIN#3 (RESET1) with external 5kΩ pull up resistor
D3 – PIN#9 (WDO) with external 5kΩ pull up resistor

1. RESET1 functionality

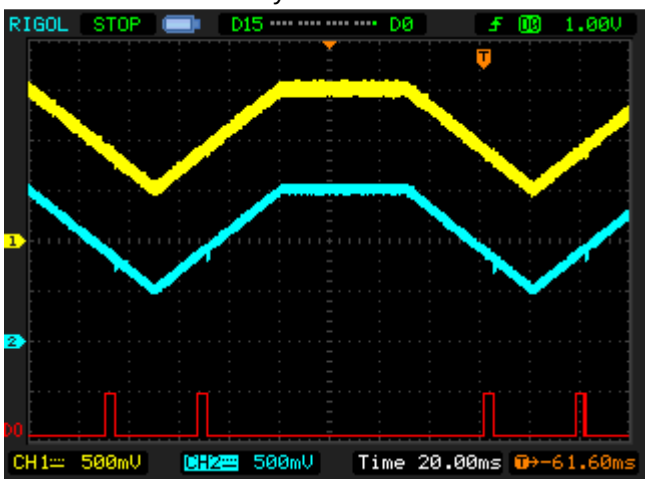


2. WDO functionality



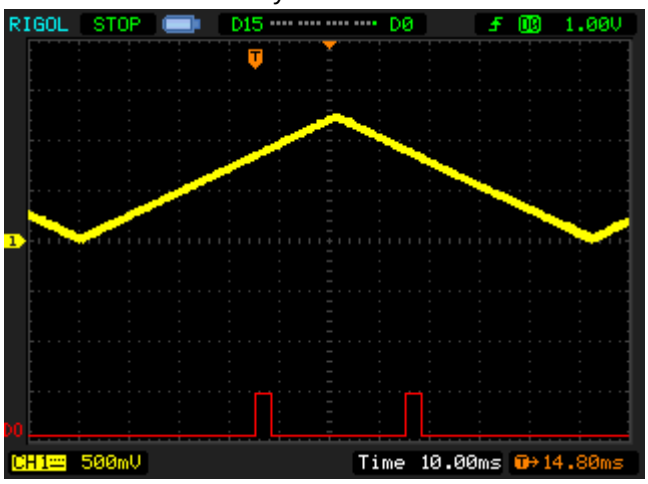
Channel 1 (yellow/top line) – PIN#4 (SENSE4H)
Channel 2 (light blue/2nd line) – PIN#12 (SENSE4L)
D0 – PIN#10 (RESET4) with external 5kΩ pull up resistor

3. RESET4 functionality



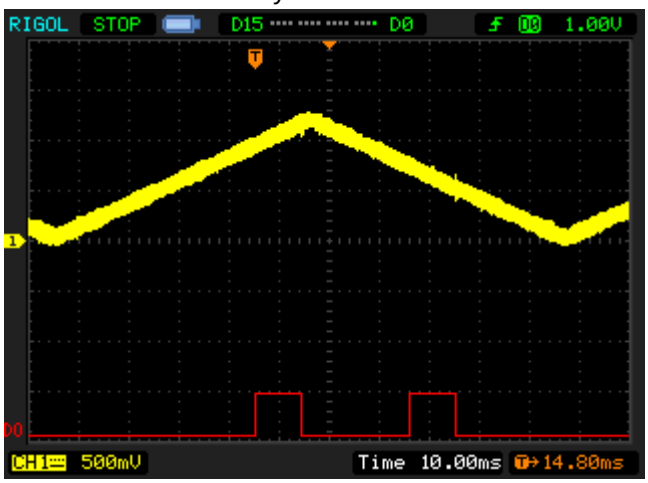
Channel 1 (yellow/top line) – PIN#13 (SENSE2)
D0 – PIN#18 (RESET2) with external 5kΩ pull up resistor

4. RESET2 functionality



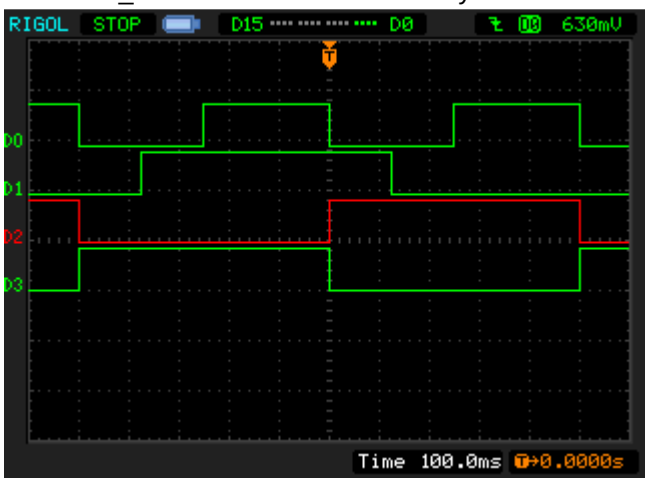
Channel 1 (yellow/top line) – PIN#8 (SENSE3)
D0 – PIN#20 (RESET3) with external 5kΩ pull up resistor

5. RESET3 functionality

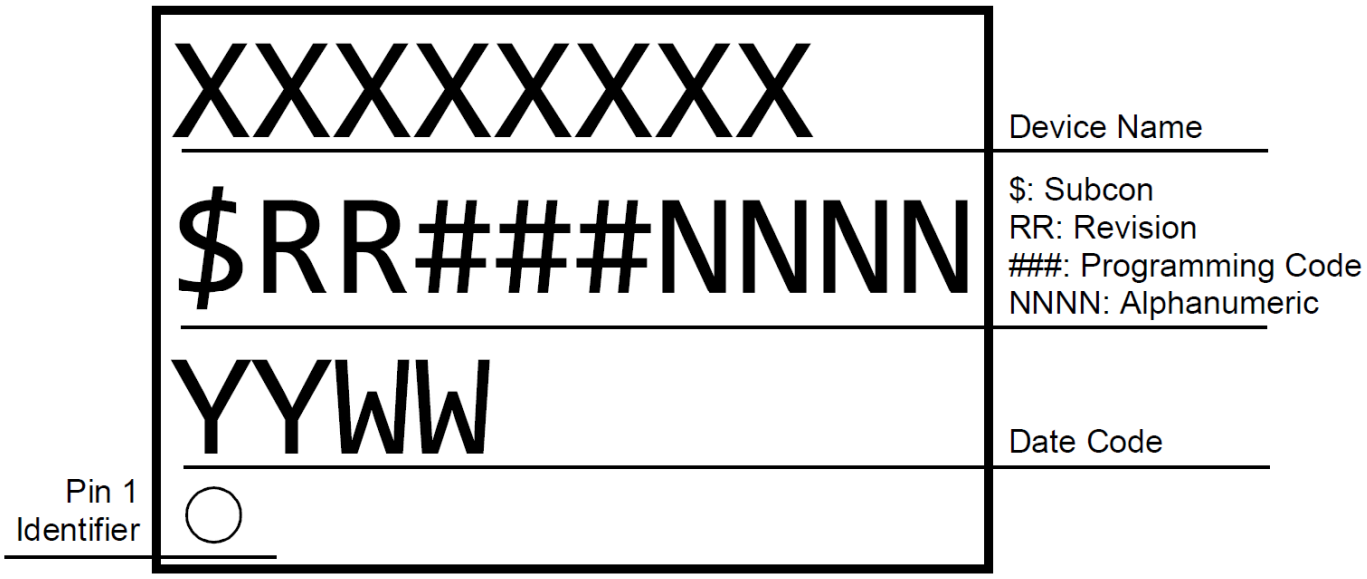


D0 – PIN#15 (Clock)
D1 – PIN#14 (Data)
D2 – PIN#17 (FAULT_IND)
D3 – PIN#16 (FAULT)

6. FAULT_IND and FAULT functionality



Package Top Marking

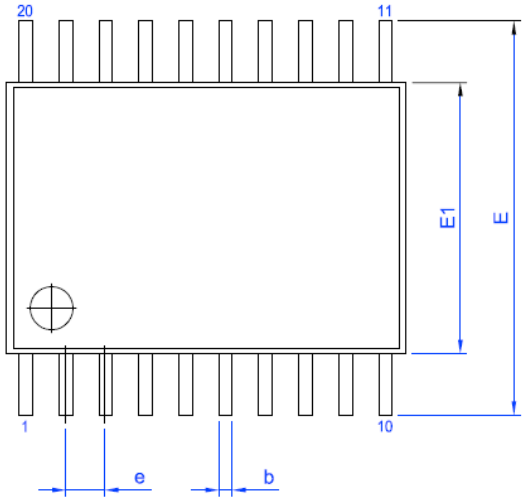


Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.10	001	U	0x2FB67D3E			08/15/2019

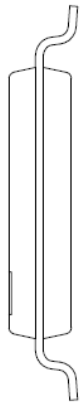
The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

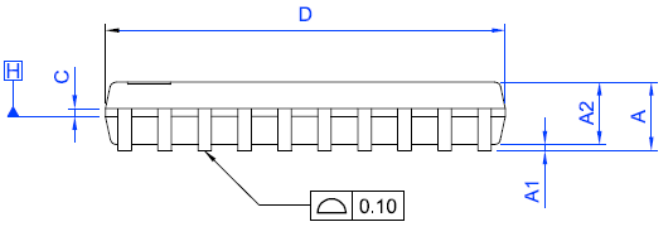
TSSOP 20L 173 MIL Green Package



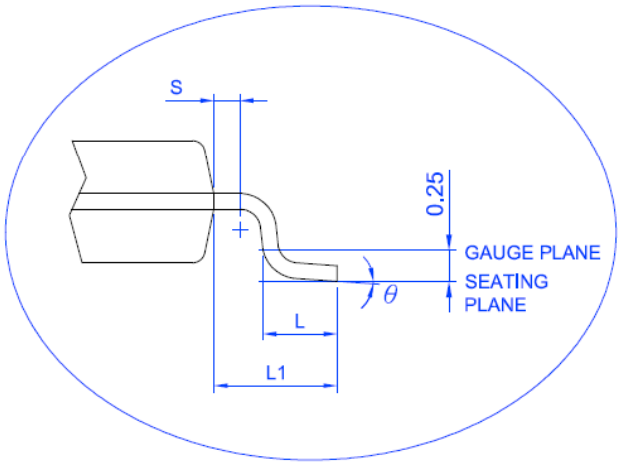
Marking View



Side View



Side View



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	-	-	1.20	D	6.40	6.50	6.60
A1	0.05	-	0.15	E1	4.30	4.40	4.50
A2	0.80	0.90	1.05	E	6.40 BSC		
b	0.19	-	0.30	L	0.50	0.60	0.75
C	0.09	-	0.20	L1	1.00 REF		
e	0.65 BSC			S	0.20	-	-
				Θ	0°	-	8°

NOTES:

1.JEDEC OUTLINE :
STANDARD : MO-153 AC REV.F
THERMALLY ENHANCED : MO-153 ACT REV.F

2.DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.

3.DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

4.DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.

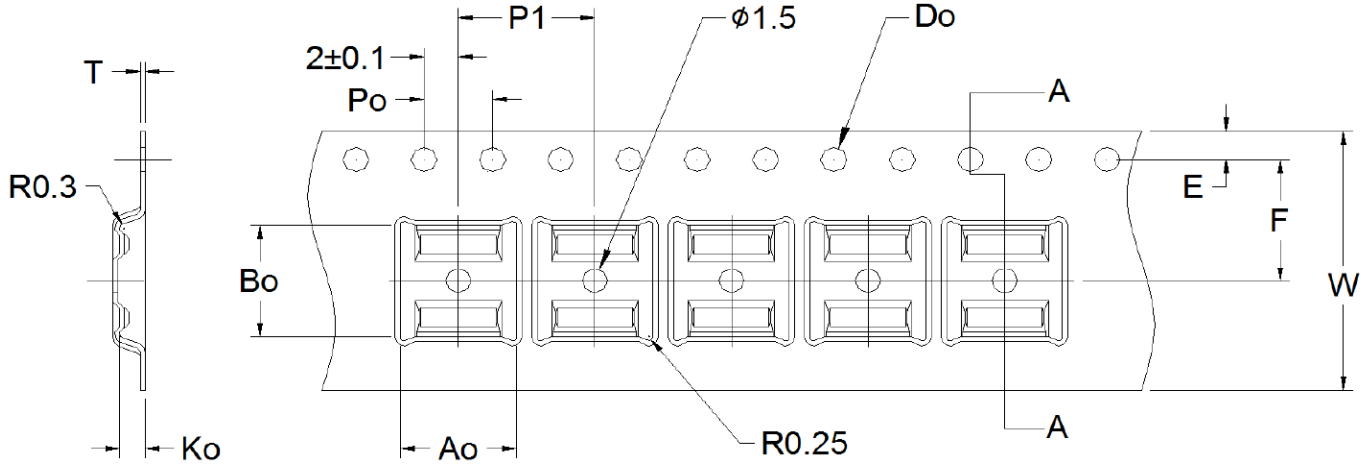
5.DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TSSOP 20L 173 MIL Green Package	20	6.5 x 6.4	4000	4000	330 / 100	42	336	42	TSSOP 20L 173 MIL Green Package	20	6.5 x 6.4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TSSOP 20L 173 MIL Green Package	6.8	6.9	1.6	4	8	1.5	1.75	7.5	16

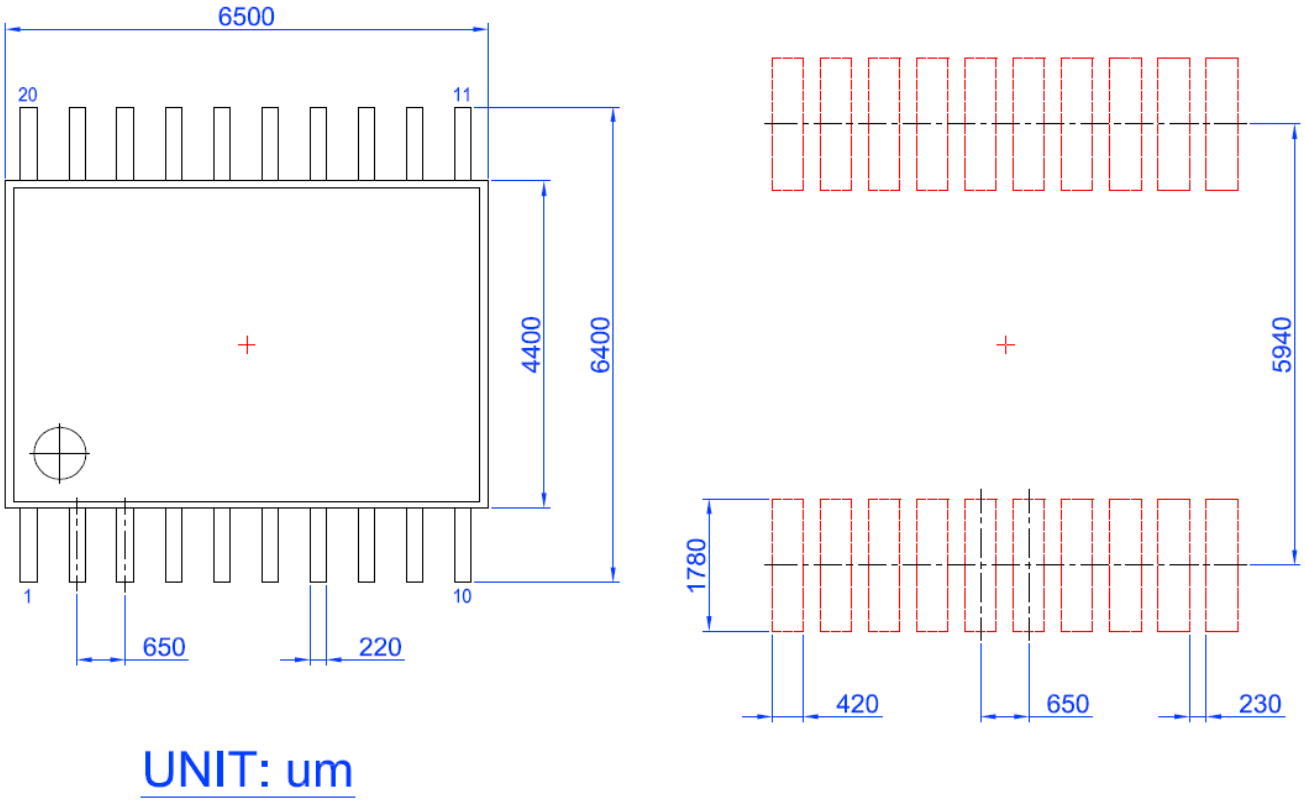


Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 25.74 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern



UNIT: um

Datasheet Revision History

Date	Version	Change
08/15/2019	0.10	New design for SLG46620-AG chip

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