# An Ultra-small, 22.5 mΩ, 2.5 A Load Switch with Reverse Blocking

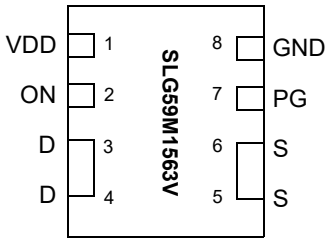
## General Description

The SLG59M1563V is a 22.5 mΩ, 2.5 A single-channel load switch that is able to switch 1 V to 5 V power rails. The product is packaged in an ultra-small 1.0 x 1.6 mm package.

## Features

- 1.0 x 1.6 x 0.55 mm STDFN 8L package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- 22.5 mΩ $RDS_{ON}$ while supporting 2.5 A
- Power Good Output
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -40 °C to 85°C
- Operating Voltage: 1.5 V to 5.5 V

## Pin Configuration

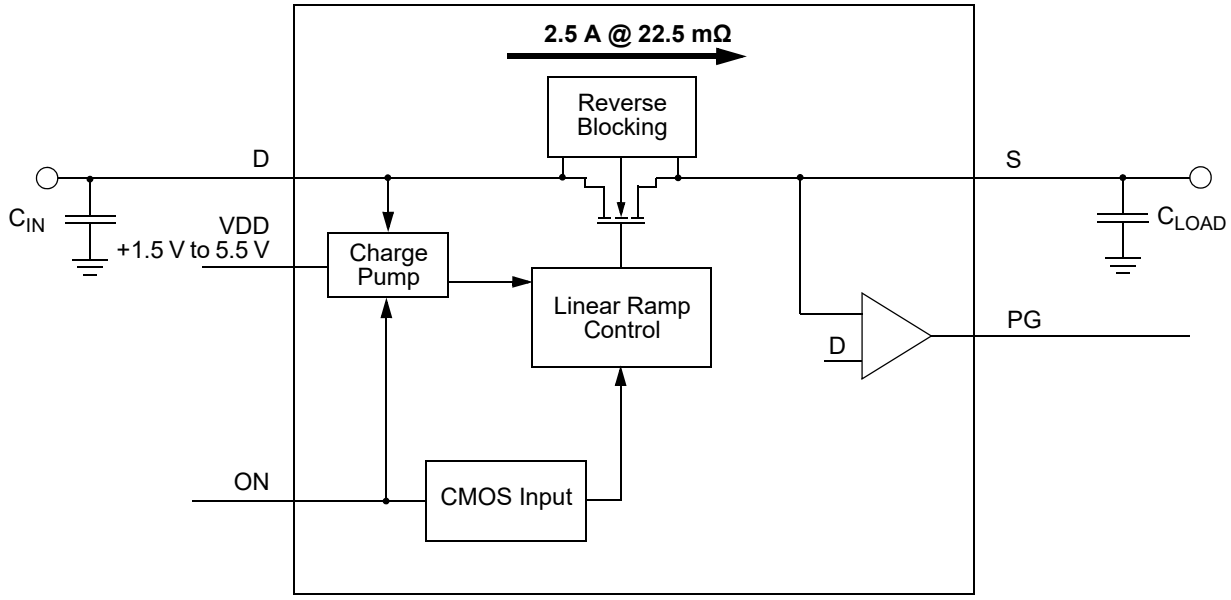



**8-pin FC-TDFN**
(Top View)

## Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

## Block Diagram



## Pin Description

| Pin # | Pin Name | Type | Pin Description |
|---|---|---|---|
| 1 | VDD | Power | VDD supplies the power for the operation of the power switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor. |
| 2 | ON | Input | A low-to-high transition on this pin initiates the operation of the SLG59M1563V's state machine. ON is a CMOS input with ON_$V_{IL}$ < 0.3 V and ON_$V_{IH}$ > 0.85 V thresholds. While there is an internal pull-down circuit to GND (~4 MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller. |
| 3, 4 | D | MOSFET | Drain terminal connection of the n-channel MOSFET (2 pins fused for D). Connect at least a low-ESR 0.1 µF capacitor from this pin to ground. Capacitors used at D should be rated at 10 V or higher. |
| 5, 6 | S | MOSFET | Source terminal connection of the n-channel MOSFET (2 pins fused for S). Connect a low-ESR capacitor from this pin to ground and consult the Electrical Characteristics table for recommended $C_{LOAD}$ range. Capacitors used at S should be rated at 10 V or higher. |
| 7 | PG | Output | A push pull output. PG is asserted HIGH when $V_S$ > 95% of $V_D$. |
| 8 | GND | GND | Ground connection. Connect this pin to system analog or power ground plane. |

## Ordering Information

| Part Number | Type | Production Flow |
|---|---|---|
| SLG59M1563V | STDFN 8L | Industrial, -40 °C to 85 °C |
| SLG59M1563VTR | STDFN 8L (Tape and Reel) | Industrial, -40 °C to 85 °C |

## Absolute Maximum Ratings

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply | | -- | -- | 7 | V |
| $T_S$ | Storage Temperature | | -65 | -- | 150 | °C |
| $ESD_{HBM}$ | ESD Protection | Human Body Model | 2000 | -- | -- | V |
| $W_{DIS}$ | Package Power Dissipation | | -- | -- | 0.4 | W |
| MOSFET $IDS_{PK}$ | Peak Current from Drain to Source | For no more than 1 ms with 1% duty cycle | -- | -- | 3.5 | A |

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics

$T_A$ = -40 °C to 85 °C unless otherwise noted. Typical values are at $T_A$ = 25 °C, unless otherwise noted.

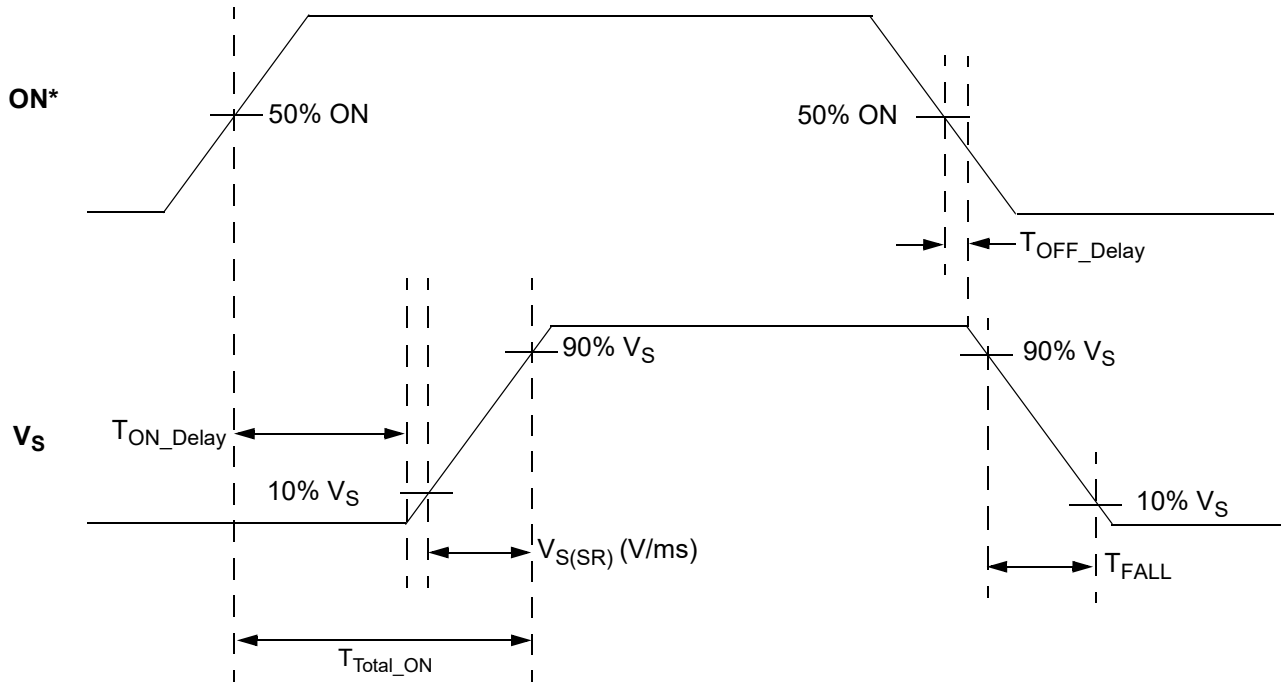
| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | -40 °C to 85 °C | 1.5 | -- | 5.5 | V |
| $I_{DD}$ | Power Supply Current (PIN 1) | when OFF | -- | -- | 1 | µA |
| | | when ON, No load | -- | 14 | 30 | µA |
| $RDS_{ON}$ | ON Resistance | $T_A$ = 25 °C; $I_{DS}$ = 100 mA | -- | 22.5 | 25 | mΩ |
| | | $T_A$ = 85 °C; $I_{DS}$ = 100 mA | -- | 25.6 | 30 | mΩ |
| MOSFET IDS | Current from D to S | Continuous | -- | -- | 2.5 | A |
| $I_{REVERSE}$ | MOSFET Reverse Leakage Current | $V_S$ = 1.0 V to 5.5 V, $V_D$ = 0 V, ON = 0 V; $V_{DD}$ = 1.5 V to 5.5 V; $T_A$ = 25 °C | -- | 0.04 | 0.55 | µA |
| | | $V_S$ = 1.0 V to 5.5 V, $V_D$ = 0 V, ON = 0 V $V_{DD}$ = 1.5 V to 5.5 V; $T_A$ = 85 °C | -- | 0.26 | 1.3 | µA |
| | | $V_S$ = 1.0 V to 5.5 V, $V_D$ = 0 V, ON = 0 V $V_{DD}$ = 1.5 V to 5.5 V; $T_A$ = -40 °C | -- | 0.31 | 9.70 | µA |
| $V_D$ | Drain Voltage | | 1.0 | -- | $V_{DD}$ | V |
| $T_{ON\_Delay}$ | ON Delay Time | 50% ON to $V_S$ Ramp Start | -- | 300 | 500 | µs |
| $T_{Total\_ON}$ | Total Turn On Time | 50% ON to 90% $V_S$; Example: $V_{DD}$ = $V_D$ = 5 V, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 20 Ω | 2.1 | 2.6 | 3.1 | ms |
| $V_{S(SR)}$ | Slew Rate | 10% $V_S$ to 90% $V_S$; Example: $V_{DD}$ = $V_D$ = 5 V, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 20 Ω | 1.4 | 1.95 | 2.2 | V/ms |
| $C_{LOAD}$ | Output Load Capacitance | $C_{LOAD}$ connected from S to GND | -- | -- | 500 | µF |
| $ON\_V_{IH}$ | High Input Voltage on ON pin | | 0.85 | -- | $V_{DD}$ | V |
| $ON\_V_{IL}$ | Low Input Voltage on ON pin | | -0.3 | 0 | 0.3 | V |
| $V_{OL}$ | Low Output Voltage on PG pin | $V_{DD}$ = 5 V, $I_{OL}$ = -0.1 mA | -- | -- | 0.4 | V |
| $V_{OH}$ | High Output Voltage on PG pin | $V_{DD}$ = 5 V, $I_{OH}$ = 0.1 mA | $V_{DD}$-0.4 | -- | $V_{DD}$ | V |
| $THERM_{ON}$ | Thermal shutoff turn-on temperature | | -- | 125 | -- | °C |
| $THERM_{OFF}$ | Thermal shutoff turn-off temperature | | -- | 100 | -- | °C |
| $THERM_{TIME}$ | Thermal shutoff time | | -- | -- | 1 | ms |
| $T_{OFF\_Delay}$ | OFF Delay Time | 50% ON to $V_S$ Fall Start; $V_{DD}$ = $V_D$ = 5 V; $R_{LOAD}$ = 20 Ω; no $C_{LOAD}$ | -- | 8 | -- | µs |

## Electrical Characteristics (continued)

$T_A$ = -40 °C to 85 °C unless otherwise noted. Typical values are at $T_A$ = 25 °C, unless otherwise noted.

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $PG_{TRIGGER}$ | Power Good Trigger Level | $V_S$ % of $V_D$ | -- | 95 | -- | % |

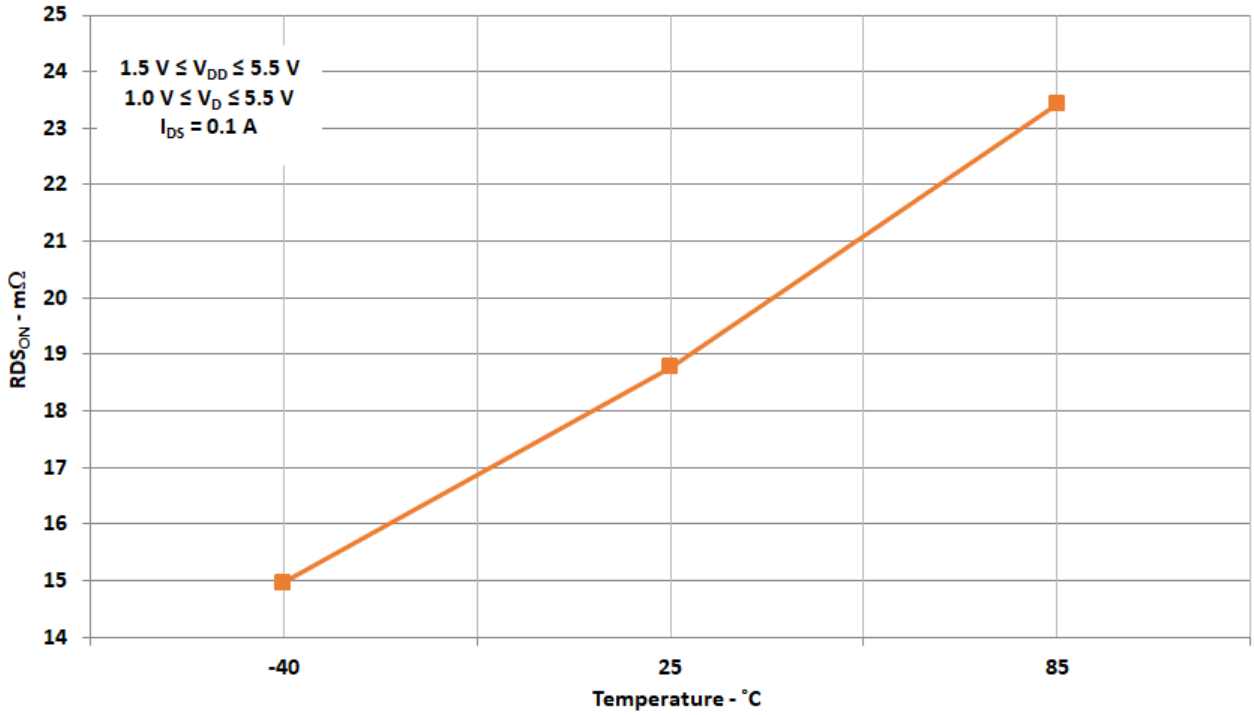
## $T_{ON\_Delay}$, $V_{S(SR)}$, and $T_{Total\_ON}$ Timing Details




Note: * Rise and Fall times of the ON signal are 100 ns

## Typical Performance Characteristics

### $RDS_{ON}$ vs. Temperature, $V_{DD}$, and $V_{IN}$



## SLG59M1563V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply $V_{DD}$ first, followed by $V_D$ after $V_{DD}$ exceeds 1 V. Then allow $V_D$ to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If $V_{DD}$ and $V_D$ need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 µF $C_{LOAD}$ will prevent glitches for rise times of $V_{DD}$ and $V_D$ less than 2 ms.

If the ON pin is toggled HIGH before $V_{DD}$ and $V_D$ have reached their steady-state values, the IPS timing parameters may differ from datasheet specifications.

## Layout Guidelines:

1. The VDD pin needs a 0.1 µF and 10 µF external capacitors to smooth pulses from the power supply. Locate these capacitors as close as possible to the SLG59M1563V's PIN1.

2. Since the D and S pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 1, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input $C_{IN}$ and output $C_{LOAD}$ low-ESR capacitors as close as possible to the SLG59M1563V's D and S pins;

4. The GND pin should be connected to system analog or power ground plane.

## SLG59M1563V Evaluation Board:

A GFET3 Evaluation Board for SLG59M1563V is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for $RDS_{ON}$ evaluation.

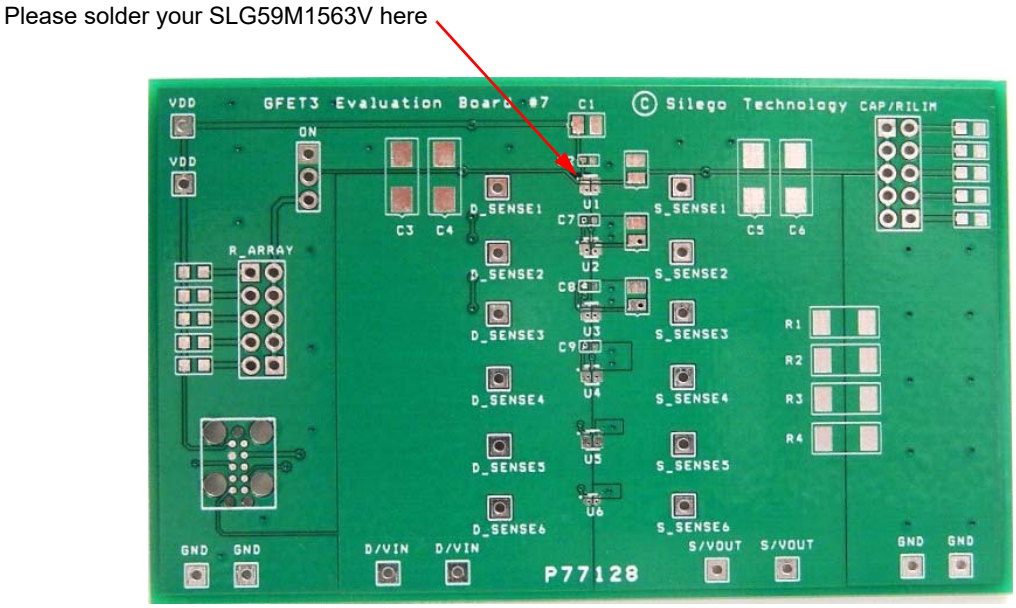



**Figure 1. SLG59M1563V Evaluation Board.**

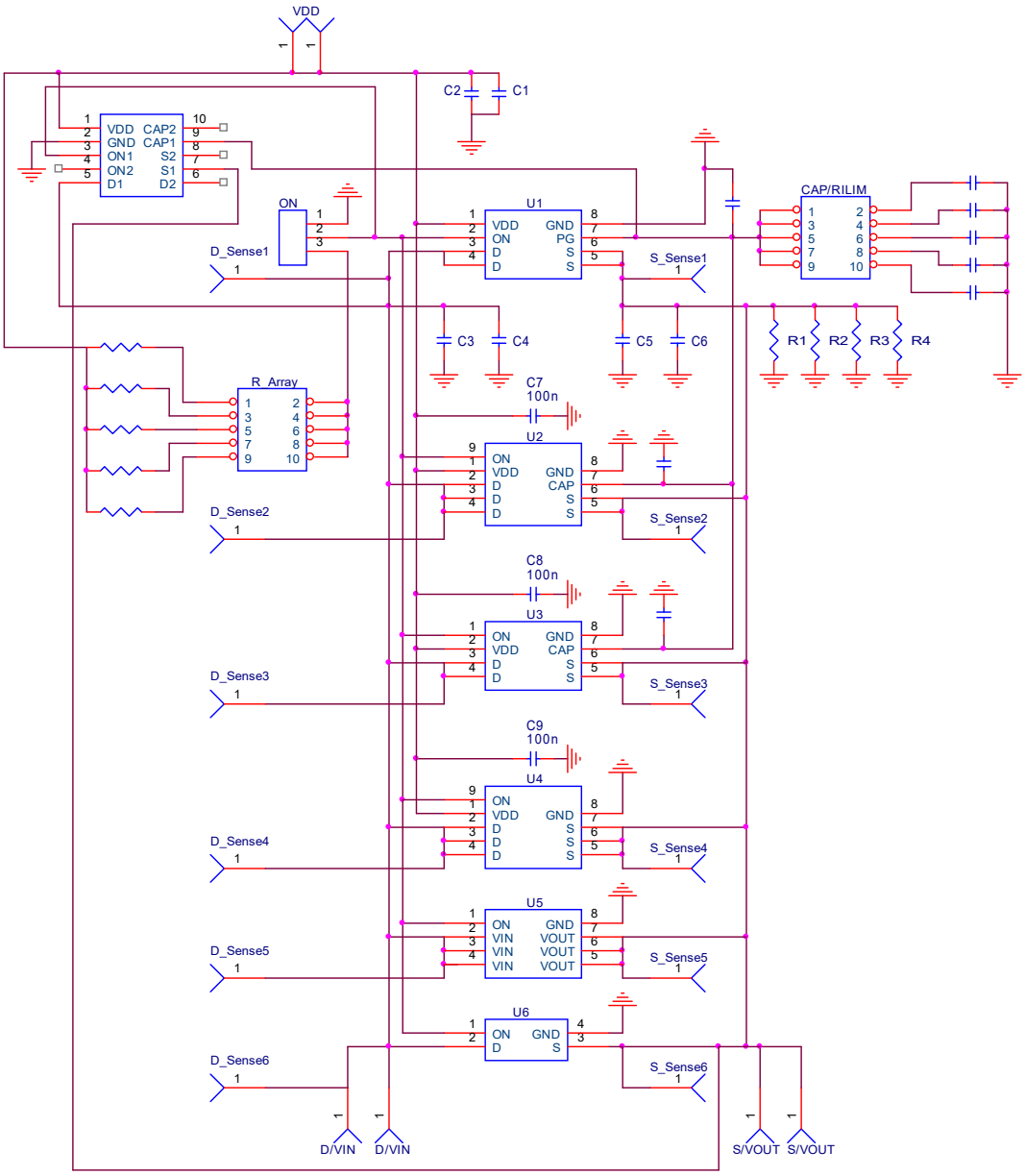



**Figure 2. SLG59M1563V Evaluation Board Connection Circuit.**

## Basic Test Setup and Connections

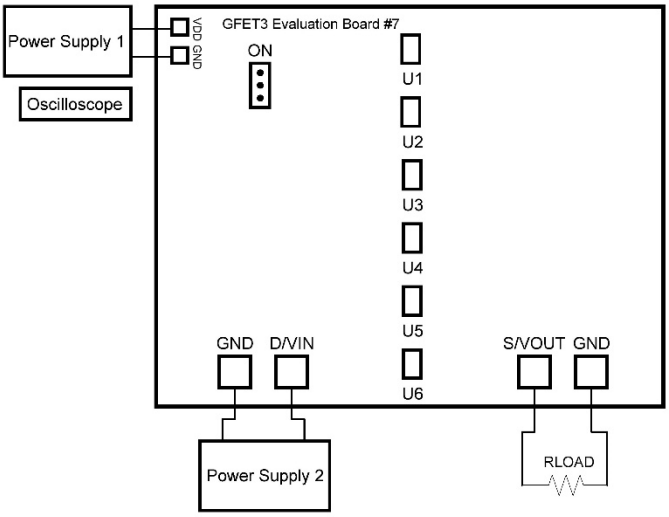



**Figure 3. Typical connections for GFET3 Evaluation.**

**EVB Configuration**

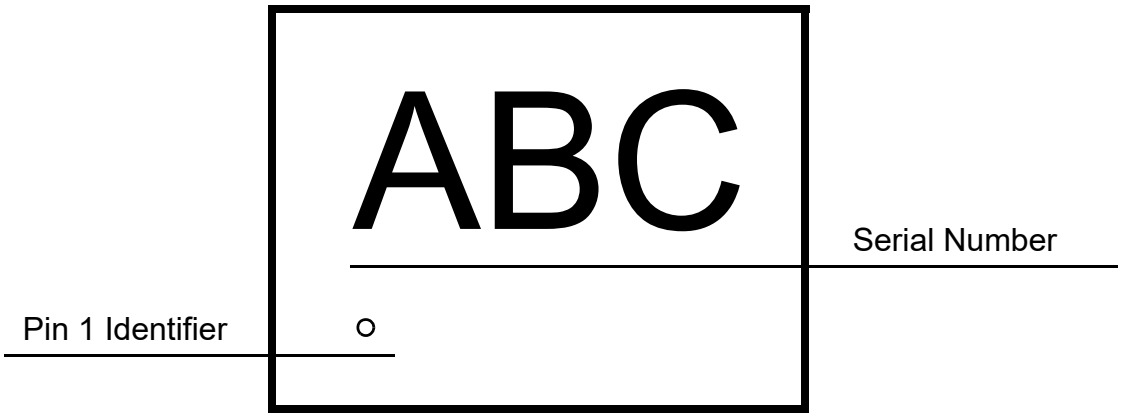
1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;

2.Turn on Power Supply 1 and set desired $V_{DD}$ from 1.5 V…5.5 V range;

3.Turn on Power Supply 2 and set desired $V_D$ from 1 V…$V_{DD}$ range;

4.Toggle the ON signal High or Low to observe SLG59M1563V operation.

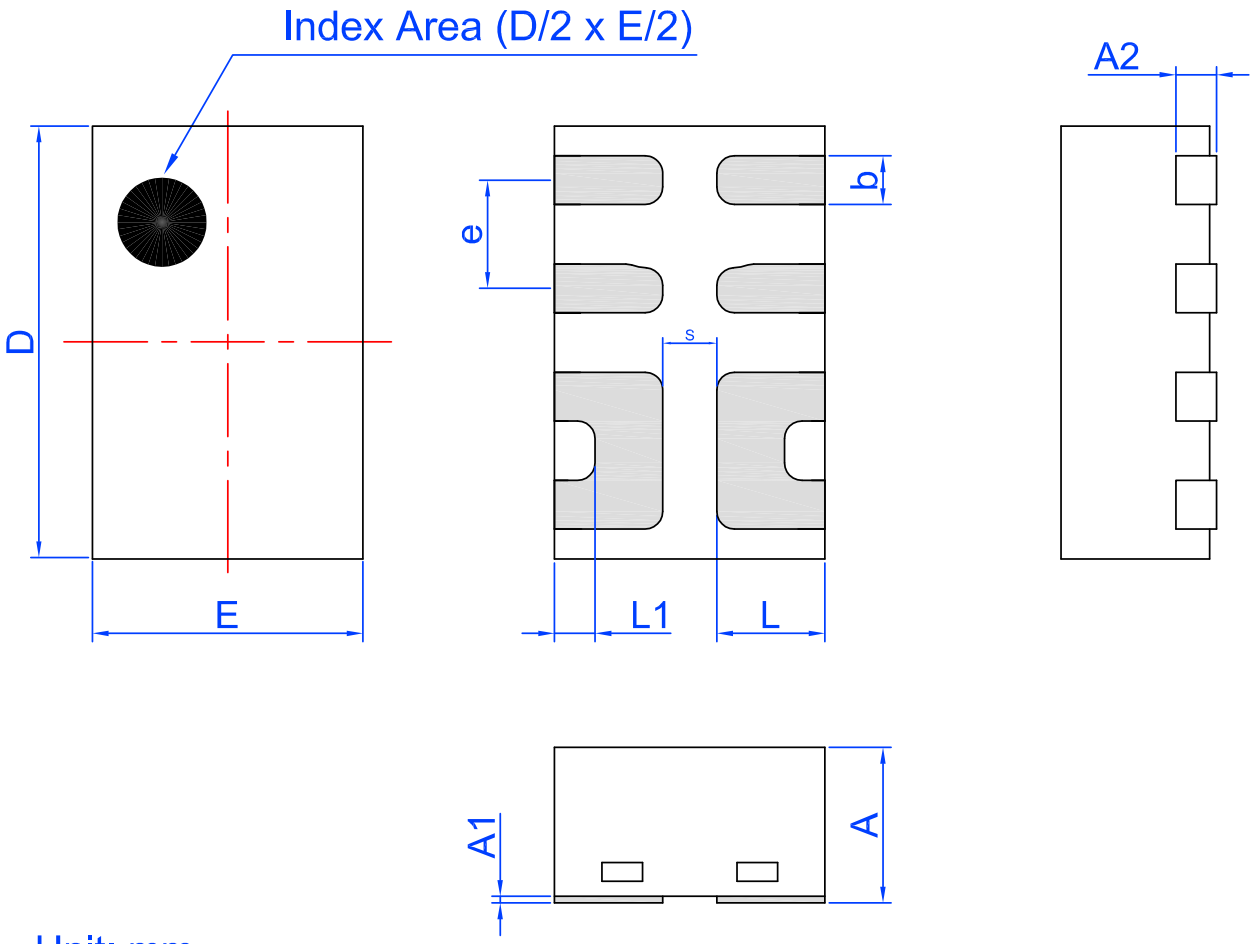
## Package Top Marking System Definition




Each character in Serial Number field can be alphanumeric A-Z

## Package Drawing and Dimensions

**8 Lead STDFN Package 1.0 x 1.6 mm (Fused Lead)**
**IC Net Weight: 0.0025 g**




Unit: mm

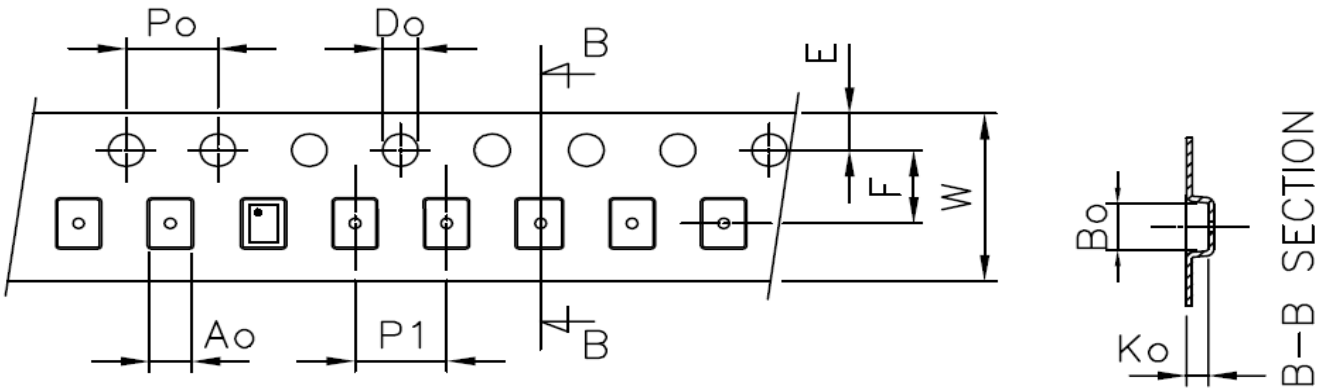
| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|---|---|---|---|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 | D | 1.55 | 1.60 | 1.65 |
| A1 | 0.005 | - | 0.060 | E | 0.95 | 1.00 | 1.05 |
| A2 | 0.10 | 0.15 | 0.20 | L | 0.35 | 0.40 | 0.45 |
| b | 0.13 | 0.18 | 0.23 | L1 | 0.10 | 0.15 | 0.20 |
| e | 0.40 BSC | | | S | 0.2 REF | | |

## Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STDFN 8L 1x1.6mm 0.4P FC Green | 8 | 1.0 x 1.6 x 0.55 | 3,000 | 3,000 | 178 / 60 | 100 | 400 | 100 | 400 | 8 | 4 |

## Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STDFN 8L 1x1.6mm 0.4P FC Green | 1.12 | 1.72 | 0.7 | 4 | 4 | 1.55 | 1.75 | 3.5 | 8 |




## Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 $mm^3$ (nominal). More information can be found at www.jedec.org.

## Revision History

| Date | Version | Change |
|---|---|---|
| 1/11/2019 | 1.03 | Updated Style and formatting<br>Added Chart<br>Added Layout Guidelines<br>Fixed typos |
| 9/13/2016 | 1.02 | Added Power Up/Down Sequencing Considerations<br>Updated text and parameter names for clarity |
| 3/9/2016 | 1.01 | Updated IDSlkg conditions |