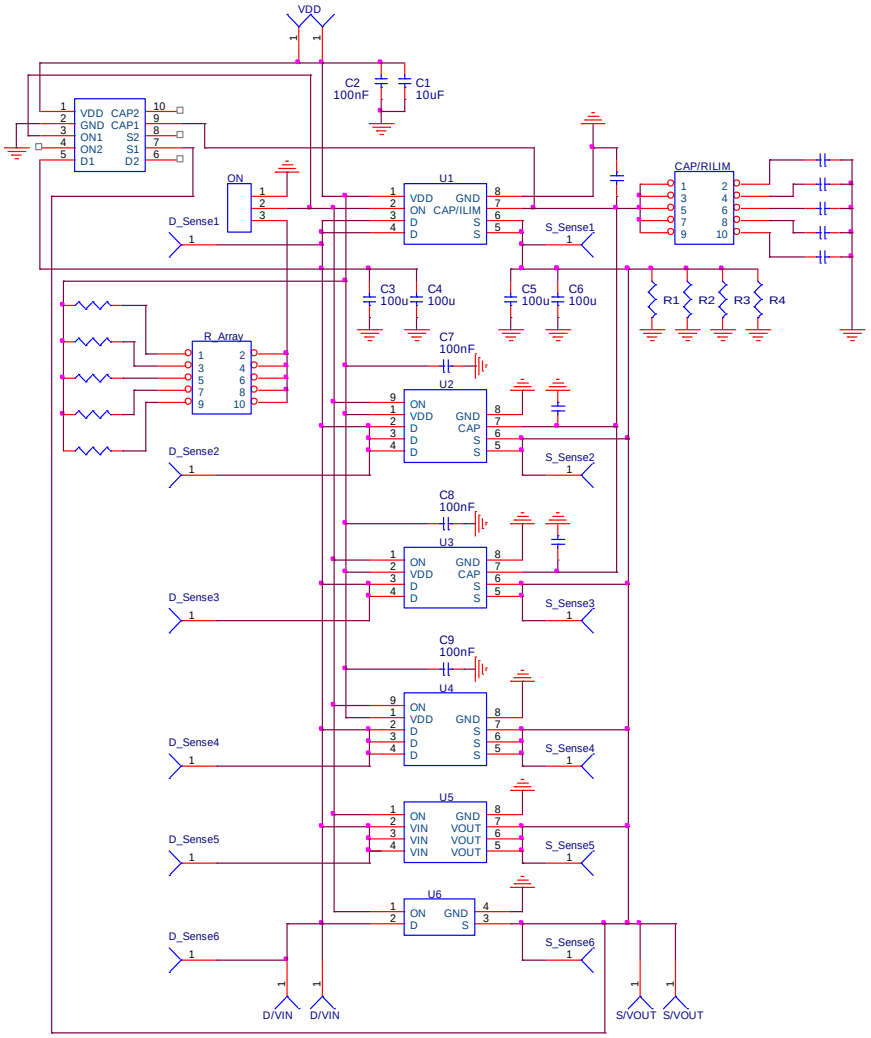

Figure 4. SLG59M1657V Connection Circuit

SILEGO

GreenFET3
SLG59M1657V
Layout Guide

Content

Description

The SLG59M1657V is a 8.4 mΩ, ~ 4 A single-channel load switch that is able to switch 0.9 V to 5.5 V power rails. The product is packaged in an ultra-small 1.5 x 2 mm package.

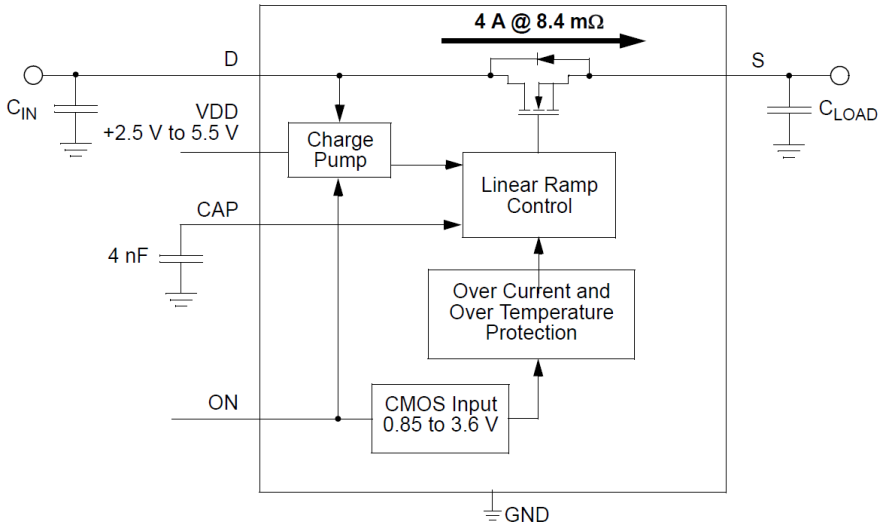

Figure 1: SLG59M1657V Block Diagram

This layout guide provides some important information about the PCB layout of SLG59M1657V applications.

SILEGO FC-TDFN 1.5x2.0-8L PKG

Unit: um

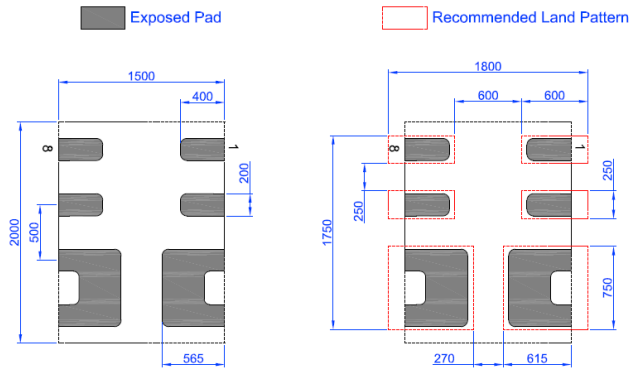

Figure 2. SLG59M1657V Package Dimensions and Recommended Land Pattern

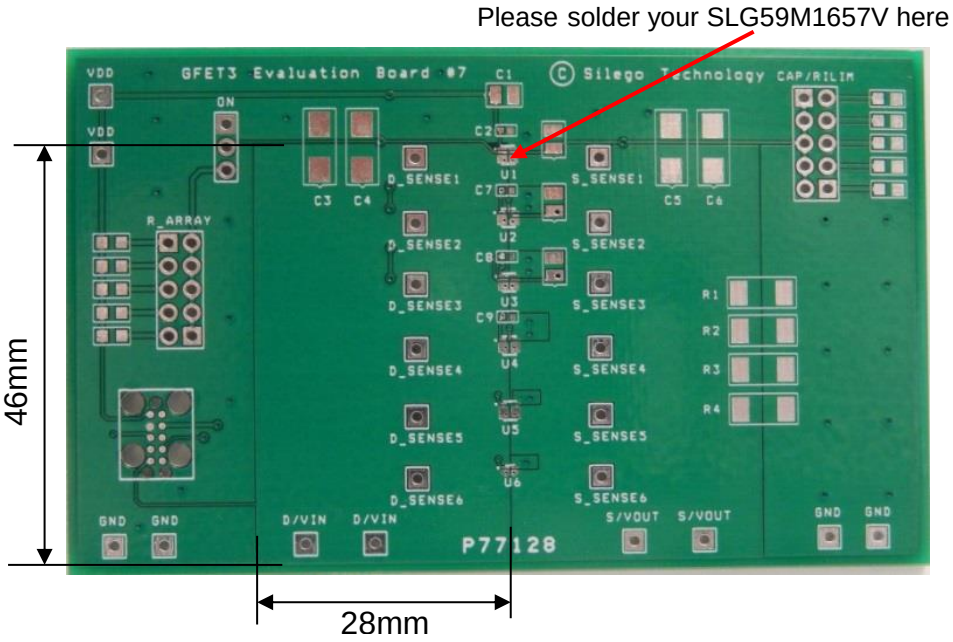

Figure 3. SLG59M1657V Evaluation Test Board

Note: Evaluation board has D_Sense and S_Sense pads. Please use them only for RDS(ON) evaluation.

2. Power and Ground Planes

2.1. The VDD pin needs are 0.1uF and 10uF external capacitors to smooth pulses from the power supply. Locate these capacitors close to PIN1.

2.2. The trace length from the control IC to the ON pin should be as short as possible and must avoid crossing this trace with power rails.

2.3. The D/VIN and S/VOUT pins carry significant current. Please note how the D/VIN and S/VOUT pads are placed directly on the power planes in Figure 3, which minimizes the Rds(ON) associated with long, narrow traces. The D/VIN, S/VOUT and GND pins dissipate most of the heat generated during high-load current condition. The layout shown in Figure 3 is illustrating a proper solution for heat to transfer as efficiently as possible out of the device.

2.4. Place the power rail ramp capacitor as close as possible to the CAP pin to avoid/reduce the effect of parasitic mount capacitance.

2.5. The GND pin (PIN8) should be connected to GND.

2.6. 2 oz. copper is recommended for higher currents.