An Ultra-small, 4 mΩ, 2 A Integrated Power Switch with Multiple Protection Features

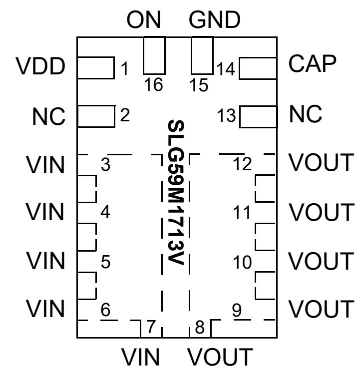
General Description

Operating from a 2.5 V to 5.5 V power supply and fully specified over the -40 °C to 85 °C temperature range, the SLG59M1713V is a high-performance 4 mΩ, 2 A single-channel nFET integrated power switch with adjustable inrush current control which is achieved by adjusting the V_{OUT} slew rate with an external capacitor. Using a proprietary MOSFET design, the SLG59M1713V achieves a stable 4 mΩ RDS_{ON} across a wide input/supply voltage range. Incorporating two-stage current protection as well as thermal protection, the SLG59M1713V is designed for all 0.8 V to 5.5V power rail applications. Using Dialog's proprietary CuFET™ technology for high-current operation, the SLG59M1713V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.6 mm x 2.5 mm STQFN package

Features

- Low Typical RDS_{ON} nFET: 4 mΩ
- Maximum Continuous Switch Current: Up to 2 A
- Supply Voltage: 2.5 V ≤ V_{DD} ≤ 5.5 V
- Wide Input Voltage Range: 0.8 V ≤ V_{IN} ≤ V_{DD}
- Capacitor-adjustable Start-up and Inrush Current Control
- Two-stage Overcurrent Protection:
  - Fixed threshold, 4 A Active Current Limit
  - Fixed 0.5 A Short-circuit Current Limit
- Internal V_{OUT} Discharge
- Operating Temperature: -40 °C to 85 °C
- Low θ_{JA}, 16-pin 1.6 mm x 2.5 mm STQFN Packaging
  - Pb-Free / Halogen-Free / RoHS compliant

Pin Configuration

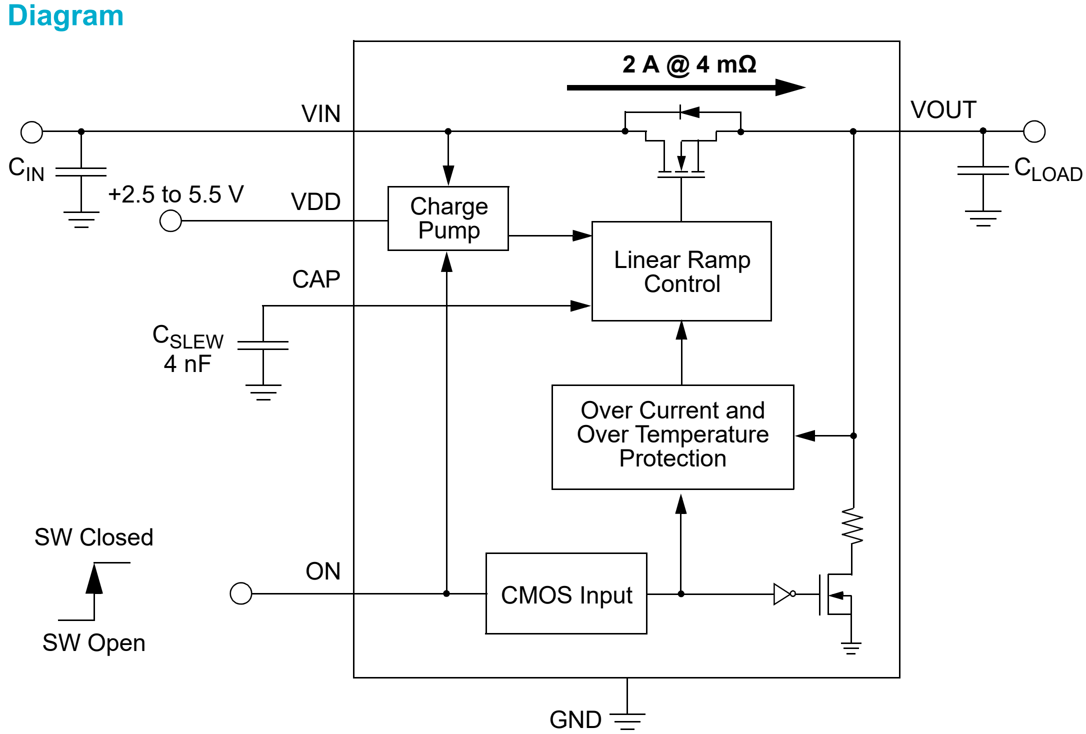


16-pin FC-STQFN
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	With an internal 1.9 V $V_{DD(UVLO)}$ threshold, VDD supplies the power for the operation of the power switch and internal control circuitry where its range is 2.5 V ≤ V_{DD} ≤ 5.5 V. Bypass the VDD pin to GND with a 0.1 μF (or larger) capacitor
2	NC	NC	No Connect
3-7	VIN	MOSFET	Drain terminal of Power MOSFET (Pins 3-7 fused together). Connect a 10 μF (or larger) low ESR capacitor from this pin to GND. Capacitors used at VIN should be rated at 10 V or higher.
8-12	VOUT	MOSFET	Source terminal of Power MOSFET (Pins 8-12 fused together). Connect a low ESR capacitor (up to 500 μF) from this pin to GND. Capacitors used at VOUT should be rated at 10 V or higher.
13	NC	NC	No Connect
14	CAP	Input	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V_{OUT} slew rate and overall turn-on time of the SLG59M1713V. For best performance, the range for C_{SLEW} values are 2 nF ≤ C_{SLEW} ≤ 22 nF. Capacitors used at the CAP pin should be rated at 10 V or higher.
15	GND	GND	Ground
16	ON	Input	A low-to-high transition on this pin closes the power switch. ON is an asserted-HIGH, level-sensitive CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH} > 0.85 V. While there is an internal pull down circuit to ground (~4 MΩ), connect this pin to the output of a general-purpose output (GPO) from a microcontroller or other application processor.

Ordering Information

Part Number	Type	Production Flow
SLG59M1713V	STQFN 16L	Industrial, -40 °C to 85 °C
SLG59M1713VTR	STQFN 16L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Pin Voltage to GND		--	--	6	V
V_{IN} to GND	Power Switch Input Voltage to GND		-0.3	--	6	V
V_{OUT} to GND	Power Switch Output Voltage to GND		-0.3	--	V_{IN}	V
ON, CAP to GND	ON and CAP Pin Voltages to GND		-0.3	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	500	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	1.6 x 2.5 mm 16L STQFN; Determined using 1 in^2, 1.2 oz. copper pads under each VIN and VOUT on FR4 pcb material	--	35	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	1.2	W
MOSFET IDS_{CONT}	Continuous Current from VIN to VOUT		--	--	2	A
MOSFET IDS_{PK}	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	3	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated). Typical values are at T_A = 25 °C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage		2.5	--	5.5	V
$V_{DD(UVLO)}$	V_{DD} Undervoltage Lockout Threshold	V_{DD} ↑	1.6	1.9	2.2	V
		V_{DD} ↓	1.5	1.8	2.2	V
I_{DD}	Power Supply Current, when OFF	$V_{DD} = V_{IN}$ = 5.5 V; ON = 0 V	--	1	2	µA
	Power Supply Current, when ON	$V_{DD} = V_{IN}$ = ON = 5.5 V; No Load	--	120	170	µA
RDS_{ON}	ON Resistance	$V_{DD} = V_{IN}$ = 5 V; T_A = 25 °C; I_{DS} = 100 mA	--	4	5.5	mΩ
		$V_{DD} = V_{IN}$ = 5 V; T_A = 85 °C; I_{DS} = 100 mA	--	5	6.8	mΩ
MOSFET IDS	Current from VIN to VOUT	Continuous	--	--	2	A
I_{FET_OFF}	MOSFET OFF Leakage Current	$V_{DD} = V_{IN}$ = 5.5 V; V_{OUT} = 0 V; ON = 0 V	--	--	2	µA
V_{IN}	Drain Voltage		0.8	--	V_{DD}	V
I_{LIMIT}	Active Current Limit, I_{ACL}	V_{OUT} > 0.3 V	3	4	5	A
	Short-circuit Current Limit, I_{SCL}	V_{OUT} < 0.3 V	--	0.5	--	A

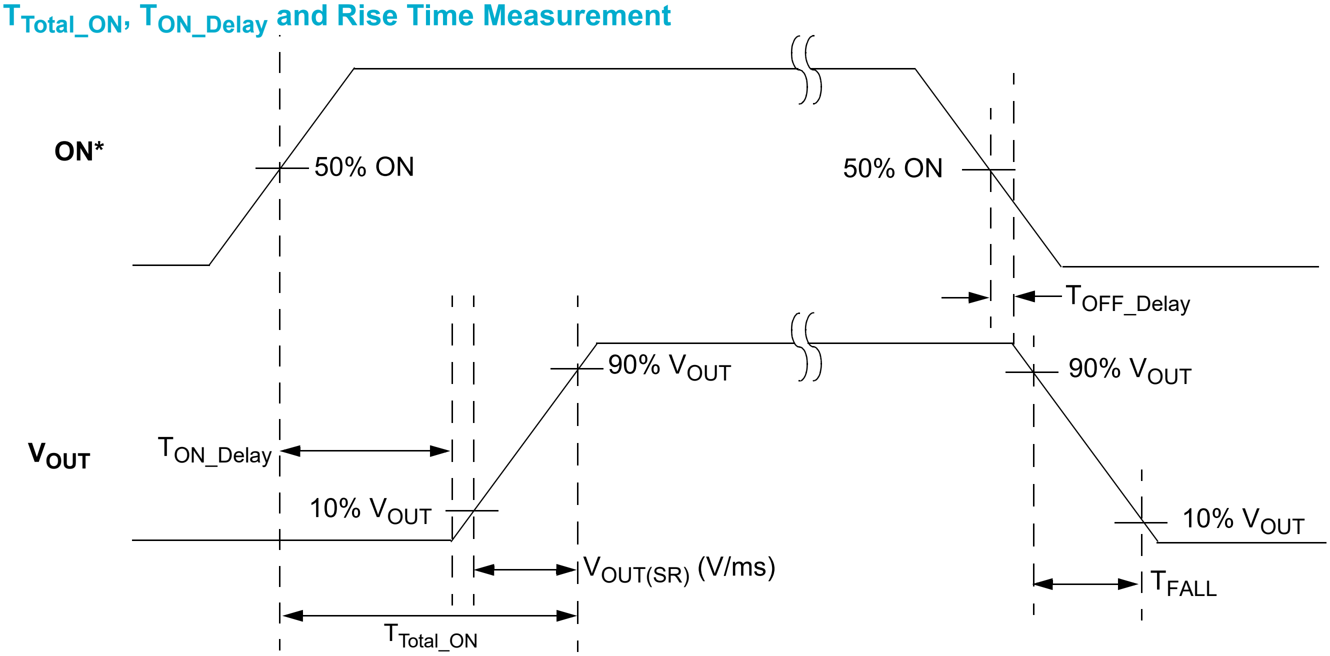
Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated). Typical values are at T_A = 25 °C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{ON_Delay}	ON Delay Time	50% ON to V_{OUT} Ramp Start; V_{DD} = V_{IN} = 5 V; C_{SLEW} = 4 nF; R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	--	200	--	µs
$V_{OUT(SR)}$	V_{OUT} Slew Rate	10% V_{OUT} to 90% V_{OUT} ↑	Set by External C_{SLEW}[1]			V/ms
		Example: C_{SLEW} = 4 nF; V_{DD} = V_{IN} = 5 V; R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	2.5	2.9	3.5	V/ms
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_{OUT} ↑	Set by External C_{SLEW}[1]			ms
		Example: C_{SLEW} = 4 nF; V_{DD} = V_{IN} = 5 V; R_{LOAD} = 20 Ω, C_{LOAD} = 10 µF	1.4	1.7	2	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_{OUT} Fall Start; V_{DD} = V_{IN} = 5 V; R_{LOAD} = 20 Ω, no C_{LOAD}	--	8	15	µs
C_{LOAD}	Output Load Capacitance	C_{LOAD} connected from VOUT to GND	--	--	500	µF
$R_{DISCHRG}$	Output Discharge Resistance	V_{IN} = V_{DD} = 5 V; ON = 0 V; V_{OUT} = 0.4 V	170	200	250	Ω
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
$I_{ON(LKG)}$	ON Pin Leakage Current	ON = ON_V_{IH} or ON = GND	--	1.5	--	µA
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	125	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	100	--	°C

Notes:
1. Refer to typical Timing Parameter vs. C_{SLEW} performance charts for additional information when available.

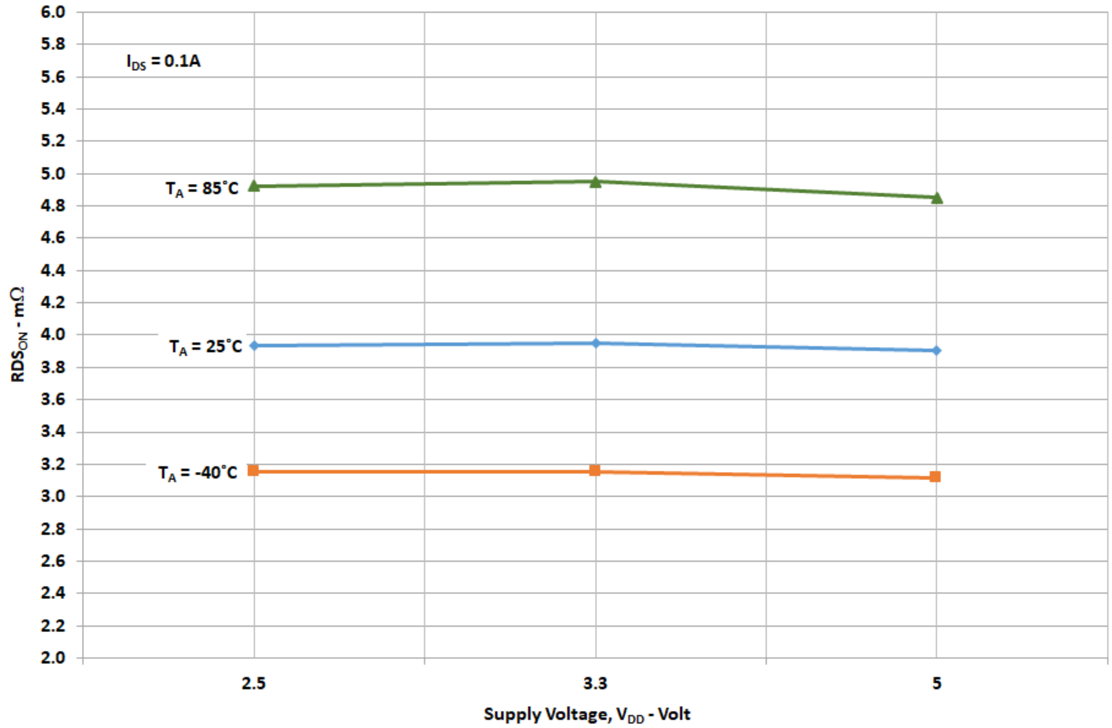
T_{Total_ON}, T_{ON_Delay} and Rise Time Measurement



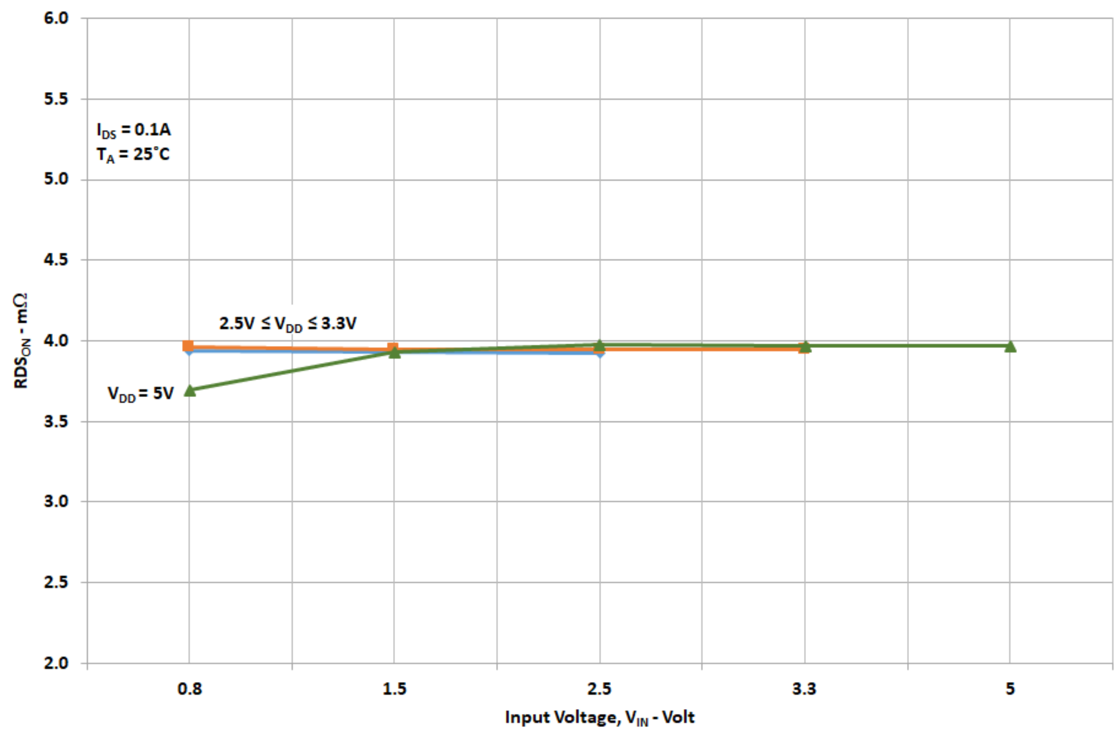
*Rise and Fall Times of the ON Signal are 100 ns

Typical Performance Characteristics

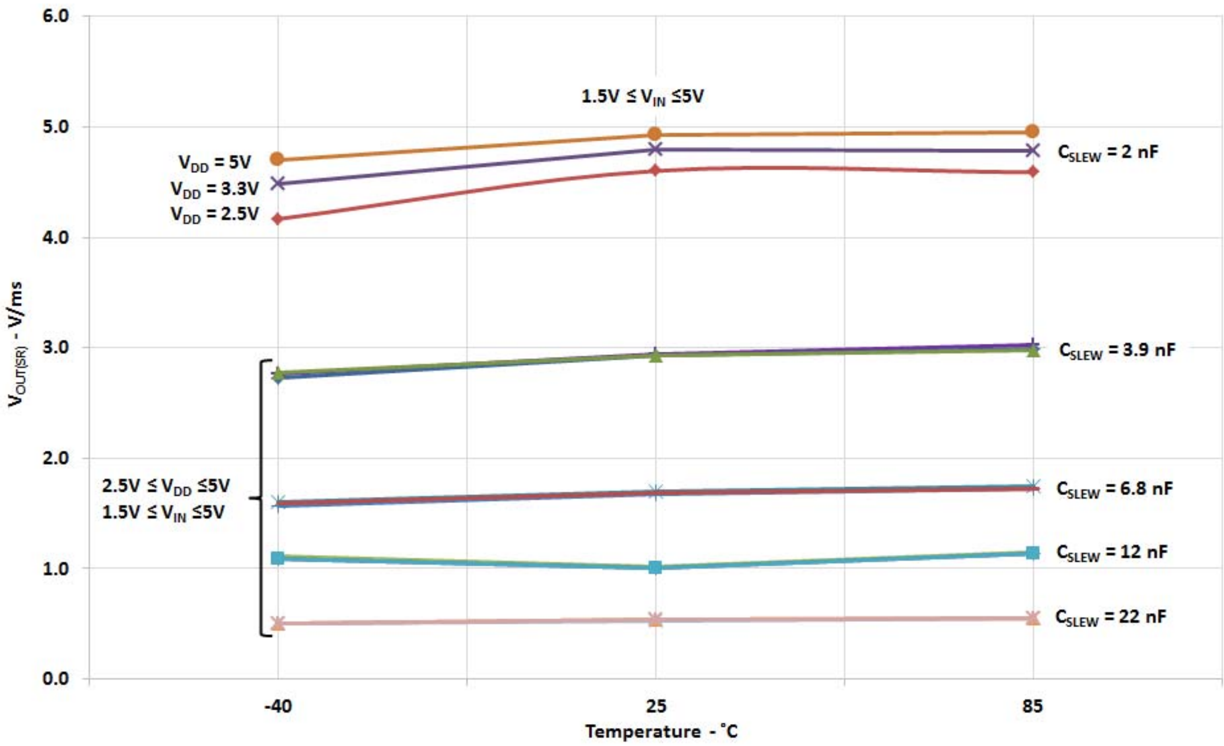
RDS_{ON} vs. V_{DD} and Temperature



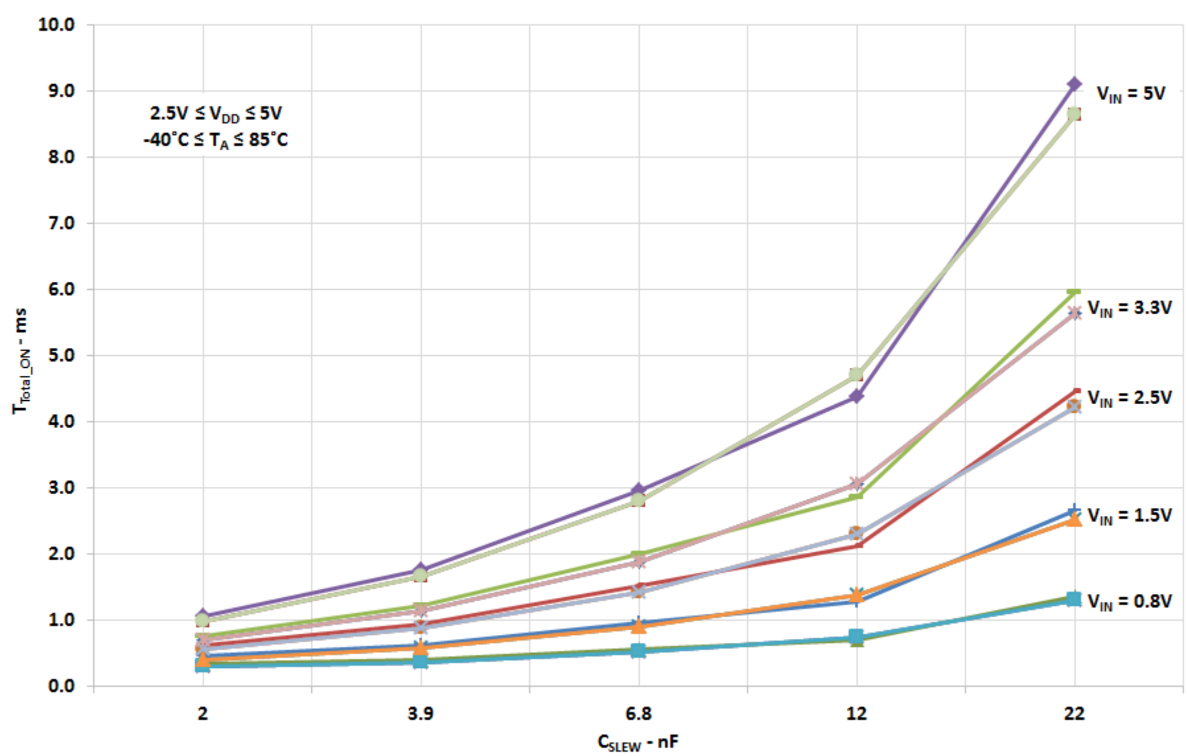
RDS_{ON} vs. V_{IN} and V_{DD}



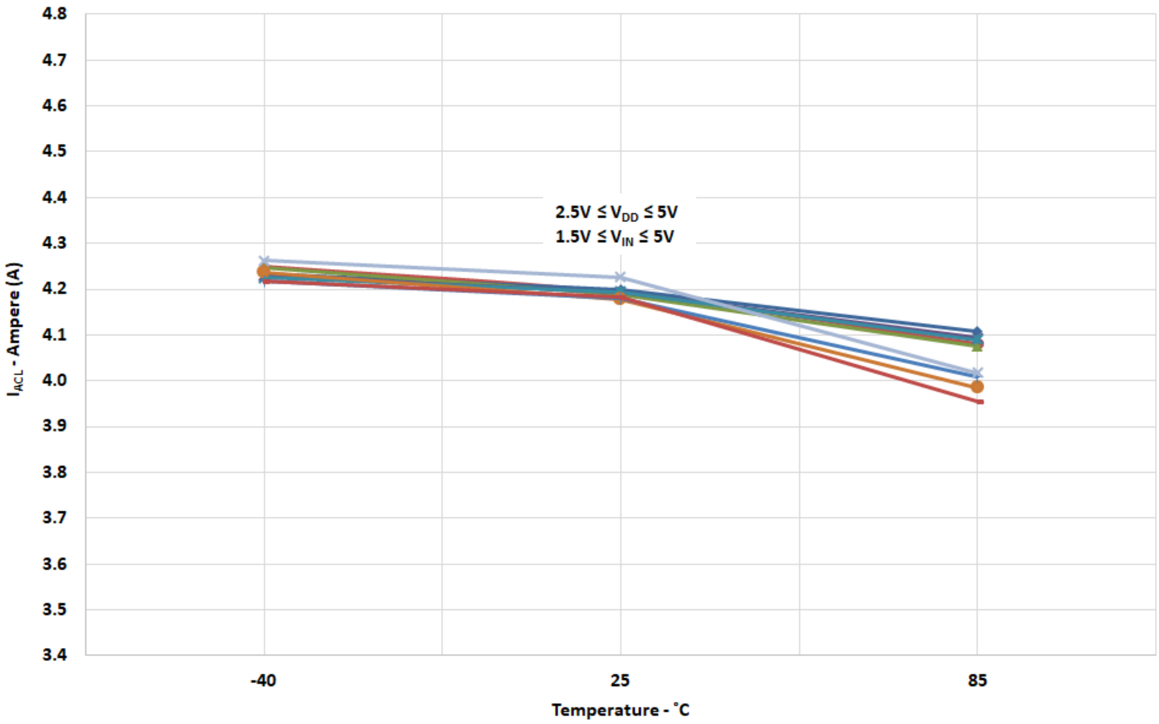
V_{OUT} Slew Rate vs. Temperature, V_{DD}, V_{IN}, and C_{SLEW}



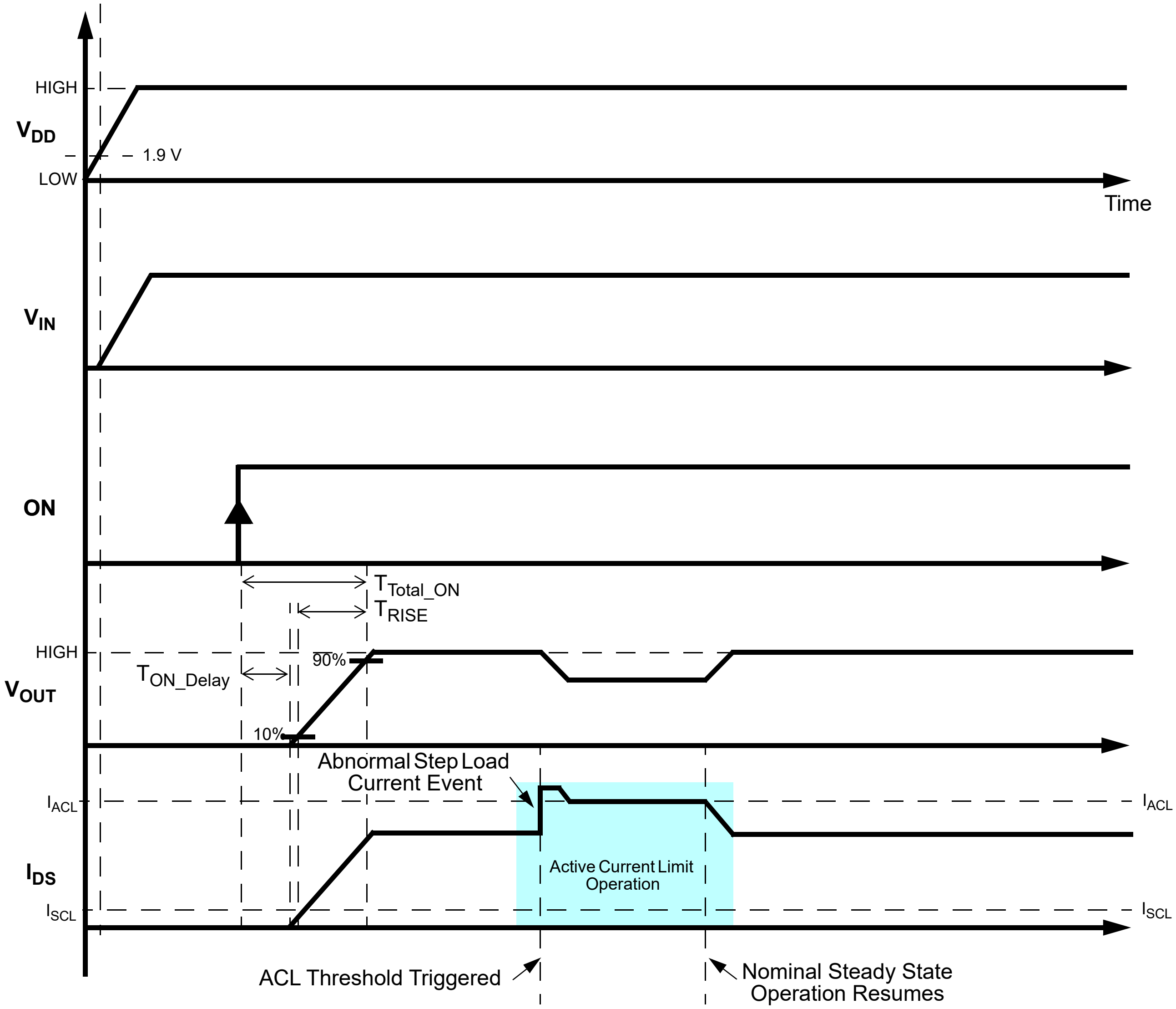
T_{Total_ON} vs. C_{SLEW}, V_{IN}, V_{DD}, and Temperature



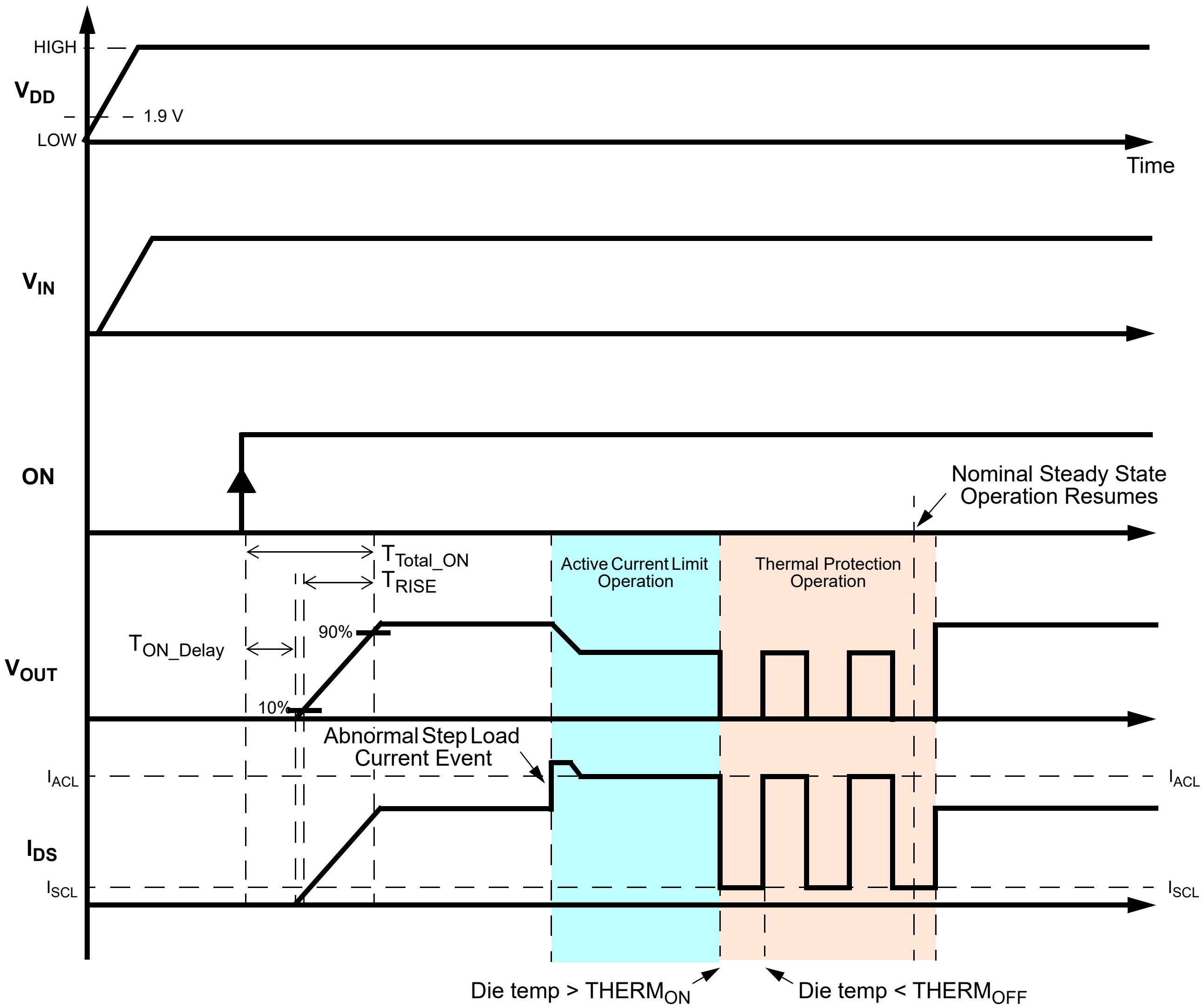
I_{ACL} vs. Temperature, V_{DD}, and V_{IN}



Timing Diagram - Basic Operation including Active Current Limit Protection



Timing Diagram - Active Current Limit & Thermal Protection Operation



SLG59M1713V Application Diagram

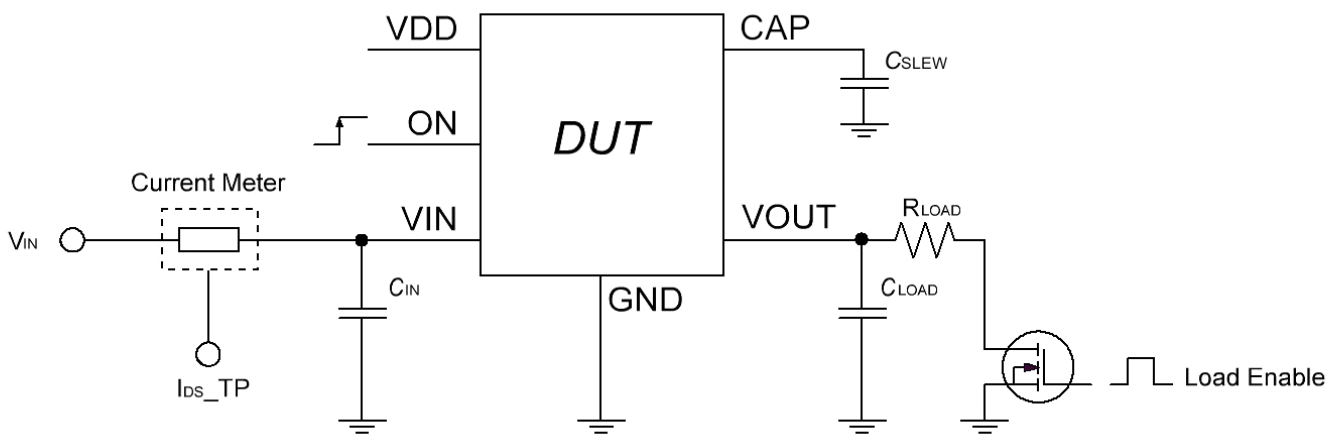


Figure 1. Test setup Application Diagram

Typical Turn-on Waveforms

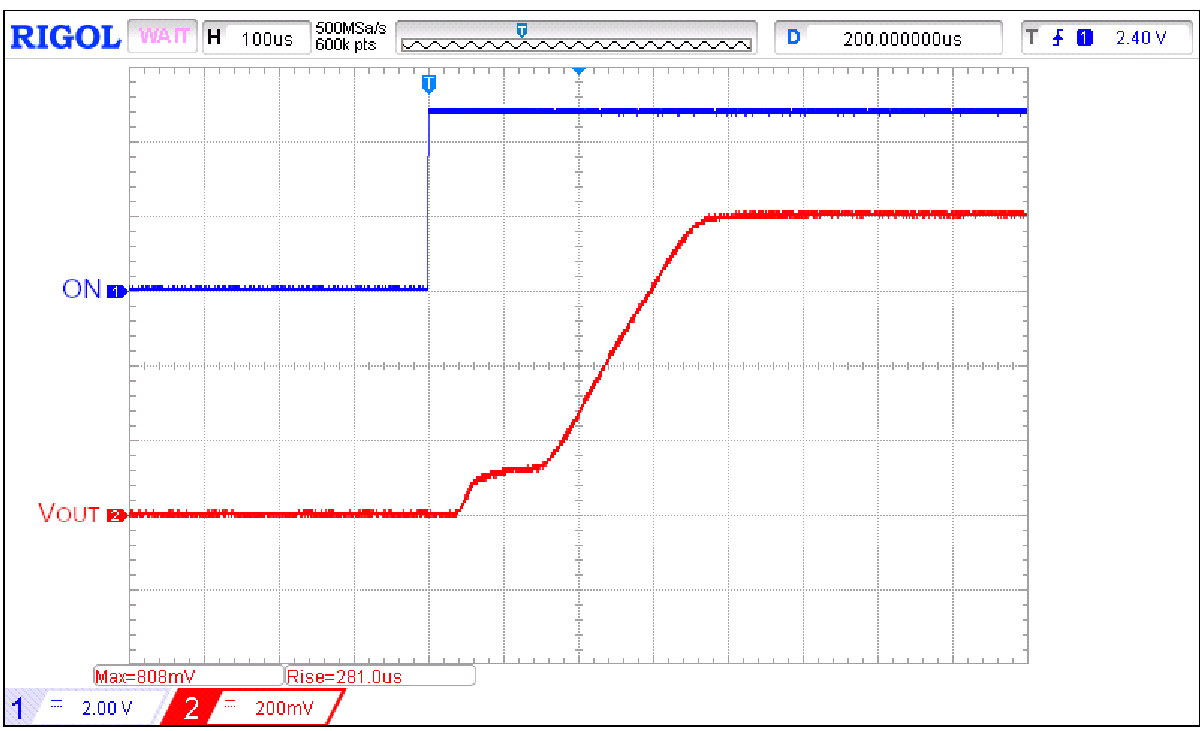


Figure 2. Typical Turn ON operation waveform for V_{DD} = 5 V, V_{IN} = 0.8 V, C_{SLEW} = 3.9 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

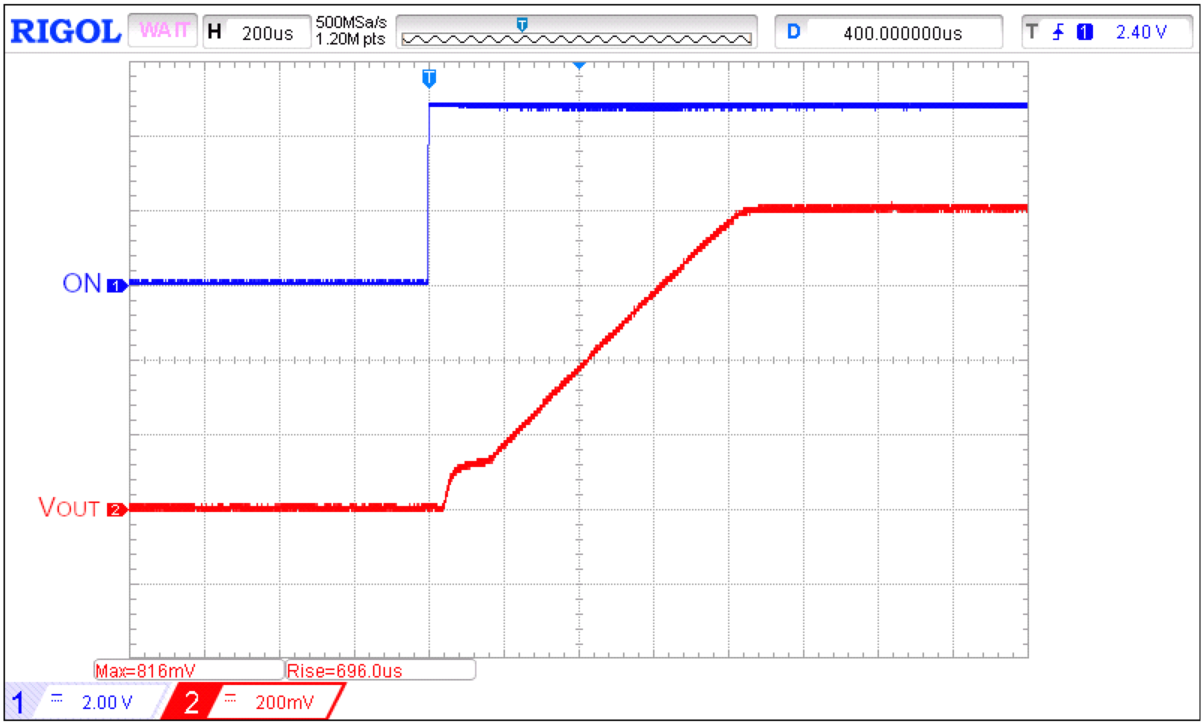


Figure 3. Typical Turn ON operation waveform for V_{DD} = 5 V, V_{IN} = 0.8 V, C_{SLEW} = 12 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

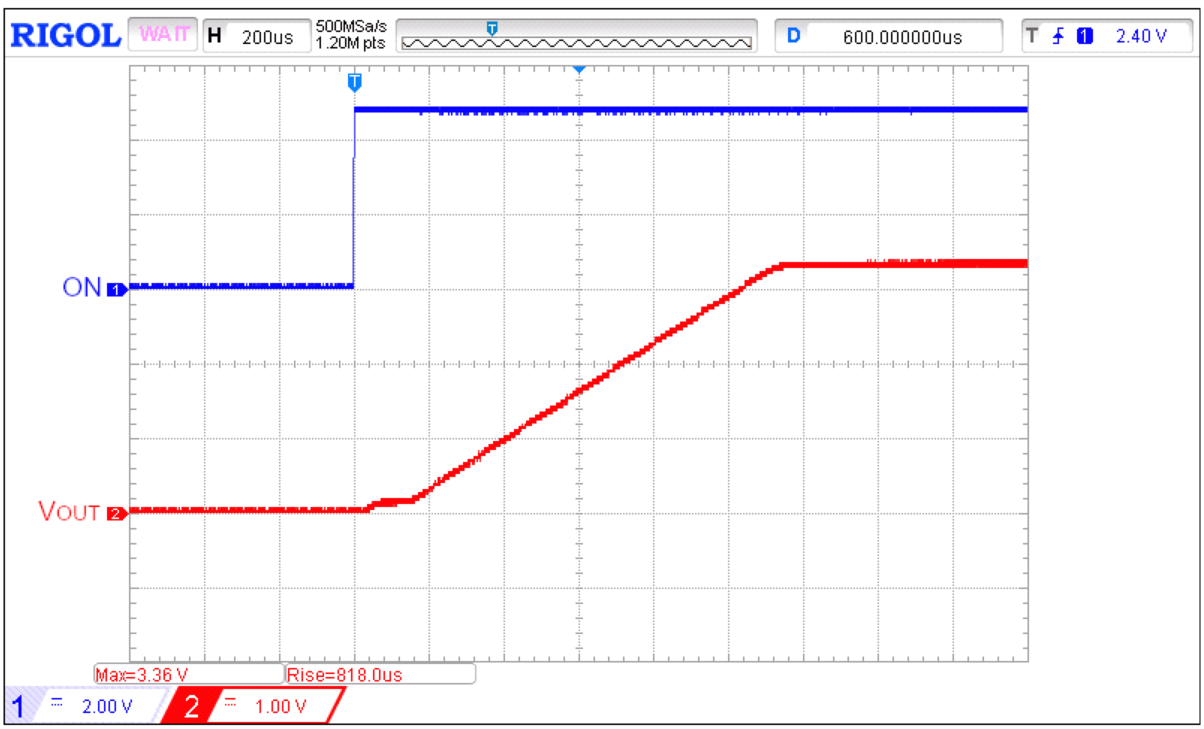


Figure 4. Typical Turn ON operation waveform for V_{DD} = 5 V, V_{IN} = 3.3 V, C_{SLEW} = 3.9 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

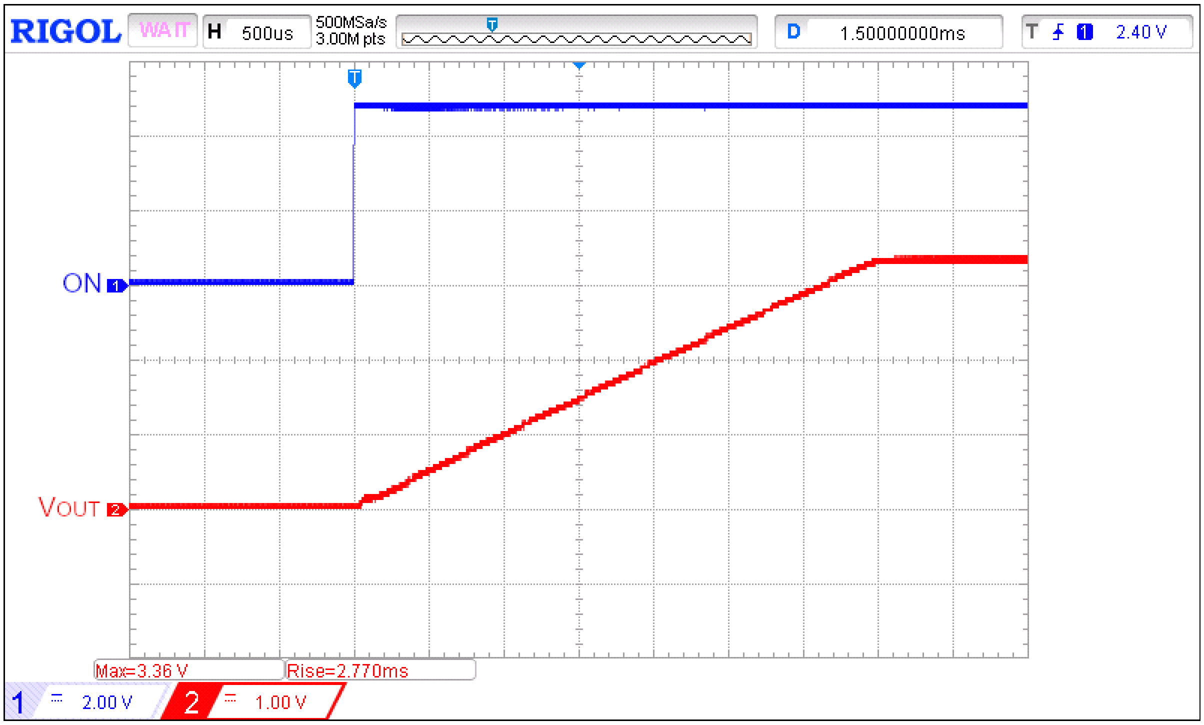


Figure 5. Typical Turn ON operation waveform for V_{DD} = 5 V V_{IN} = 3.3 V, C_{SLEW} = 12 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

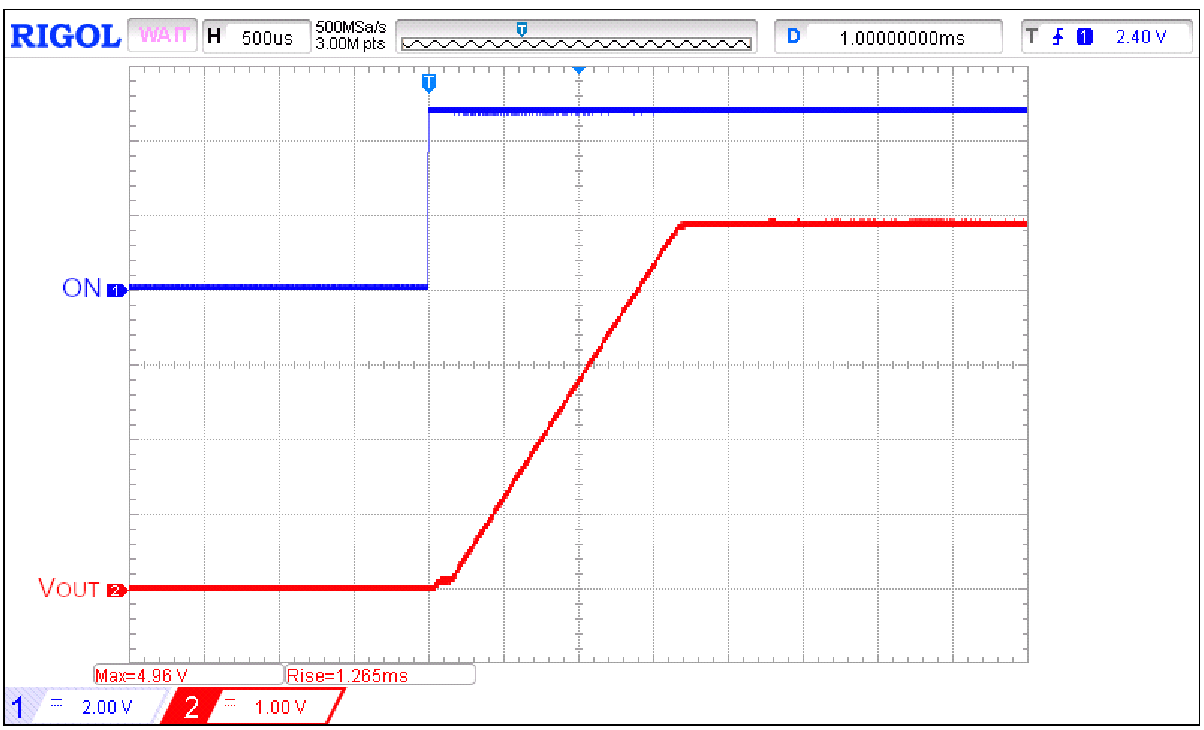


Figure 6. Typical Turn ON operation waveform for V_{DD} = 5 V, V_{IN} = 5 V, C_{SLEW} = 3.9 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

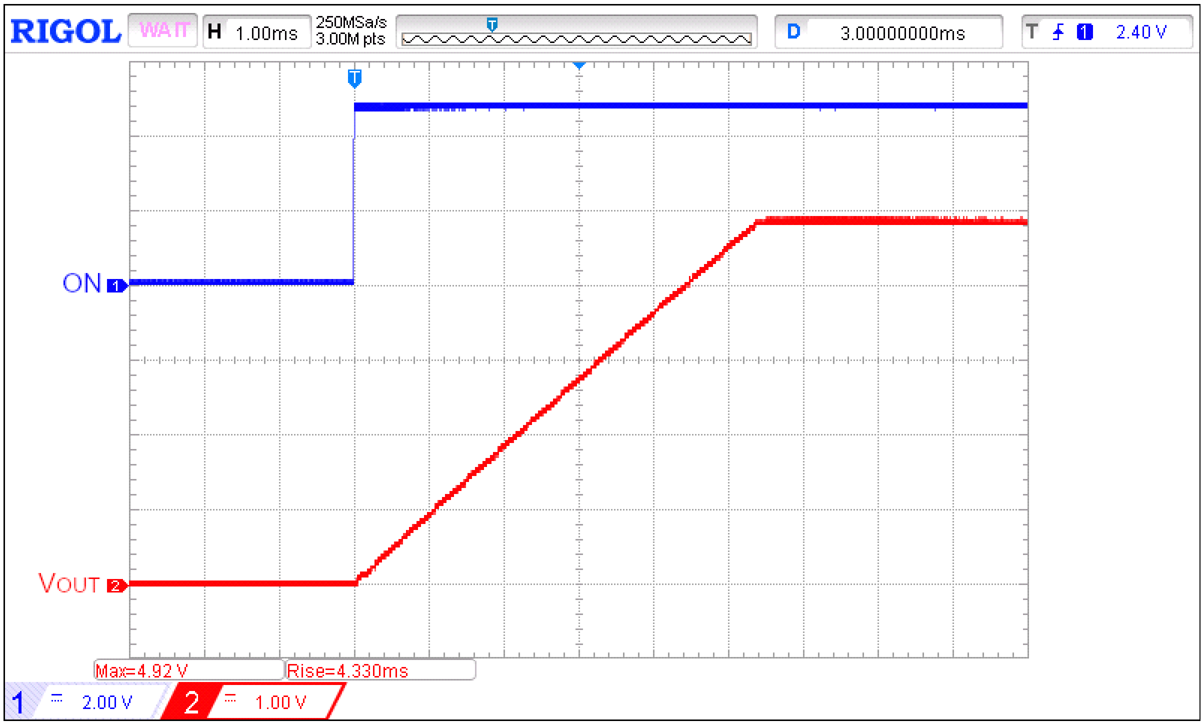


Figure 7. Typical Turn ON operation waveform for V_{DD} = 5 V, V_{IN} = 5 V, C_{SLEW} = 12 nF, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

Typical Turn-off Waveforms

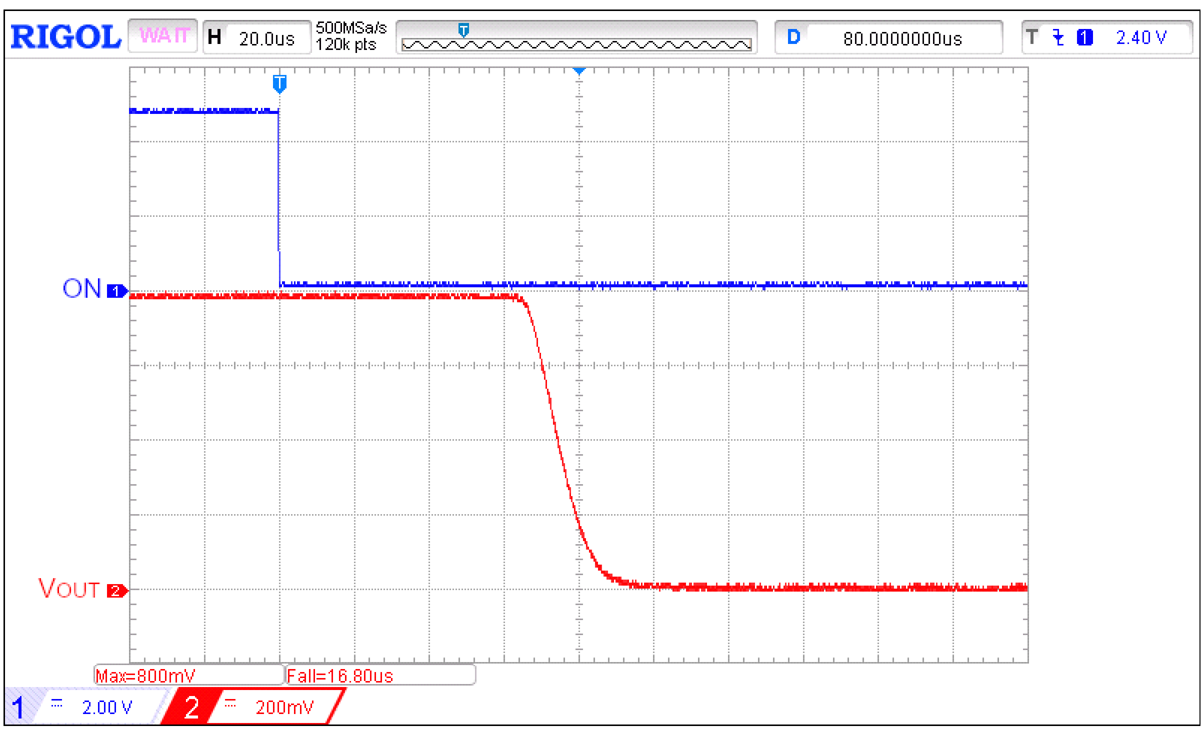


Figure 8. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 0.8 V, no C_{LOAD}, R_{LOAD} = 20 Ω

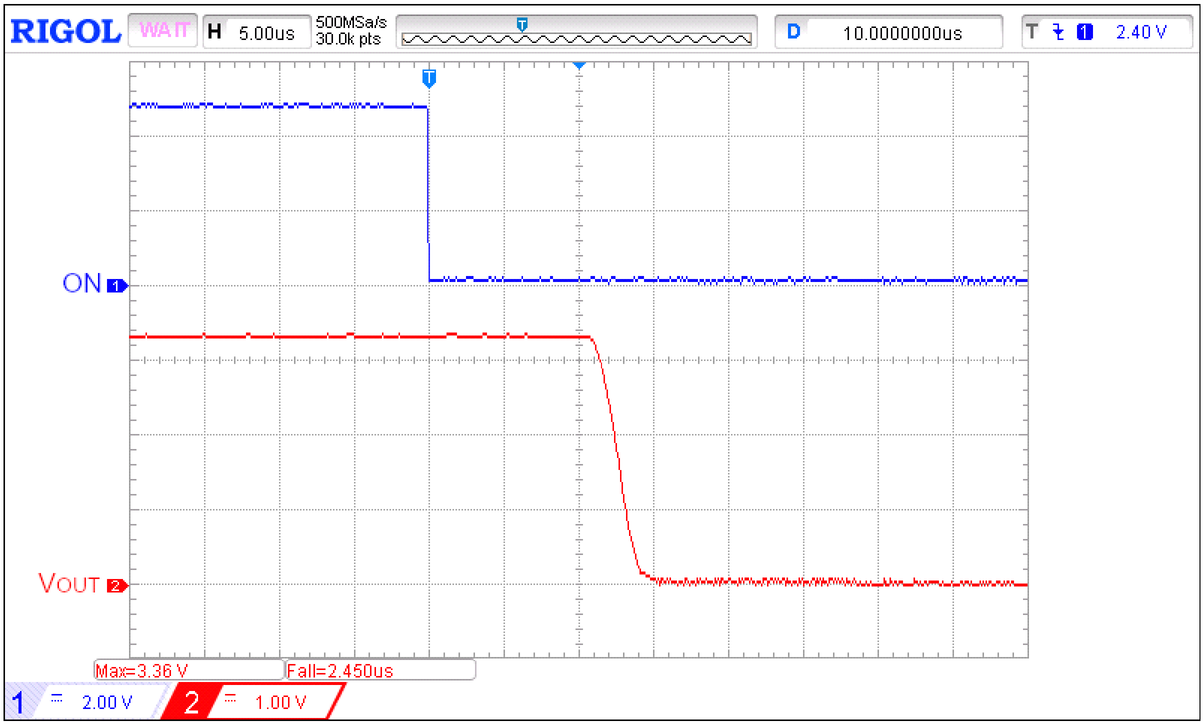


Figure 9. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 3.3 V, no C_{LOAD}, R_{LOAD} = 20 Ω

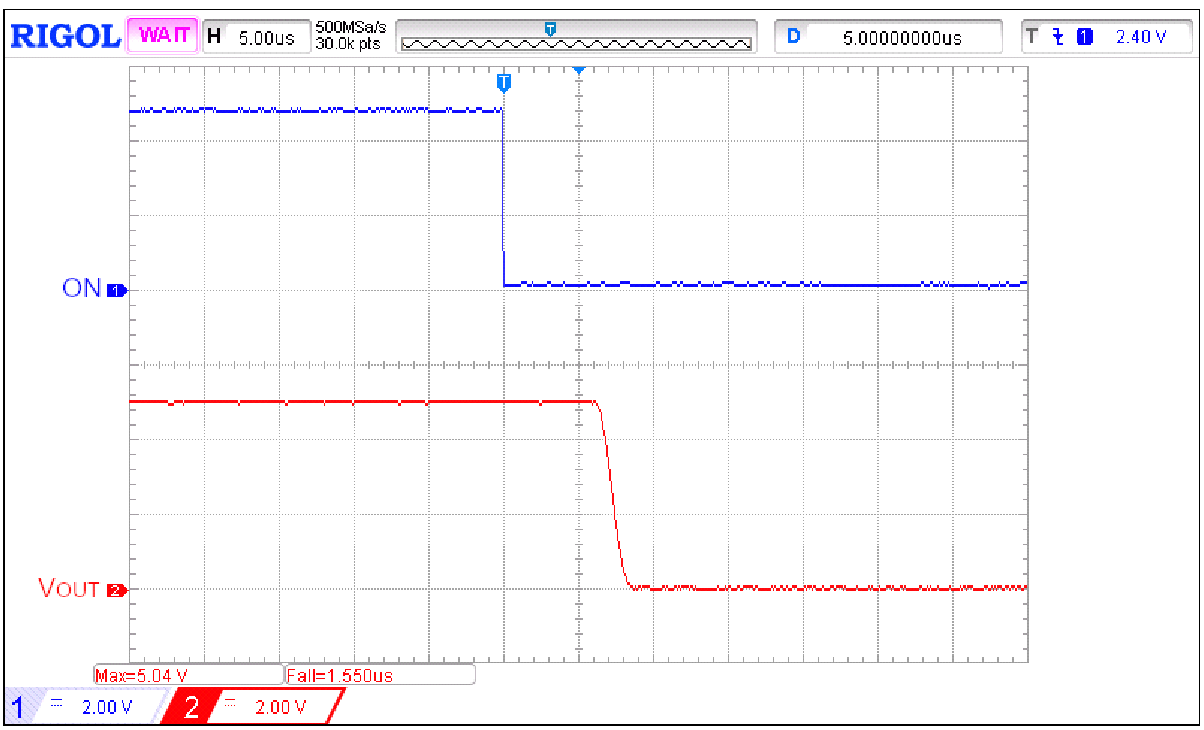


Figure 10. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 5 V, no C_{LOAD}, R_{LOAD} = 20 Ω

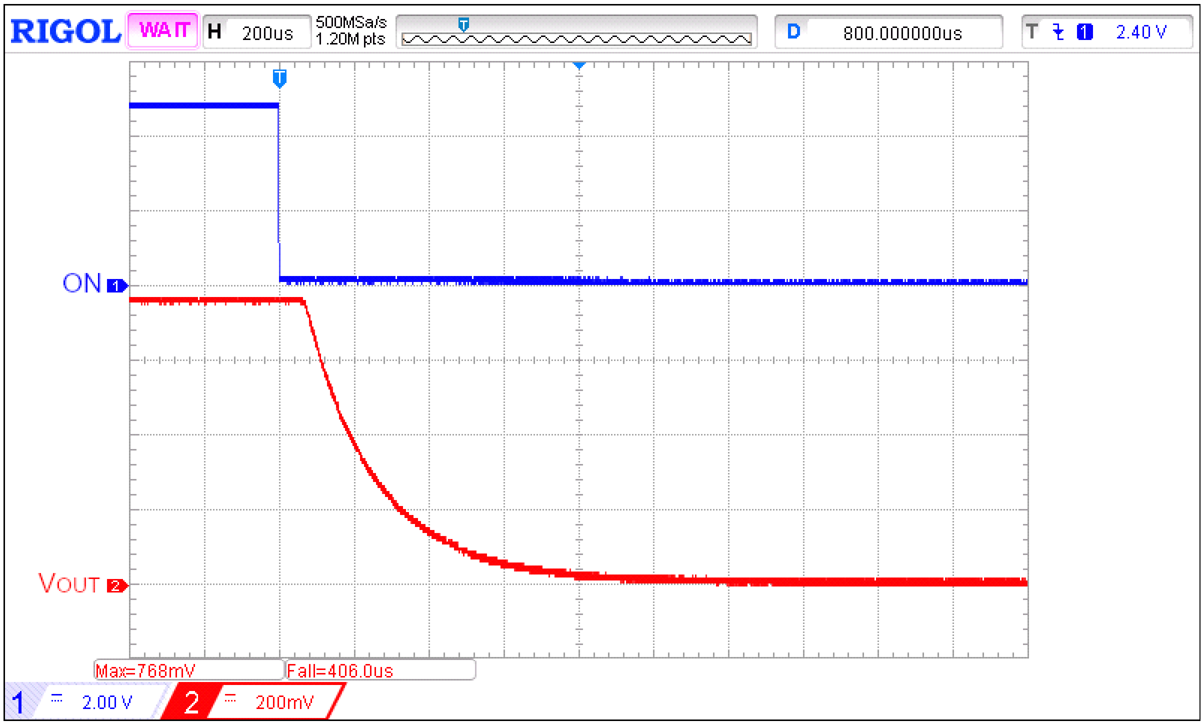


Figure 11. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 0.8 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

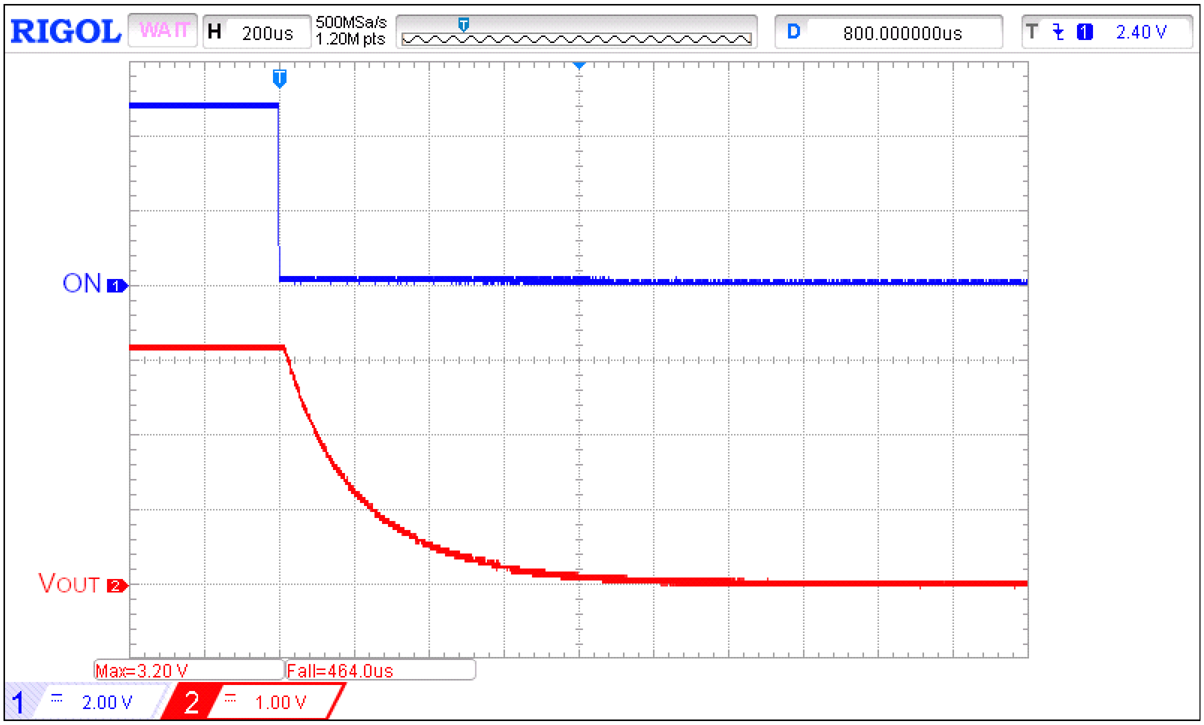


Figure 12. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 3.3 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

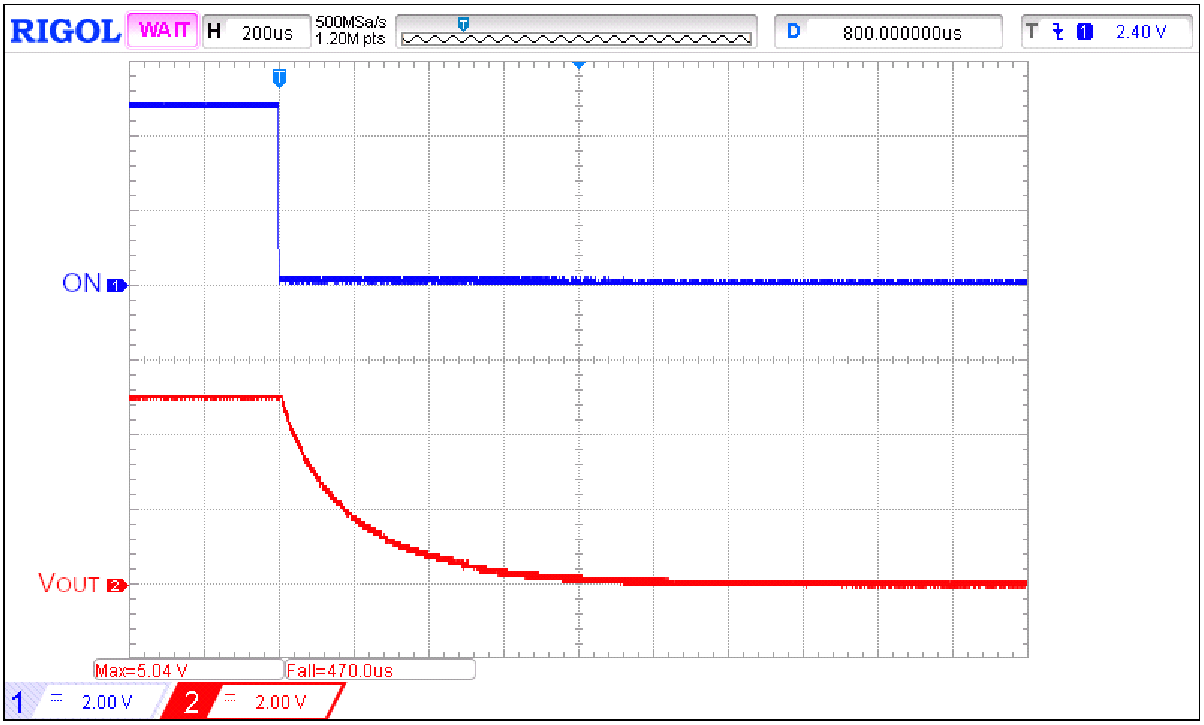


Figure 13. Typical Turn OFF operation waveform for V_{DD} = 5 V, V_{IN} = 5 V, C_{LOAD} = 10 µF, R_{LOAD} = 20 Ω

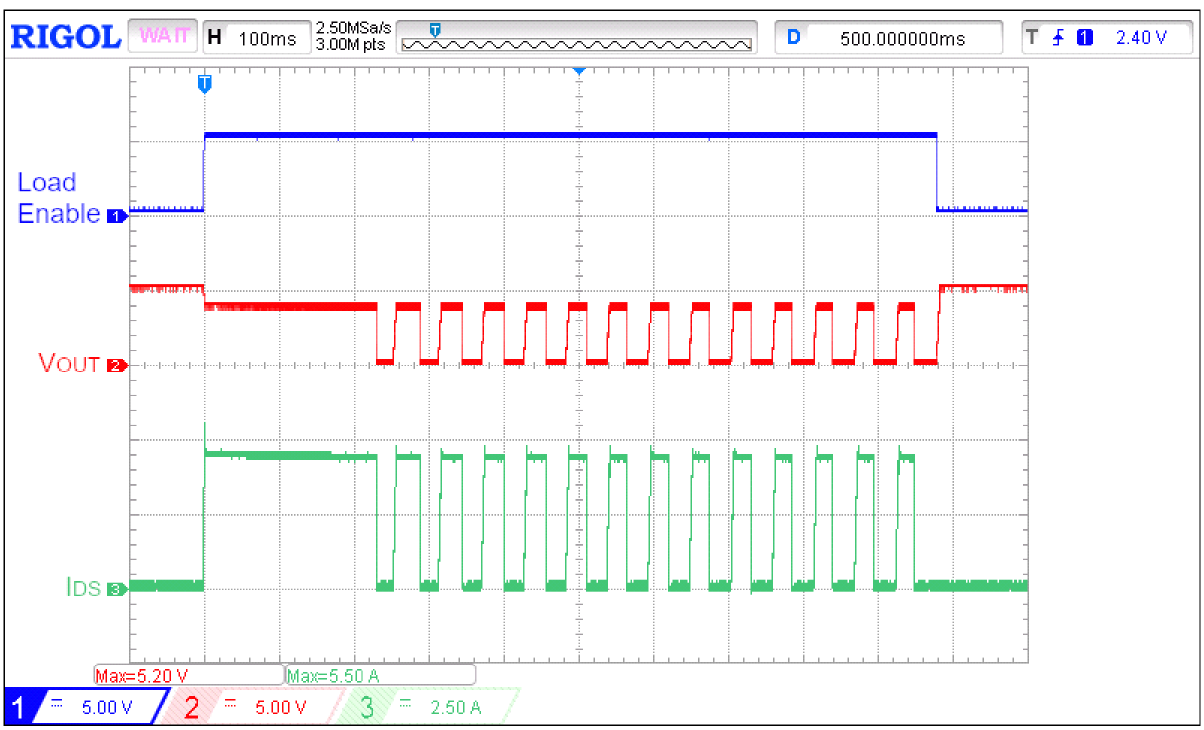


Figure 14. Typical ACL operation waveform for V_{DD} = 5 V, V_{IN} = 5 V, C_{LOAD} = 10 µF, I_{ACL} = 4 A

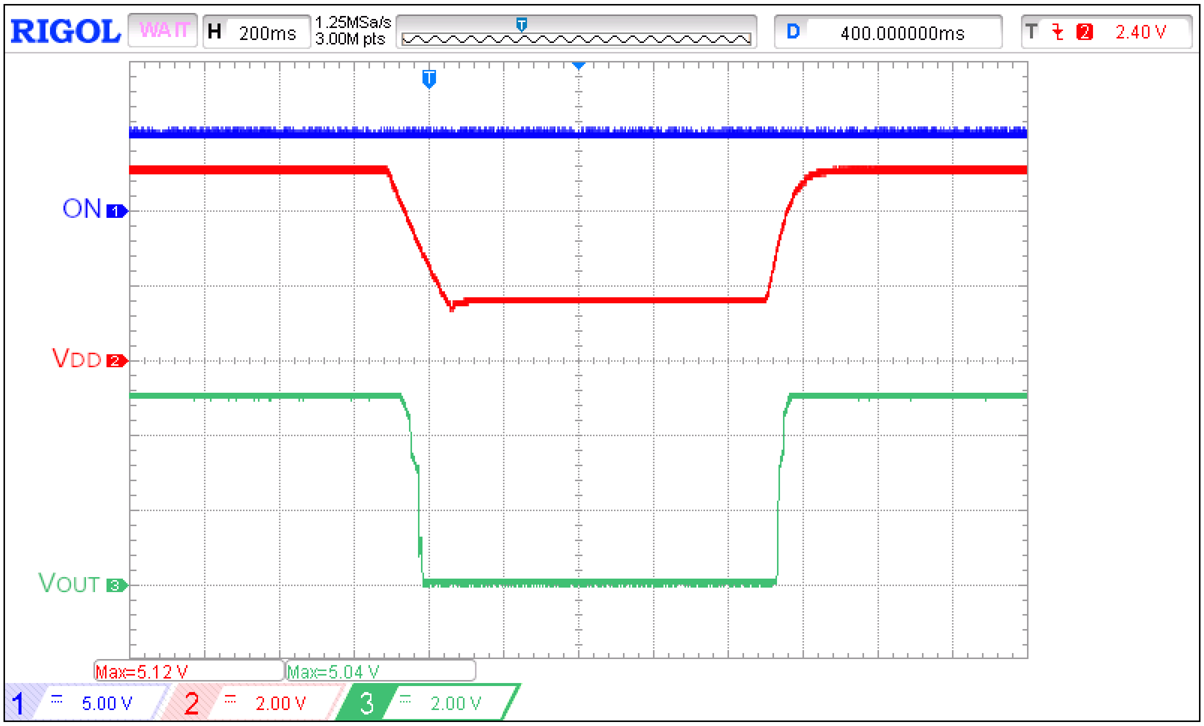


Figure 15. Typical UVP operation waveform for V_{DD} = 5 V, V_{IN} = 5 V, V_{DD} step from 5 V to 1.5 V

SLG59M1713V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_{IN} after V_{DD} exceeds 1.9 V. Then allow V_{IN} to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_{IN} need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 µF C_{LOAD} will prevent glitches for rise times of V_{DD} and V_{IN} less than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_{IN} have reached their steady-state values, the IPS timing parameters may differ from datasheet specifications.

The slew rate of output V_{OUT} follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

SLG59M1713V Current Limiting Operation

The SLG59M1713V has two types of current limiting triggered by the output V_{OUT} voltage.

1. Standard Current Limiting Mode (with Thermal Shutdown Protection)

When the V_{OUT} voltage > 300 mV, the output current is initially limited to the Active Current Limit (I_{ACL}) specification listed in the Electrical Characteristics table. The ACL monitor's response time is very fast and is triggered within a few microseconds to sudden (transient) changes in load current. When a load current overload is detected, the ACL monitor increases the FET resistance to keep the current from exceeding the power switch's I_{ACL} threshold. During active current-limit operation, V_{OUT} is also reduced by I_{ACL} x $RDS_{ON(ACL)}$. This observed behavior is illustrated in the timing diagrams on Pages 8 and 9.

However, if a load-current overload condition persists where the die temperature rises because of the increased FET resistance, the power switch's internal Thermal Shutdown Protection circuit can be activated. If the die temperature exceeds the listed $THERM_{ON}$ specification, the FET is shut OFF completely, thereby allowing the die to cool. When the die cools to the listed $THERM_{OFF}$ temperature threshold, the FET is allowed to turn back on. This process may repeat as long as the output current overload condition persists.

2. Short Circuit Current Limiting Mode (with Thermal Shutdown Protection)

When the V_{OUT} voltage < 300 mV (which is the case with a hard short, such as a solder bridge on the power rail), the power switch's internal Short-circuit Current Limit (SCL) monitor limits the FET current to approximately 500 mA (the I_{SCL} threshold). While the internal Thermal Shutdown Protection circuit remains enabled and since the I_{SCL} threshold is much lower than the I_{ACL} threshold, thermal shutdown protection may become activated only at higher ambient temperatures.

SLG59M1713V Start-up Inrush Current Considerations with Capacitive Loads

In distributed power applications, the SLG59M1713V is generally implemented on the outboard or downstream side of switching regulator dc/dc converters with internal overcurrent protection. As an adjustable output voltage slew-rate, integrated power switch, it is important to understand the start-up operation of the SLG59M1713V with capacitive loads. An equivalent circuit of the SLG59M1713V's slew-rate control loop with capacitors at its VIN and VOUT pins is shown in Figure 16:

SLG59M1713V Start-up Inrush Current Considerations with Capacitive Loads (continued)

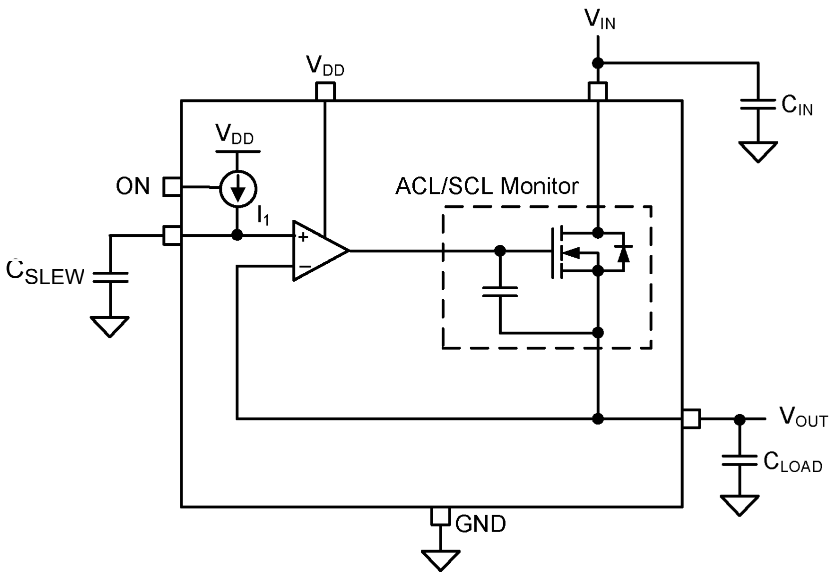


Figure 16. SLG59M1713V's Equivalent Slew-rate Control Loop Circuit

For a desired V_{OUT} slew-rate ($V_{OUT(SR)}$), a corresponding C_{SLEW} value is selected. At the VOUT pin and with ON = LOW, the internal FET is OFF, V_{OUT} is initially at 0 V, and there is no stored charge on C_{LOAD}. When a low-to-high transition is applied to the IC's ON pin, an internal current source (I_1) is enabled which, in turn, charges the external slew-rate capacitor, C_{SLEW}. The SLG59M1713V's internal micropower op amp sets the circuit's $V_{OUT(SR)}$ based on the slew rate of the nodal voltage at its non-inverting pin (the voltage at the CAP pin).

As a function of $V_{OUT(SR)}$ and C_{LOAD}, a 1st-order expression for the circuit's FET current (and inrush current) when a low-to-high transition on the ON pin is applied becomes:

$$\text{Start-up Current } I_{DS} \text{ or } I_{INRUSH} = V_{OUT(SR)} \times C_{LOAD}$$

From the expression above and for a given $V_{OUT(SR)}$, C_{LOAD} determines the magnitude of the inrush current; that is, for large values of C_{LOAD}, large inrush currents can result. If the inrush currents are large enough to trigger the overcurrent protection of an upstream dc/dc converter, the system can be shut down.

In applications where the desired $V_{OUT(SR)}$ is fast and C_{LOAD} is very large (>200 µF), there is a secondary effect on the observed $V_{OUT(SR)}$ attributed to the SLG59M1713V's internal short-circuit current limit monitor (its SCL monitor). If the resultant inrush current is larger than the IC's I_{SCL} threshold, the SCL current monitor limits the inrush current and the current to charge C_{LOAD} until the I_{SCL} OFF threshold is crossed (~0.3V). During the time the SCL monitor's been activated, the inrush current profile may exhibit an observable reduction in $V_{OUT(SR)}$ as shown in Figure 17 where C_{SLEW} was set to 1.5 nF and 470 µF was chosen for C_{LOAD}.

SLG59M1713V Start-up Inrush Current Considerations with Capacitive Loads (continued)

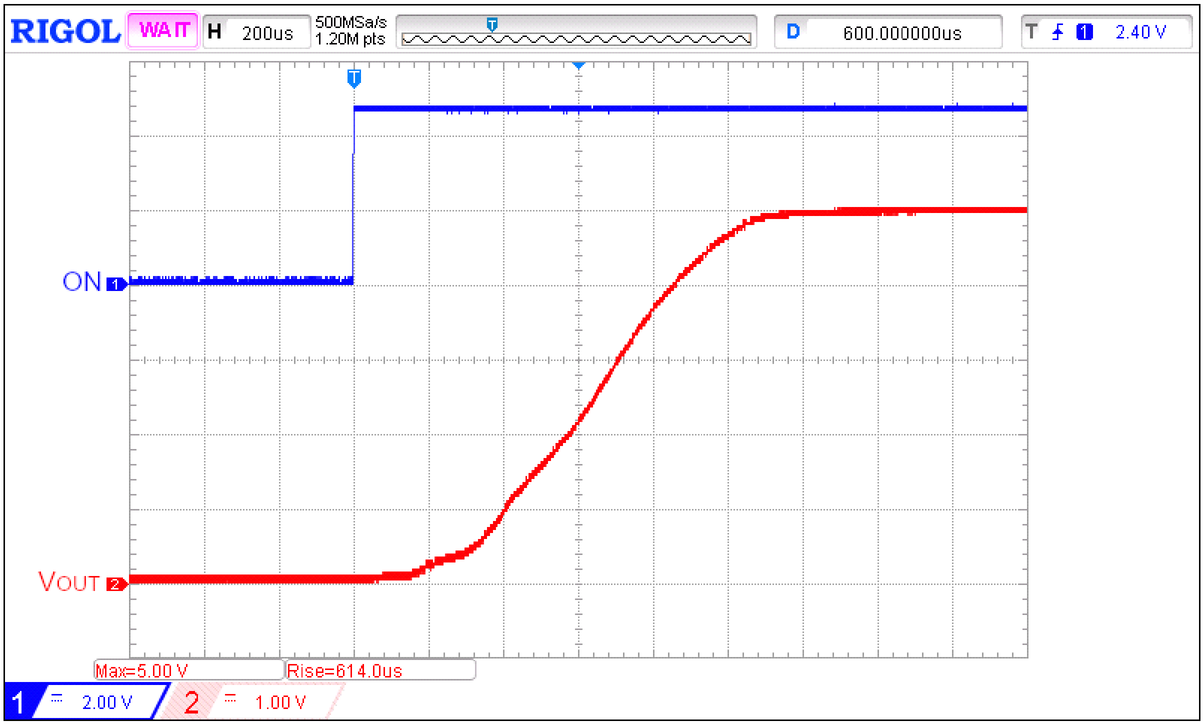


Figure 17. A SLG59M1713V with C_{SLEW} set to 1.5 nF and 470 μF for C_{LOAD}. C_{LOAD}-to-C_{SLEW} ratio is greater than 33,600. Note that the internal SCL monitor's been triggered and $V_{OUT(SR)}$ is reduced until V_{OUT} reaches ~0.3 V.

A closer analysis of the IC's internal slew-control large-scale yields the following:

$$\frac{I_{SCL}}{C_{LOAD}} = M_{SR} \times \frac{I_1}{C_{SLEW}}$$

where

I_{SCL} = IC's short-circuit current limit threshold, typically 0.5 A;
M_{SR} = An internal slew-rate multiplier from the IC's CAP pin to the VOUT pin;
I_1 = An internal current source to charge the external capacitor (C_{SLEW}).

Rearranging the equation to isolate both C_{LOAD} and C_{SLEW} yields the following:

$$\frac{C_{LOAD}}{C_{SLEW}} = \frac{I_{SCL}}{I_1 \times M_{SR}}$$

For the SLG59M1713V device, the right-hand side of the expression is approximately 33,600 after taking into account part-to-part variations because of process, voltage, and temperature.

Referring to the configuration of Figure 17's scope capture, the C_{LOAD}-to-C_{SLEW} ratio is 313,333 (470 μF/1.5 nF) where it is evident that the SCL monitor circuit is charging C_{LOAD} shortly after a low-to-high ON transition. If it is desired to avoid a reduction in $V_{OUT(SR)}$, the choices are decreasing C_{LOAD} and/or increasing C_{SLEW} so that the ratio is always less than 33,600 including taking into account external capacitor tolerances for initial accuracy and temperature.

As shown in Figure 18, it was chosen to reduce $V_{OUT(SR)}$ by increasing C_{SLEW} to 15 nF while keeping C_{LOAD} at 470 μF. With this configuration, the ratio of C_{LOAD} to C_{SLEW} is about 31,333 (smaller than 33,600). Upon a low-to-high transition on the ON pin, the V_{OUT} increases smoothly with no evidence of SCL monitor's interaction.

SLG59M1713V Start-up Inrush Current Considerations with Capacitive Loads (continued)

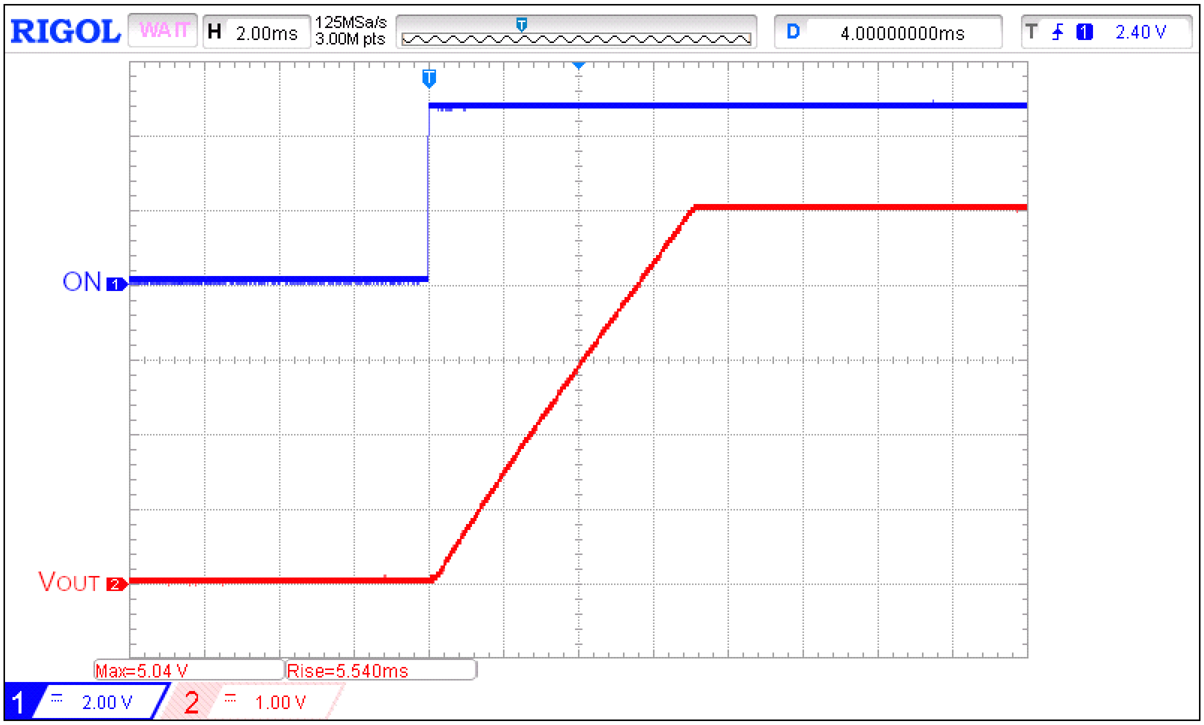


Figure 18. A SLG59M1713V with C_{SLEW} set to 15 nF and 470 μF retained for C_{LOAD}. C_{LOAD}-to-C_{SLEW} ratio is smaller than 33,600. Note smooth V_{OUT} transition.

Power Dissipation

The junction temperature of the SLG59M1713V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59M1713V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:

PD = Power dissipation, in Watts (W)
RDS_{ON} = Power MOSFET ON resistance, in Ohms (Ω)
I_{DS} = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:
T_J = Junction temperature, in Celsius degrees (°C)
θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W)
T_A = Ambient temperature, in Celsius degrees (°C)

Power Dissipation (continued)

During active current-limit operation, the SLG59M1713V's power dissipation can be calculated by taking into account the voltage drop across the power switch (V_{IN}-V_{OUT}) and the magnitude of the output current in active current-limit operation (I_{ACL}):

$$PD = (V_{IN} - V_{OUT}) \times I_{ACL} \text{ or}$$

$$PD = (V_{IN} – (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)
V_{IN} = Input Voltage, in Volts (V)
R_{LOAD} = Load Resistance, in Ohms (Ω)
I_{ACL} = Output limited current, in Amps (A)
$V_{OUT} = R_{LOAD} \times I_{ACL}$

For more information on Dialog GreenFET3 integrated power switch features, please visit our Documents search page at our website and see App Note "AN-1068 GreenFET3 Integrated Power Switch Basics".

Layout Guidelines:

1. The VDD pin needs a 0.1 µF (or larger) external capacitor to smooth pulses from the power supply. Locate this capacitor as close as possible to the SLG59M1713V's pin 1.

2. Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 19, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1713V's VIN and VOUT pins;

4. The GND pin should be connected to system analog or power ground plane.

5. 2 oz. copper is recommended for high current operation.

SLG59M1713V Evaluation Board:

A GFET3 Evaluation Board for SLG59M1713V is designed according to the statements above and is illustrated on Figure 19. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

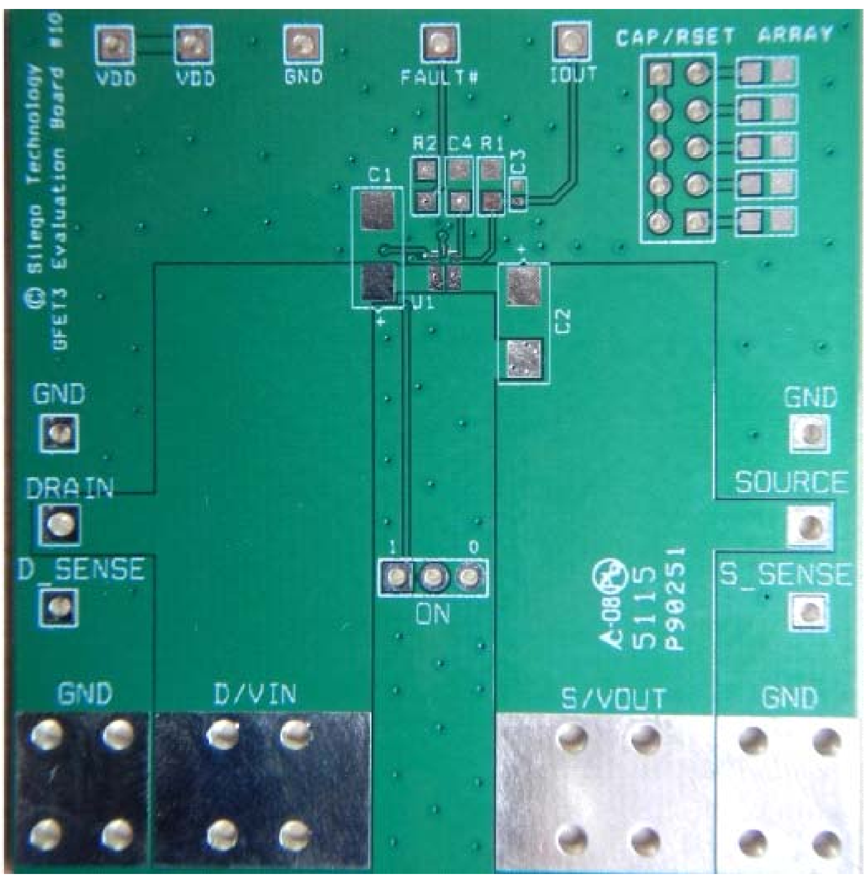


Figure 19. SLG59M1713V Evaluation Board

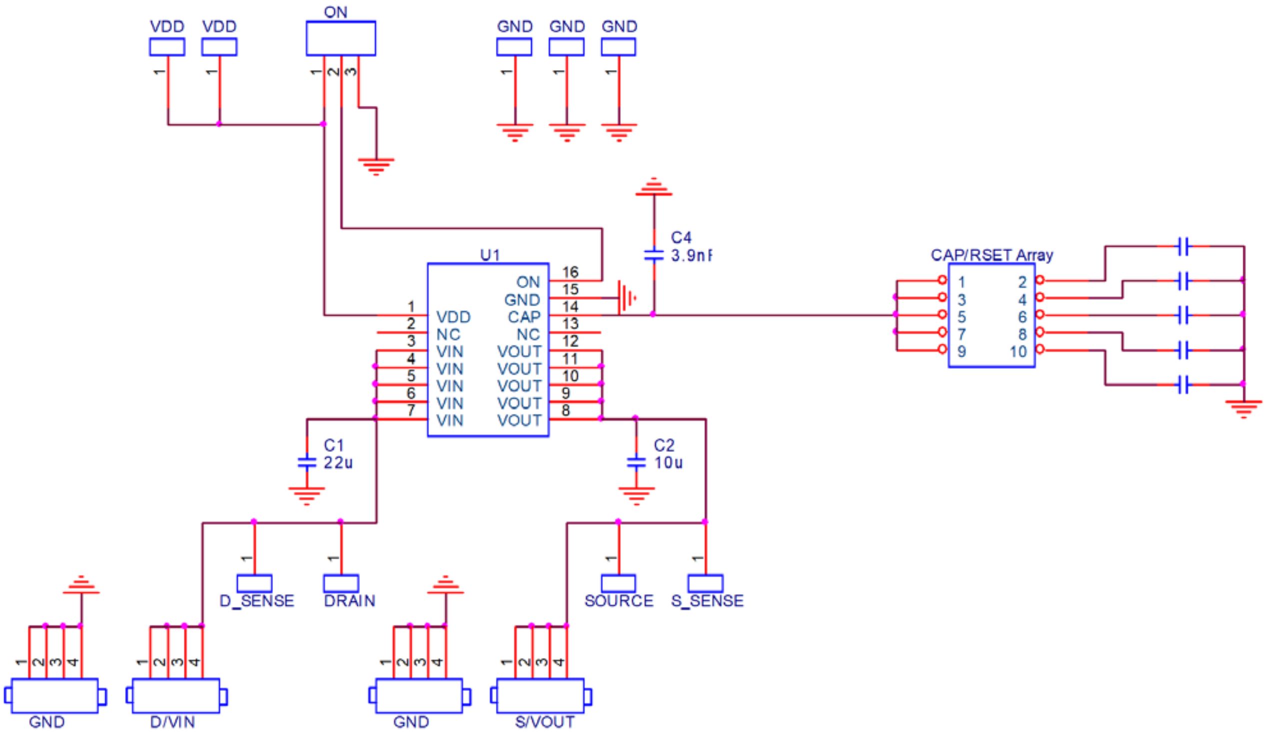


Figure 20. SLG59M1713V Evaluation Board Connection Circuit

Basic Test Setup and Connections

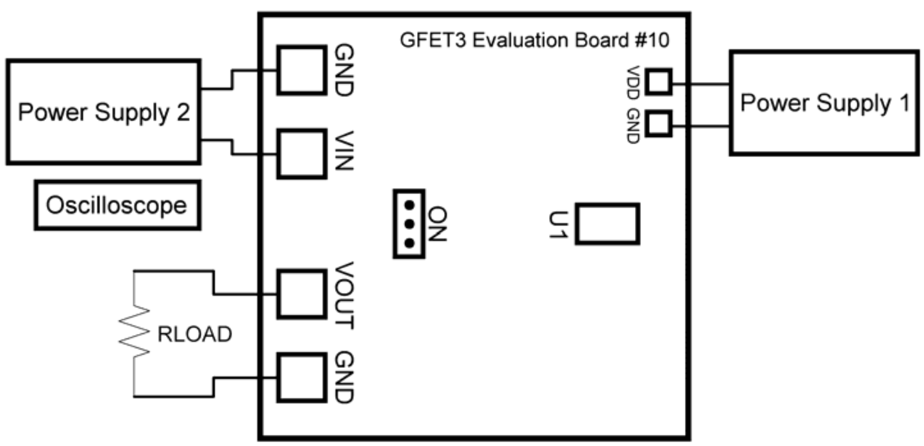


Figure 21. SLG59M1713V Evaluation Board Connection Circuit

EVB Configuration

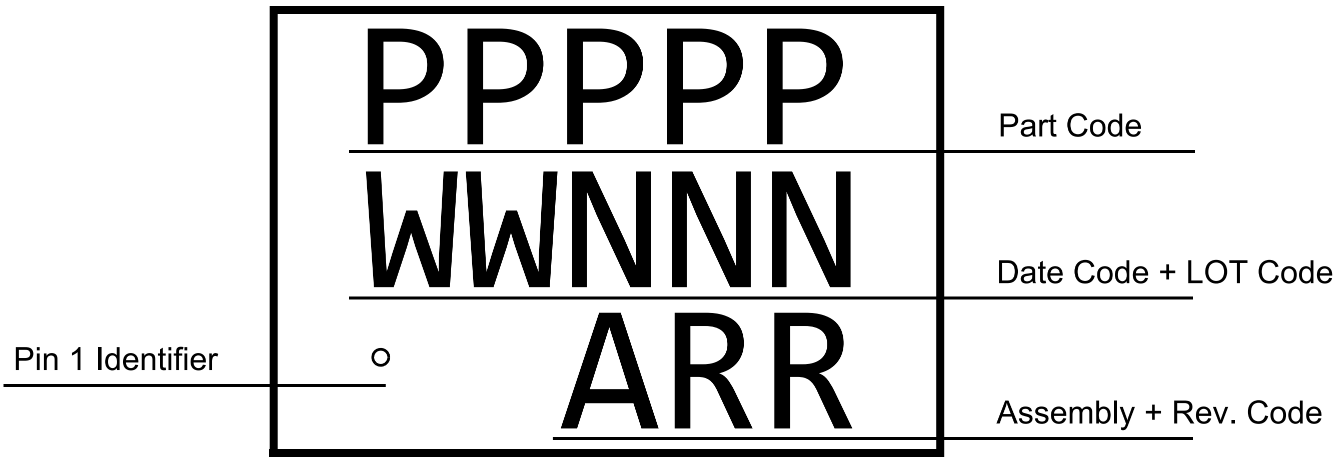
1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;

2. Turn on Power Supply 1 and set desired V_{DD} from 2.5 V…5.5 V range;

3. Turn on Power Supply 2 and set desired V_{IN} from 0.8 V…V_{DD} range;

4 .Toggle the ON signal High or Low to observe SLG59M1713V operation.

Package Top Marking System Definition

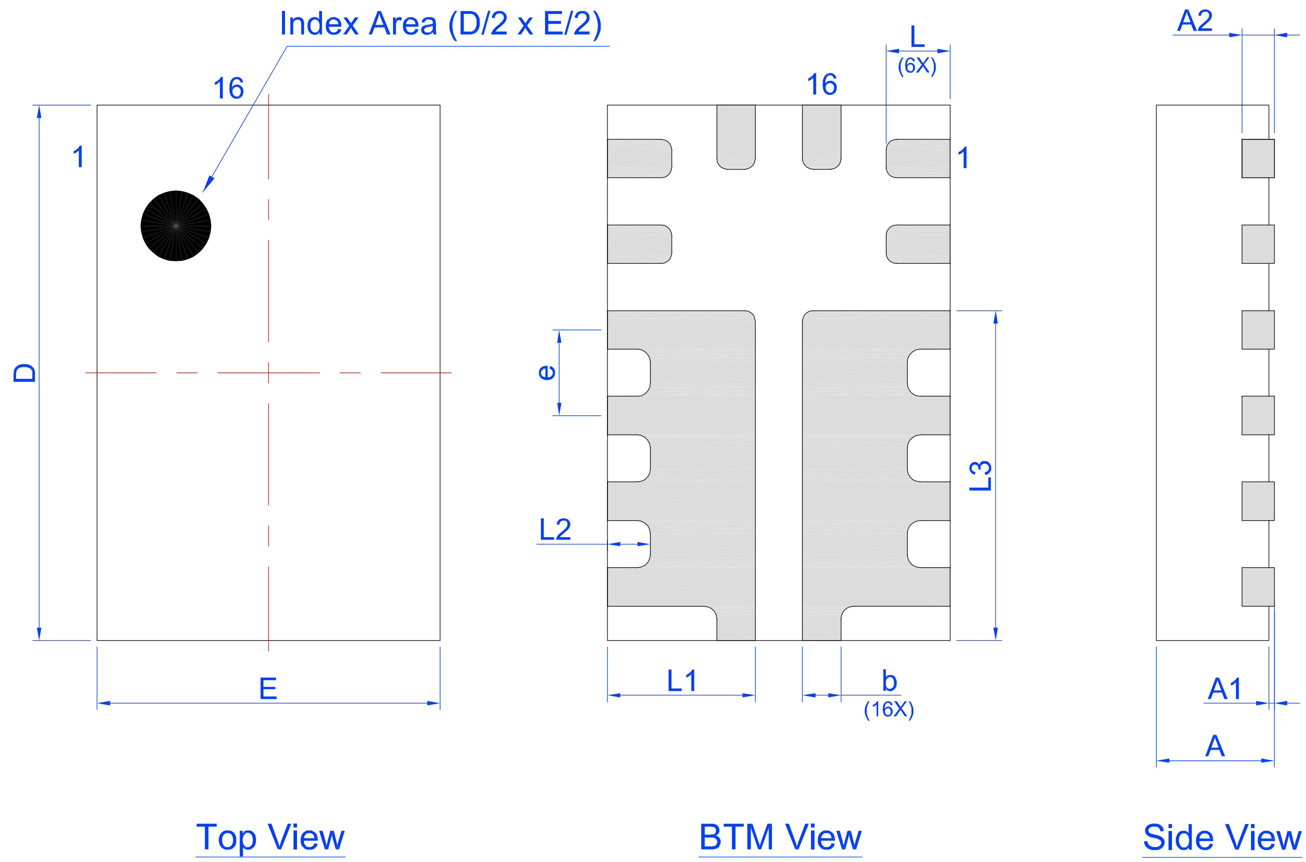


PPPPP - Part ID Field
WW - Date Code Field[1]
NNN - Lot Traceability Code Field[1]
A - Assembly Site Code Field [2]
RR - Part Revision Code Field[2]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

Package Drawing and Dimensions

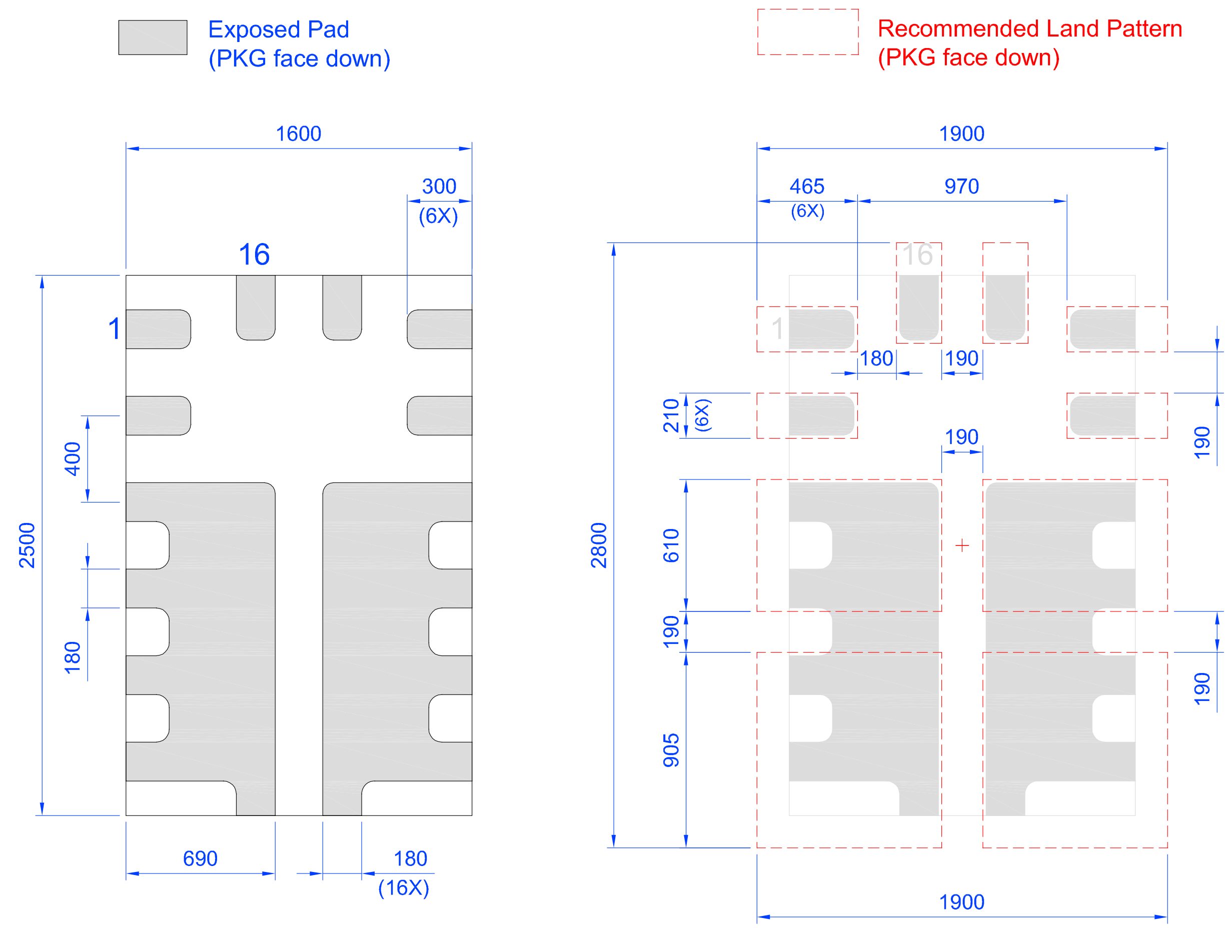
16 Lead STQFN Package 1.6 mm x 2.5 mm (Fused Lead)



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.45	2.50	2.55
A1	0.005	-	0.05	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.64	0.69	0.74
e	0.40 BSC			L2	0.15	0.20	0.25
				L3	1.49	1.54	1.59

SLG59M1713V 16-pin STQFN PCB Landing Pattern



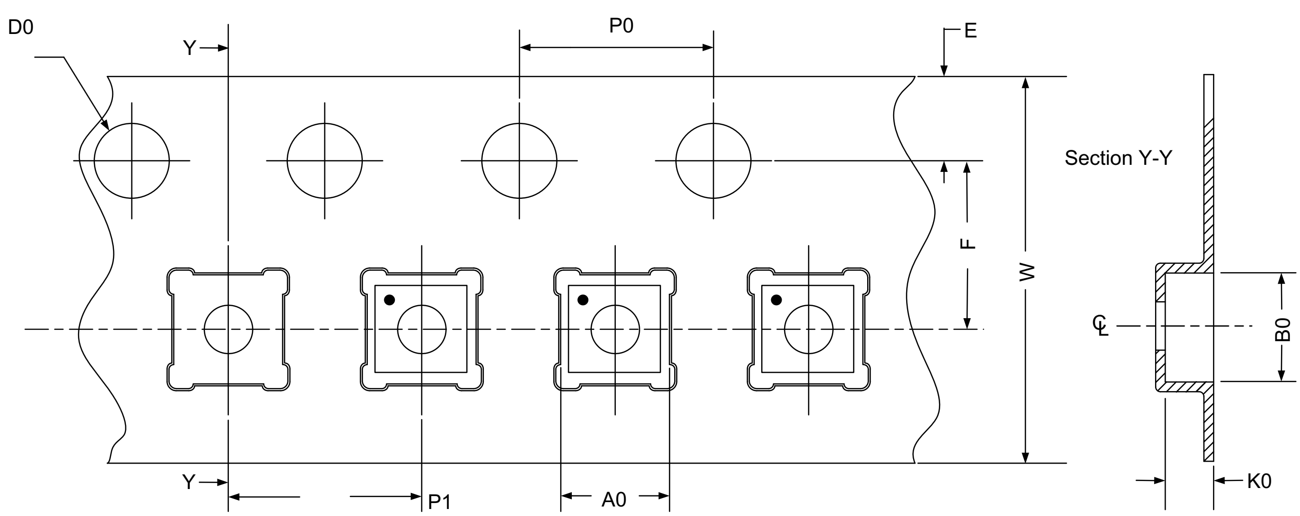
Unit: um

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 16L 1.6x2.5mm 0.4P FCA Green	16	1.6x2.5x 0.55mm	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	PocketBTM Length	PocketBTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 16L 1.6x2.5mm 0.4P FCA Green	1.8	2.8	0.7	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.2 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
4/16/2019	1.03	Updated Charts Added Scopeshots
4/11/2019	1.02	Updated Timing Diagrams for clarification
4/5/2019	1.01	Updated Style and formatting Added Layout Guidelines Fixed typos
2/23/2017	1.00	Production Release