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Description

The SLG59M1742C is a 18 mΩ, ~1 A single-channel load switch that is able to switch 0.25 V to 1.5 V power rails. The product is packaged in an ultra-small 0.71 x 1.16 mm package.

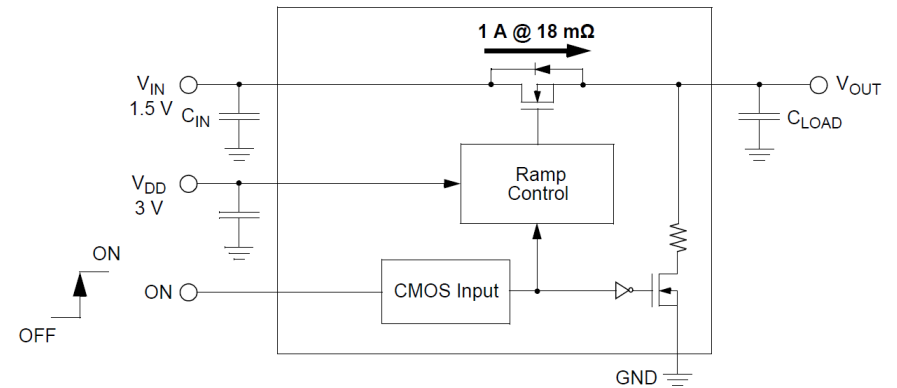


Figure 1: SLG59M1742C Block Diagram

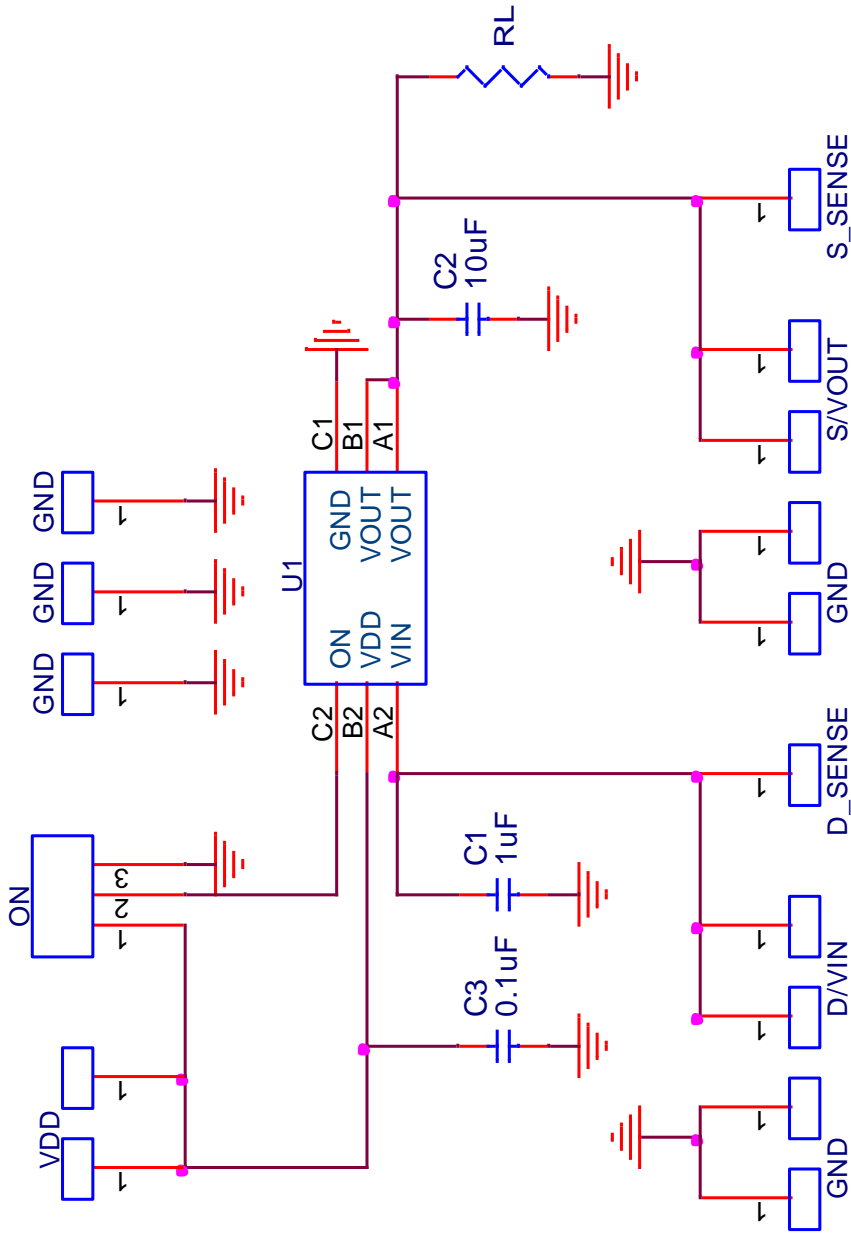
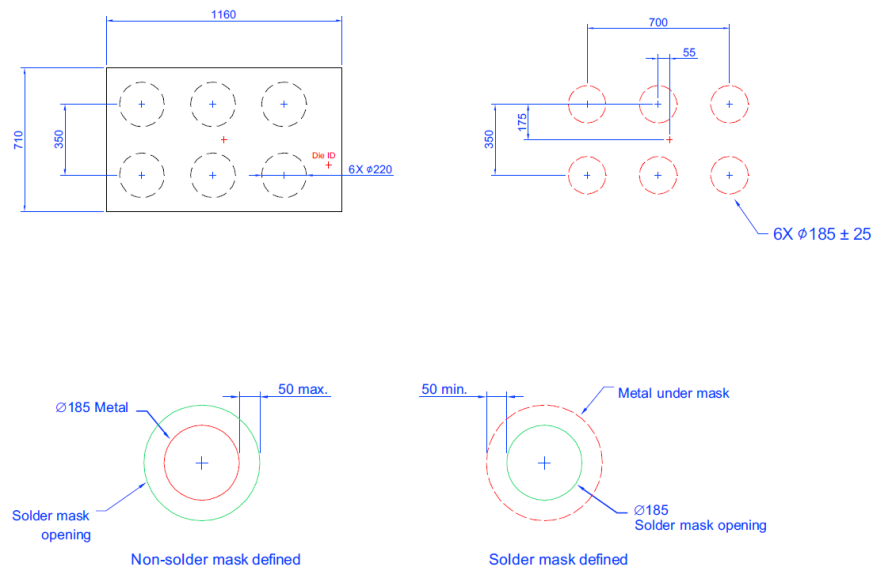


Figure 4. SLG59M1742C Connection Circuit

This layout guide provides some important information about the PCB layout of SLG59M1742C applications.

SILEGO WLCSP 0.71x1.16-6B PKG

Unit: μm



[Solder mask detail \(not to scale\)](#)

Figure 2. SLG59M1742C Package Dimensions and Recommended Land Pattern

2. Power and Ground Planes

- 2.1. The VDD pin (B2) needs a $0.1\mu\text{F}$ (or larger) external capacitor to smooth pulses from the power supply. Locate this capacitor as close to B2 pin.
- 2.2. The trace length from the control IC to the ON pin should be as short as possible and must avoid crossing this trace with power rails.
- 2.3. The VIN and VOUT pins carry significant current. Please note how the VIN and VOUT pads are placed directly on the power planes in Figure 3, which minimizes the $R_{DS\text{ON}}$ associated with long, narrow traces. The VIN, VOUT and GND pins dissipate most of the heat generated during high-load current condition. The layout shown in Figure 3 is illustrating a proper solution for heat to transfer as efficiently as possible out of the device.
- 2.4. Connect a $1\mu\text{F}$ (or larger) low-ESR capacitor from VIN pin (A2) to ground.
- 2.5. The GND pin (C1) should be connected to GND.

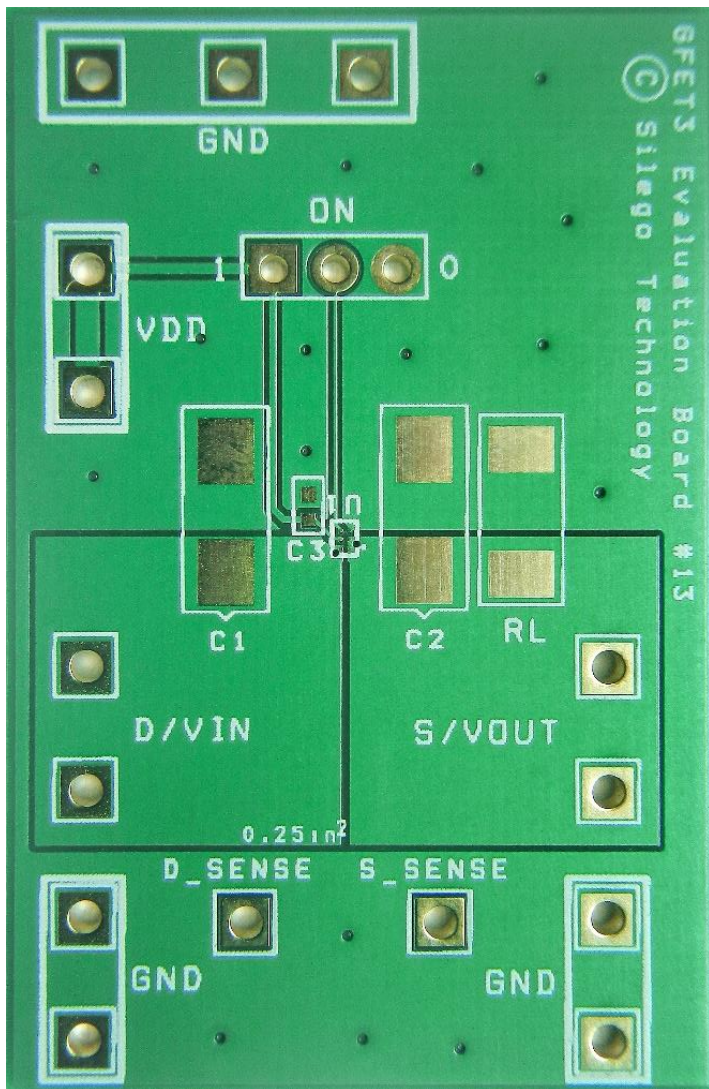


Figure 3. SLG59M1742C Evaluation Test Board

Note: Evaluation board has D_Sense and S_Sense pads. Please use them only for $R_{DS(on)}$ evaluation.

3. Basic Test Setup and Connections

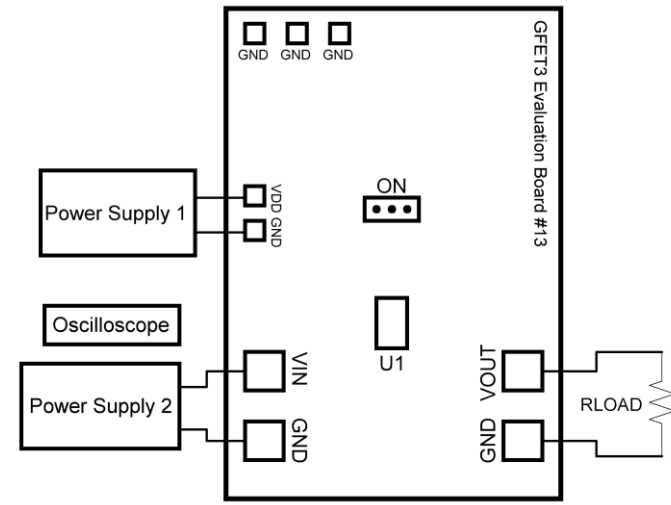


Figure 5. Typical connections for GFET3 Evaluation

3.1 EVB Configuration

1. Connect oscilloscope probes to VIN, VOUT, ON, etc.
2. Turn ON Power Supply 1 and set desirable V_{DD} in range of 2.7 V...3.6 V
3. Turn ON Power Supply 2 and set desirable V_{IN} in range of 0.25 V...1.5 V
4. Switch ON to High or Low to evaluate GFET3 operation