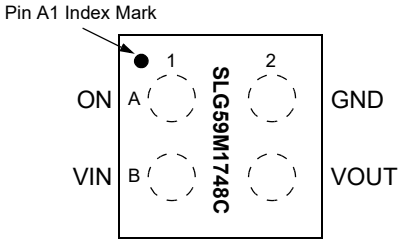
A Reverse Blocking 36 mΩ, 2.2 A pFET Integrated Power Switch in 0.64 mm^2 WLCSP

General Description

Operating from a 1.6 V to 5 V power supply, the SLG59M1748C is a self-powered, high-performance, 36 mΩ pFET integrated power switch designed for high-side power-rail applications up to 2.2 A. When ON, internal reverse-current protection will quickly open the switch in the event of a reverse-voltage condition is detected (a $V_{OUT} > V_{IN} + 32$ mV condition opens the switch). When OFF, the pFET's internal body diode is connected to the higher voltage of V_{IN}/V_{OUT} to prevent reverse-path leakage current. The SLG59M1748C is an ideal pFET integrated power switch in any application where two power sources are likely to be multiplexed to one output.

Pin Configuration



4L WLCSP
(Laser Marking View)

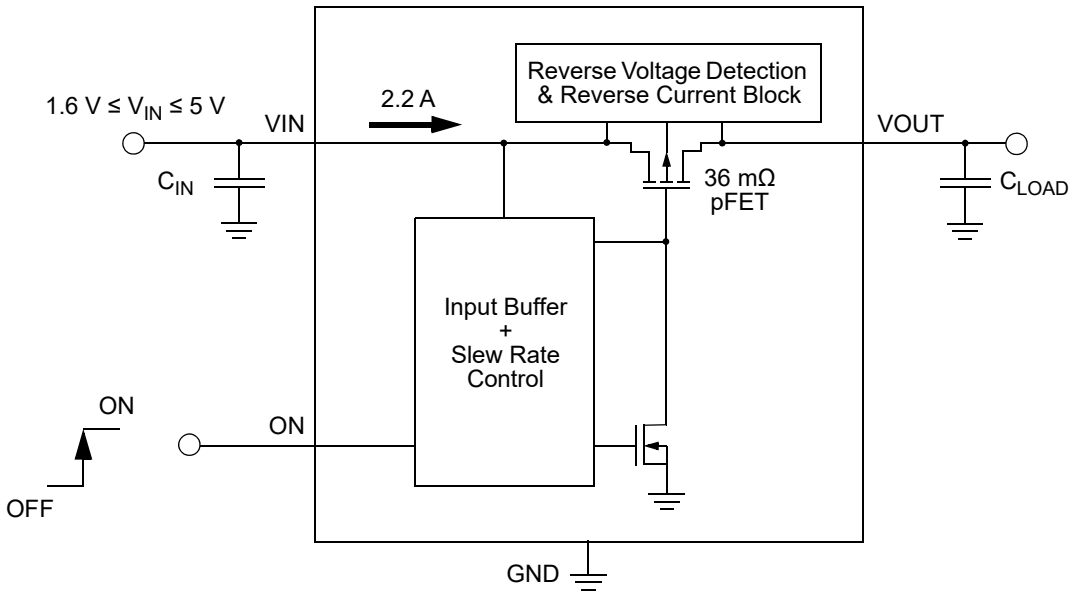
Features

- Integrated 2.2 A Continuous I_{DS} pFET Power Switch
- Low Typical RDS_{ON}:
  - 36 mΩ at V_{IN} = 5 V
  - 46.9 mΩ at V_{IN} = 3.3 V
  - 58.9 mΩ at V_{IN} = 2.5 V
  - 100 mΩ at V_{IN} = 1.6 V
- Input Voltage: 1.6 V to 5 V
- Operating Temperature: -40 °C to 85 °C
- Low θ_{JA}, 4-pin 0.8 mm x 0.8 mm, 0.4 mm pitch 4L WLCSP Packaging
- Pb-Free / Halogen-Free / RoHS compliant

Applications

- Fast Turn On/Off power rail switching with big load capacitance
- Frequent wake & sleep power cycle
- Mobile devices and portable devices

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
A1	ON	Input	A low-to-high transition on this pin initiates the operation of the SLG59M1748C. ON is an asserted HIGH, level-sensitive CMOS input with ON_V_{IL} < 0.3 V and ON_V_{IH} > 0.85 V. As the ON pin input circuit does not have an internal pull-down resistor, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited.
B1	VIN	MOSFET	Input terminal connection of the p-channel MOSFET. Connect a 10 µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at 10 V or higher.
B2	VOUT	MOSFET	Output terminal connection of the p-channel MOSFET. Capacitors used at VOUT should be rated at 10 V or higher.
A2	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59M1748C	WLCSP 4L	Industrial, -40 °C to 85 °C
SLG59M1748CTR	WLCSP 4L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{IN}	Power Switch Input Voltage			--	--	6	V
V_{OUT} to GND	Power Switch Output Voltage to GND			-0.3	--	6	V
ON to GND	ON Pin Voltage to GND			-0.3	--	V_{IN}	V
T_S	Storage Temperature			-65	--	140	°C
ESD_{HBM}	ESD Protection	Human Body Model		2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model		500	--	--	V
MSL	Moisture Sensitivity Level			1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	0.8 x 0.8 mm 4L WLCSP; Determined using a 1 in^2, 1 oz .copper pad under each VIN and VOUT terminal and FR4 pcb material.		--	110	--	°C/W
W_{DIS}	Package Power Dissipation			--	--	0.5	W
MOSFET IDS_{PK}	Peak Current from VIN to VOUT	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	V_{IN} = 5 V	--	--	2.5	A
			V_{IN} = 1.6 V	--	--	1.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C. Typical values are at T_A = 25 °C unless otherwise noted.

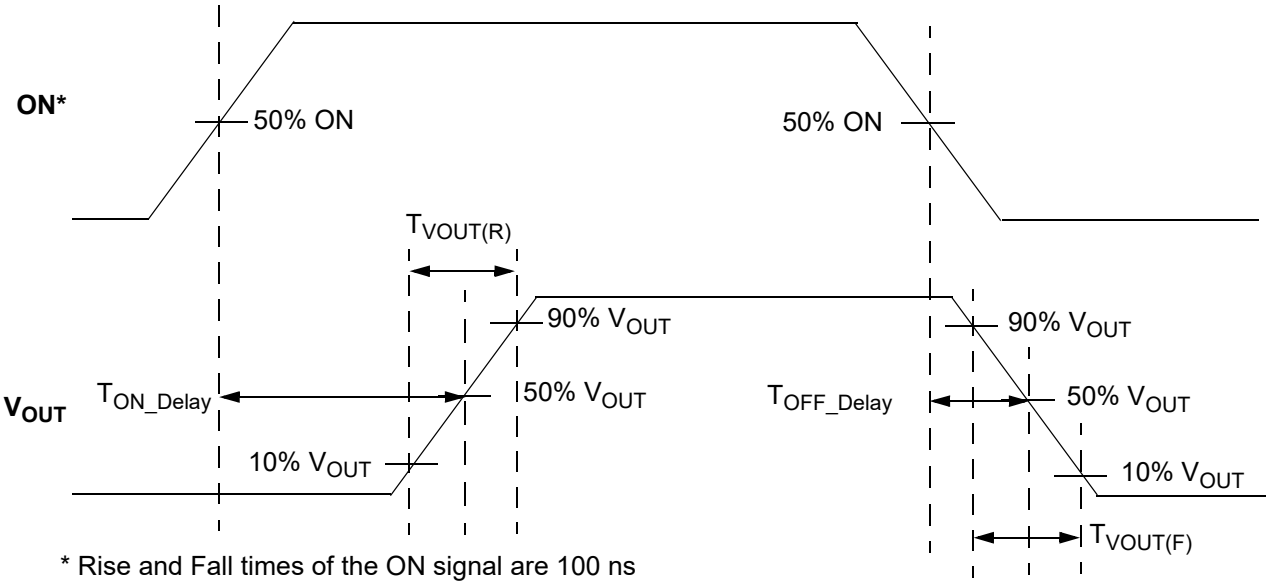
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Switch Input Voltage	-40 °C to 85 °C	1.6	--	5	V
I_{IN}	Power Switch Current (Pin B1)	When OFF, V_{IN} = 5.0 V, No load	--	0.39	0.62	µA
		When OFF, V_{IN} = 3.3 V, No load	--	0.28	0.50	µA
		When OFF, V_{IN} = 2.5 V, No load	--	0.24	0.46	µA
		When OFF, V_{IN} = 1.6 V, No load	--	0.22	0.43	µA
		When ON = V_{IN} = 5.0 V, No load	--	0.47	0.72	µA
		When ON = V_{IN} = 3.3 V, No load	--	0.36	0.53	µA
		When ON = V_{IN} = 2.5 V, No load	--	0.33	0.47	µA
		When ON = V_{IN} = 1.6 V, No load	--	0.30	0.44	µA
I_{ON_LKG}	ON Pin Input Leakage		--	--	0.15	µA
RDS_{ON}	ON Resistance, T_A = 25°C	V_{IN} = 5 V, I_{DS} = 100 mA	--	36	45.1	mΩ
		V_{IN} = 3.3 V, I_{DS} = 100 mA	--	46.9	57.2	mΩ
		V_{IN} = 2.5 V, I_{DS} = 100 mA	--	58.9	72	mΩ
		V_{IN} = 1.6 V, I_{DS} = 100 mA	--	100	121	mΩ
RDS_{ON}	ON Resistance, T_A = 85°C	V_{IN} = 5 V, I_{DS} = 100 mA	--	42.4	51	mΩ
		V_{IN} = 3.3 V, I_{DS} = 100 mA	--	54.5	67.1	mΩ
		V_{IN} = 2.5 V, I_{DS} = 100 mA	--	69.2	84.2	mΩ
		V_{IN} = 1.6 V, I_{DS} = 100 mA	--	115	139	mΩ
MOSFET IDS	Current from VIN to VOUT	Continuous, V_{IN} = 5 V	--	--	2.2	A
		Continuous, V_{IN} = 1.6 V	--	--	1.2	A

Electrical Characteristics (continued)

T_A = -40 °C to 85 °C. Typical values are at T_A = 25 °C unless otherwise noted.

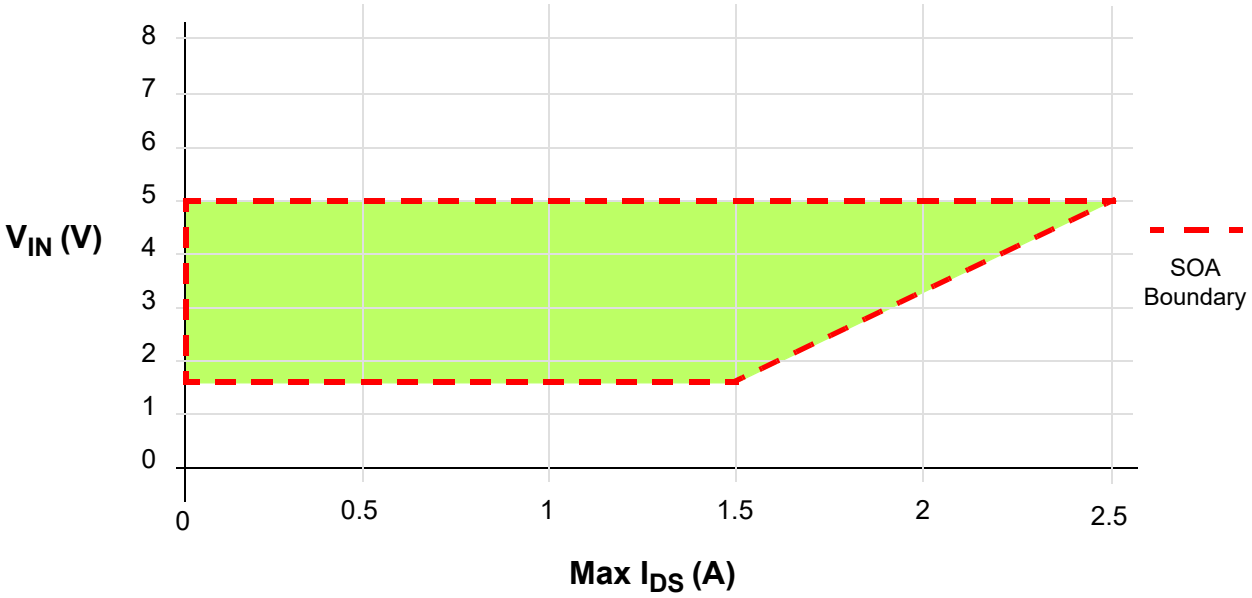
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{FET_OFF}	MOSFET OFF Leakage Current	ON = LOW; V_{OUT} = 0 V, V_{IN} = 5 V	--	0.45	1.7	µA
V_{RVD_T}	Reverse-voltage Detect Threshold Voltage	$V_{OUT} – V_{IN}$; V_{IN} = 5 V; ON = HIGH	--	32	--	mV
T_{RVD_T}	Reverse-voltage Detect Threshold Response Time	V_{IN} = 5 V; ON = HIGH	--	50	--	µs
T_{RVD_REARM}	Reverse-voltage Detect Rearm Time	V_{IN} = 5 V; ON = HIGH; From V_{IN} rise higher than V_{OUT} until $V_{OUT} = V_{IN}$	--	0.8	--	ms
V_{RVD_R}	Reverse-voltage Detect Release Threshold Voltage	$V_{IN} – V_{OUT}$; V_{IN} = 5 V; ON = HIGH	--	2	--	mV
$I_{REVERSE}$	MOSFET Reverse Leakage Current	ON = Don't Care; V_{IN} = 0 V, V_{OUT} = 5 V	--	0.4	1.7	µA
T_{ON_Delay}	ON Delay Time	50% ON to 50% V_{OUT} ↑; V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	0.9	1.3	2	ms
		50% ON to 50% V_{OUT} ↑; V_{IN} = 2.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	0.79	1.1	1.6	ms
		50% ON to 50% V_{OUT} ↑; V_{IN} = 1.6 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	0.70	1	1.45	ms
$T_{VOUT(R)}$	V_{OUT} Rise Time	10% to 90% V_{OUT} ↑; V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	0.8	1.2	1.65	ms
		10% to 90% V_{OUT} ↑; V_{IN} = 2.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	0.5	0.76	1.1	ms
		10% to 90% V_{OUT} ↑; V_{IN} = 1.6 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	0.23	0.5	0.85	ms
$T_{VOUT(F)}$	V_{OUT} Fall Time	90% to 10% V_{OUT} ↓; V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	2.4	3.2	4	µs
		90% to 10% V_{OUT} ↓; V_{IN} = 2.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	2	2.8	3.3	µs
		90% to 10% V_{OUT} ↓; V_{IN} = 1.6 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	1.8	2.6	3.3	µs
T_{OFF_Delay}	OFF Delay Time	50% ON to 50% V_{OUT} ↓; V_{IN} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	4.8	6.2	7.65	µs
		50% ON to 50% V_{OUT} ↓; V_{IN} = 2.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	3.9	5.4	6.9	µs
		50% ON to 50% V_{OUT} ↓; V_{IN} = 1.6 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	4.7	6.6	8.6	µs
ON_V_{IH}	Initial Turn On Voltage		0.85	--	V_{IN}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V

T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



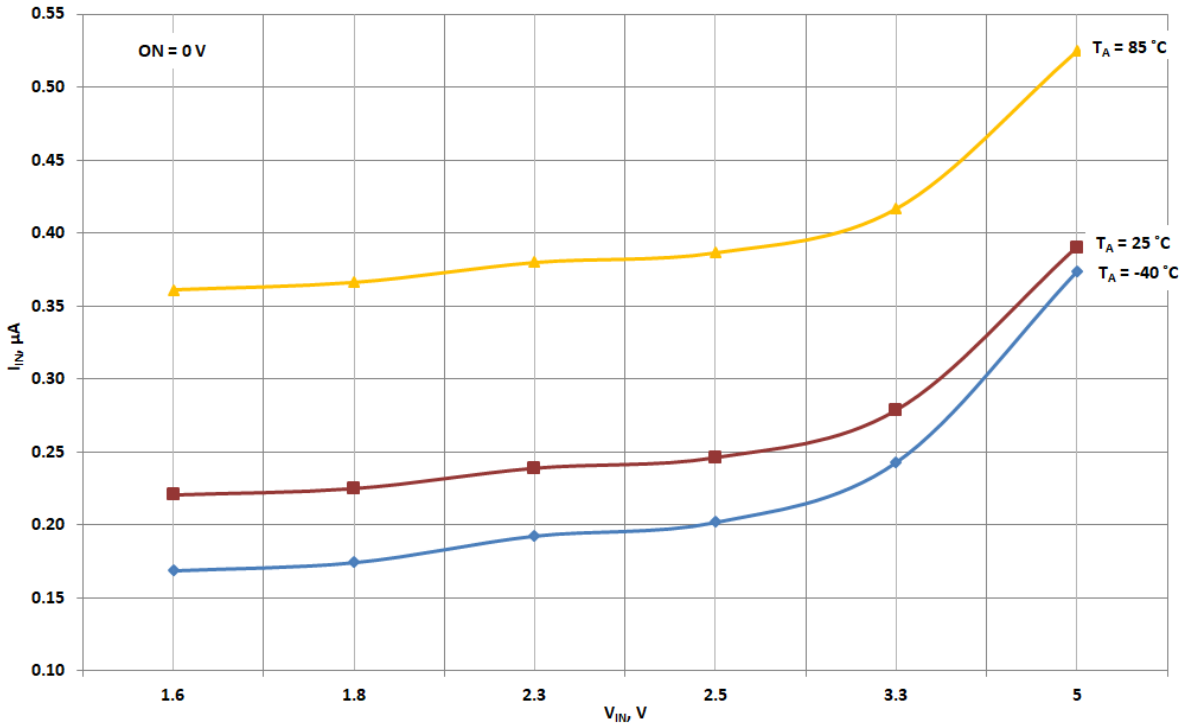
* Rise and Fall times of the ON signal are 100 ns

V_{IN} vs. Max I_{DS}, Safe Operation Area

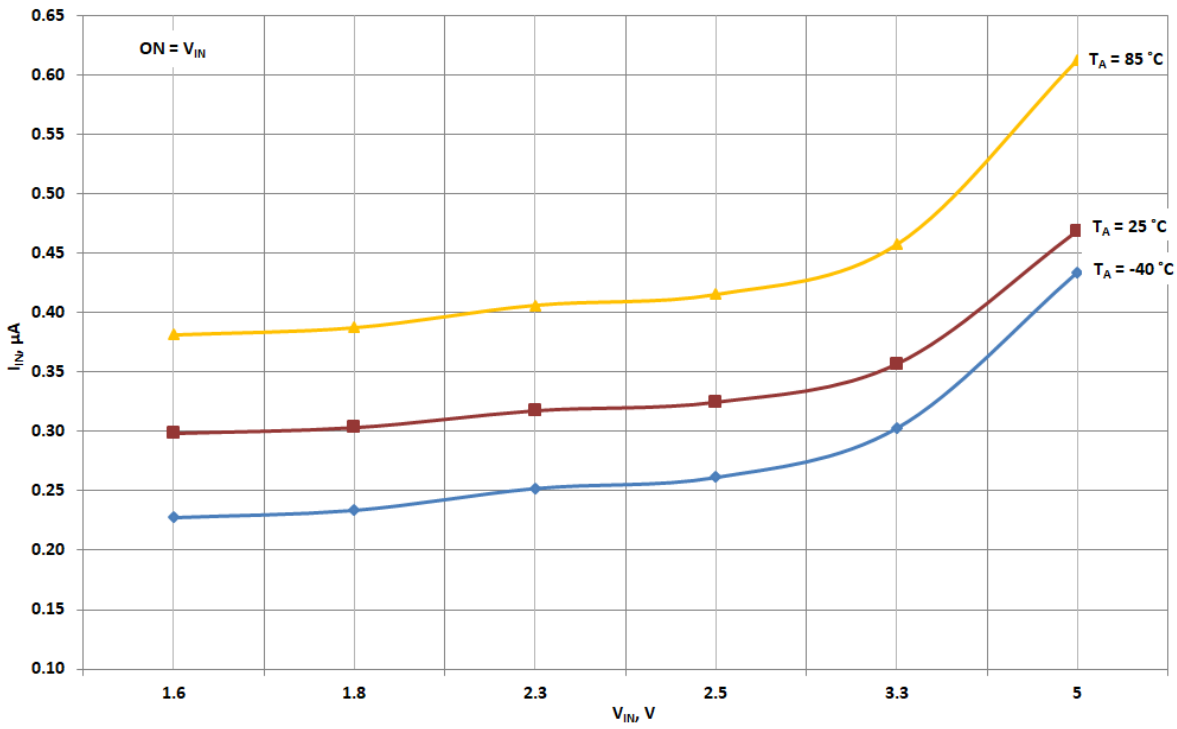


Applications Information

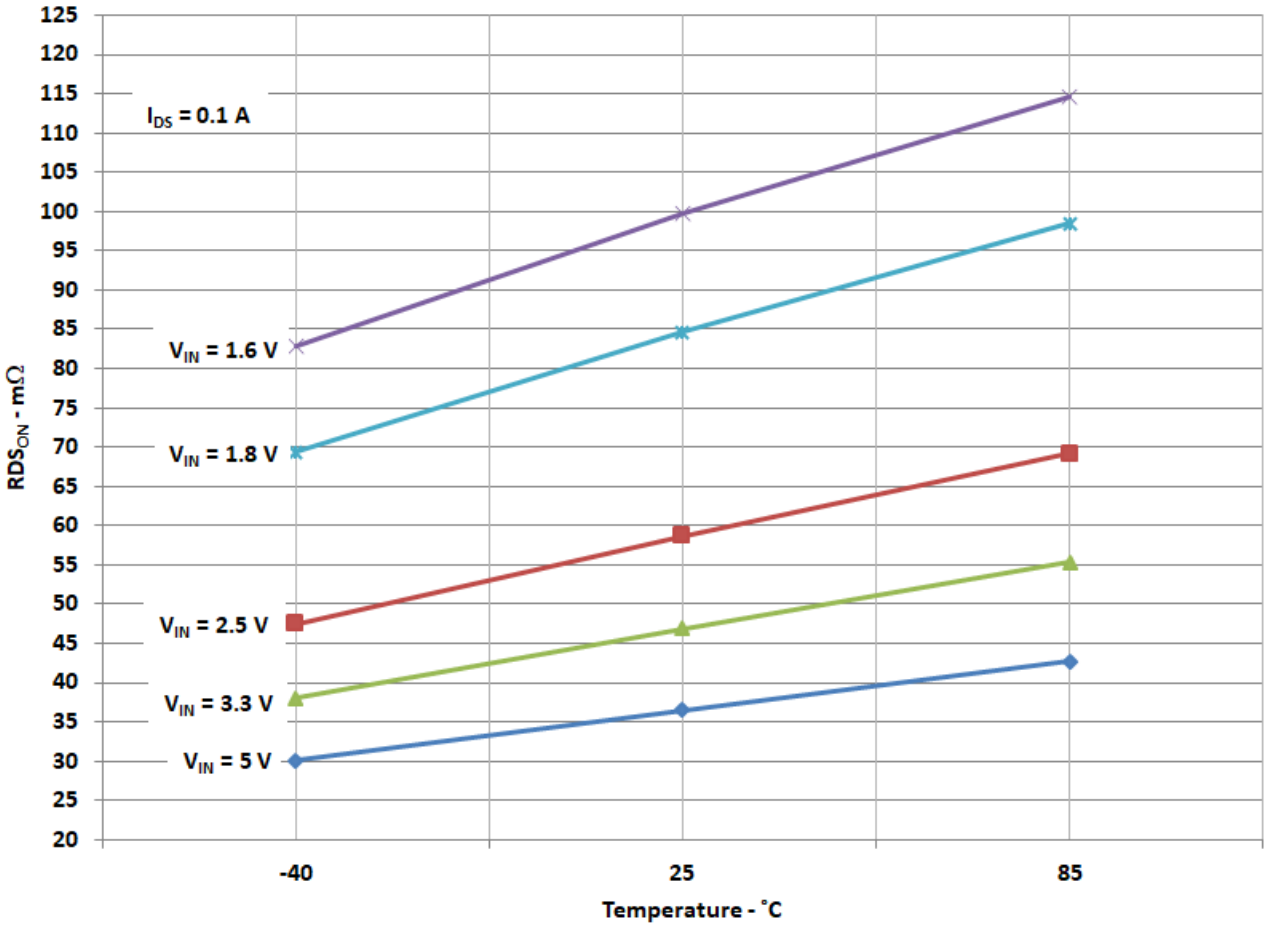
I_{IN} (when OFF) vs. V_{IN} and Temperature



I_{IN} (when ON) vs. V_{IN} and Temperature



RDS_{ON} vs. Temperature and V_{IN}



Typical Turn-on Waveforms

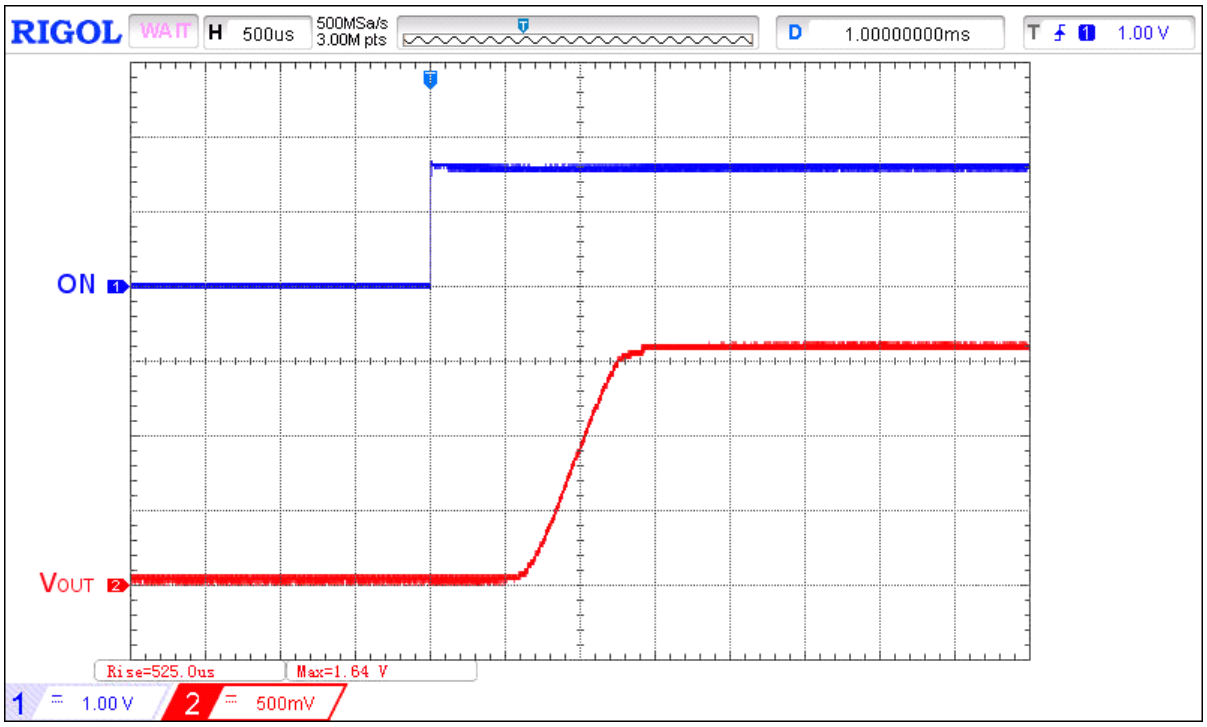


Figure 1. Typical Turn ON operation waveform for V_{IN} = 1.6 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω

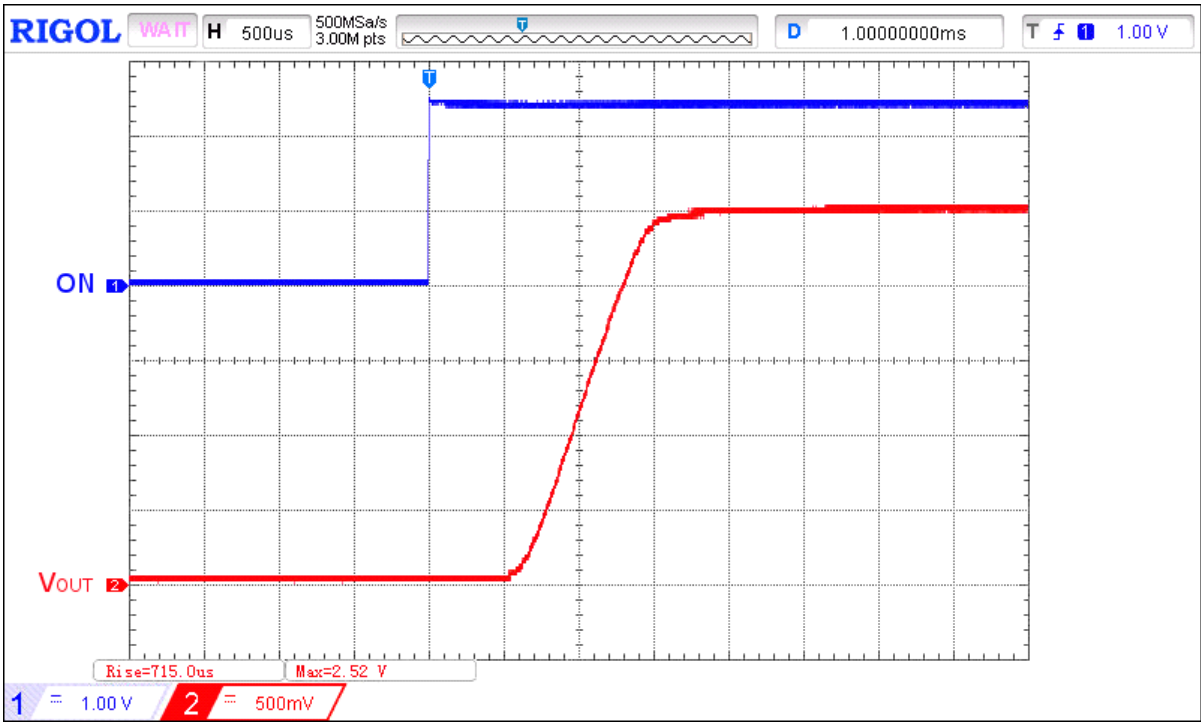


Figure 2. Typical Turn ON operation waveform for V_{IN} = 2.5 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω

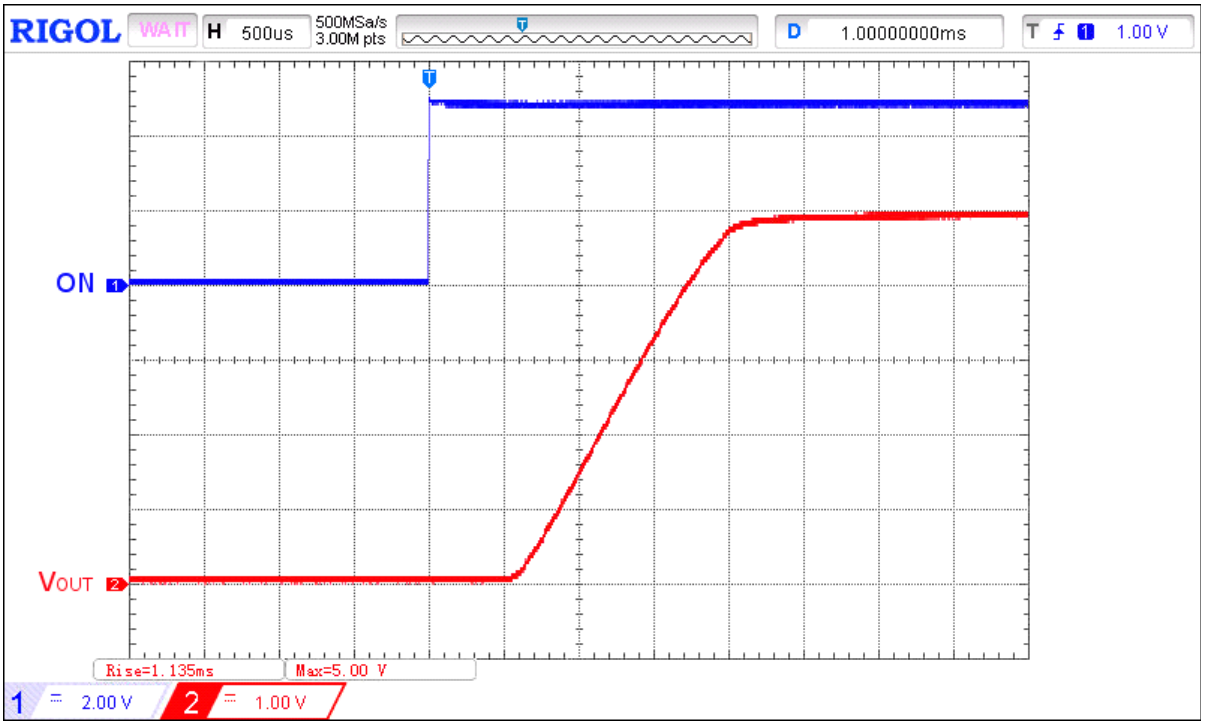


Figure 3. Typical Turn ON operation waveform for V_{IN} = 5 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω

Typical Turn-off Waveforms

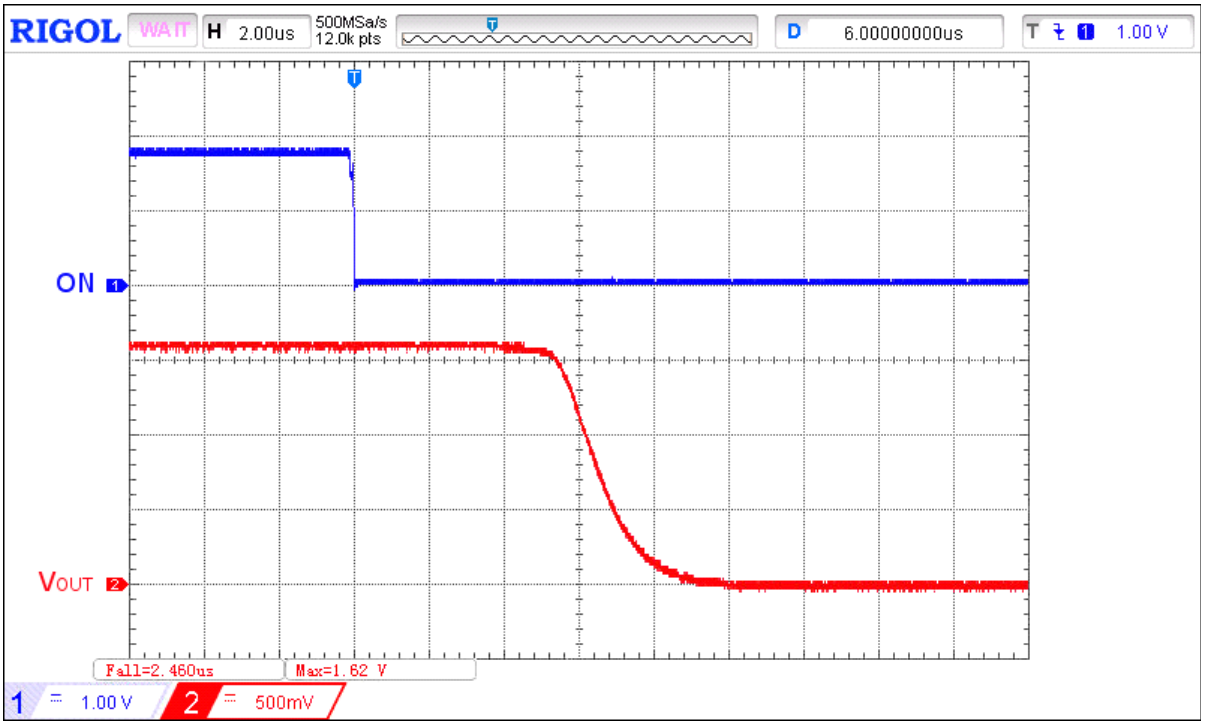


Figure 4. Typical Turn OFF operation waveform for V_{IN} = 1.6 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω

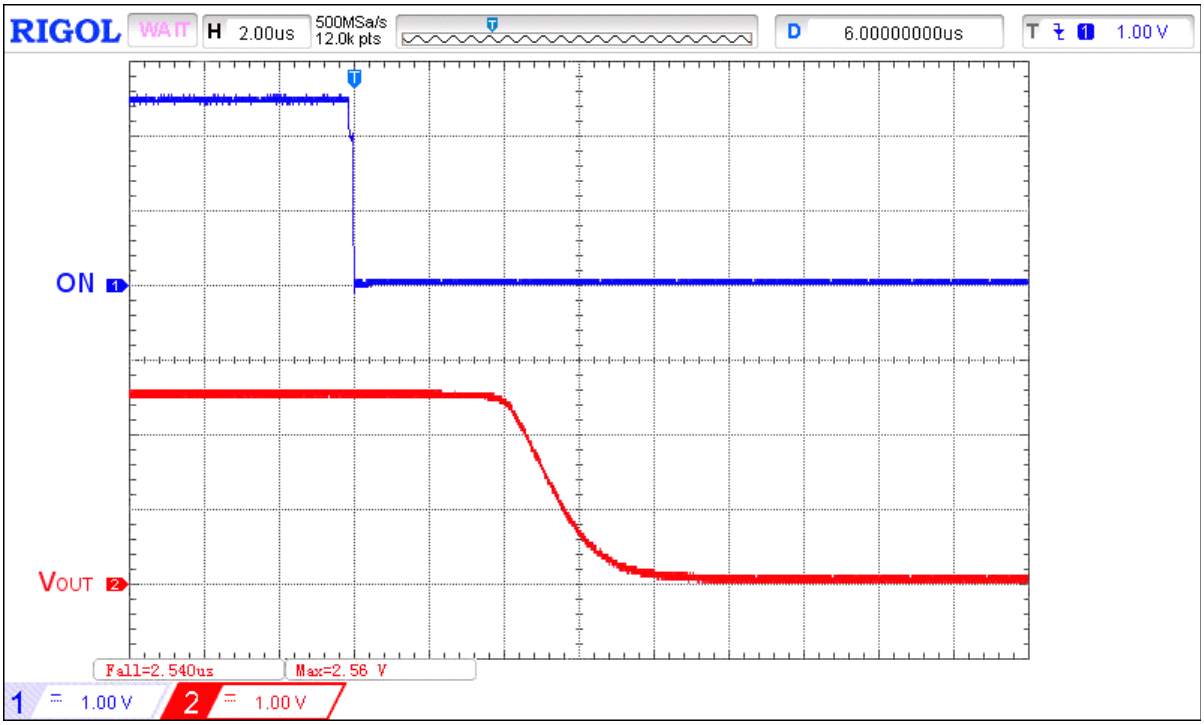


Figure 5. Typical Turn OFF operation waveform for V_{IN} = 2.5 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω

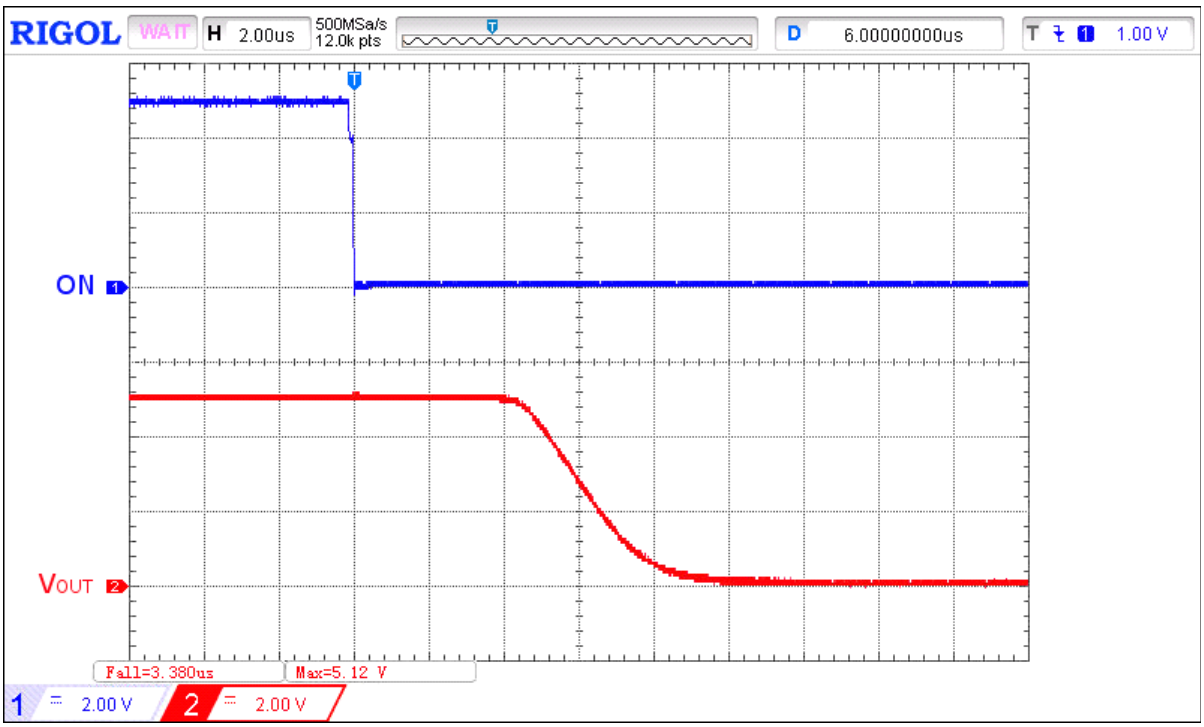


Figure 6. Typical Turn OFF operation waveform for V_{IN} = 5 V, C_{LOAD} = 0.1 µF, R_{LOAD} = 10 Ω

V_{IN} Inrush Current Details

When the SLG59M1748C is enabled with ON ↑, the power switch closes to charge the V_{OUT} output capacitor to V_{IN}. The charging current drawn from V_{IN} is commonly referred to as "V_{IN} inrush current" and can cause the input power source to collapse if the V_{IN} inrush current is too high during the V_{OUT} slew time.

Since the V_{OUT} rise time of the SLG59M1748C is fixed, V_{IN} inrush current is then a function of the output capacitance at VOUT. The expression relating V_{IN} inrush current, the SLG59M1748C V_{OUT} rise time, and C_{LOAD} is:

$$V_{IN}\ \text{Inrush Current} = C_{LOAD} \times \frac{\Delta V_{OUT}\,(10\%\ \text{to}\ 90\%)}{T_{VOUT(R)}\,(10\%\ \text{to}\ 90\%)}$$

where in this expression ΔV_{OUT} is equivalent to V_{IN} if the initial SLG59M1748C's output voltages are zero.

In the table below are examples of V_{IN} inrush currents assuming zero initial charge on C_{LOAD} as a function of V_{IN}.

V_{IN}	$T_{VOUT(R)}$	C_{LOAD}	Inrush Current
2.5 V	0.76 ms	100 µF	0.26 A
5 V	1.2 ms	100 µF	0.33 A

Since the relationship is linear and if C_{LOAD} were increased to 250 µF, then V_{IN} inrush currents would be 2.5x higher in either example. Since the V_{OUT} slew time is fixed, an upper limit for C_{LOAD} should be set by the SLG59M1748C's continuous I_{DS}; e.g., 2.2 A for 5 V applications and 1.2 A for 1.6 V applications.

If a large C_{LOAD} capacitor is required in the application and depending upon the strength of the input power source, it may very well be necessary to increase the C_{IN}-to-C_{LOAD} ratio to minimize V_{IN} droop during turn-on.

For other V_{OUT} rise time options, please contact Dialog for additional information.

Power Dissipation Considerations

The junction temperature of the SLG59M1748C depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON} generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1748C is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = RDS_{ON} \times I_{DS}^2$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

RDS_{ON}= Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

Power Dissipation Considerations (continued)

In nominal operating mode, the SLG59M1748C's power dissipation can also be calculated by taking into account the voltage drop across the switch (V_{IN} - V_{OUT}) and the magnitude of the switch's output current (I_{DS}):

$$PD_{TOTAL} = (V_{IN} - V_{OUT}) \times I_{DS} \text{ or}$$

$$PD_{TOTAL} = (V_{IN} – (R_{LOAD} \times I_{DS})) \times I_{DS}$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

V_{IN} = Switch input Voltage, in Volts (V)

R_{LOAD} = Output Load Resistance, in Ohms (Ω)

I_{DS} = Switch output current, in Amps (A)

V_{OUT} = Switch output voltage, or $R_{LOAD} \times I_{DS}$

Multiplexing Two Power Sources to a Common Output

As mentioned in the General Description section on Page 1, the SLG59M1748C can be used in applications for multiplexing two power rails to a common output. A pair of SLG59M1748Cs is necessary for this application and the circuit is illustrated on Figure 7. In this application, a 5 V power rail is connected to VIN1 and 3.3 V power rail is connected to VIN2.

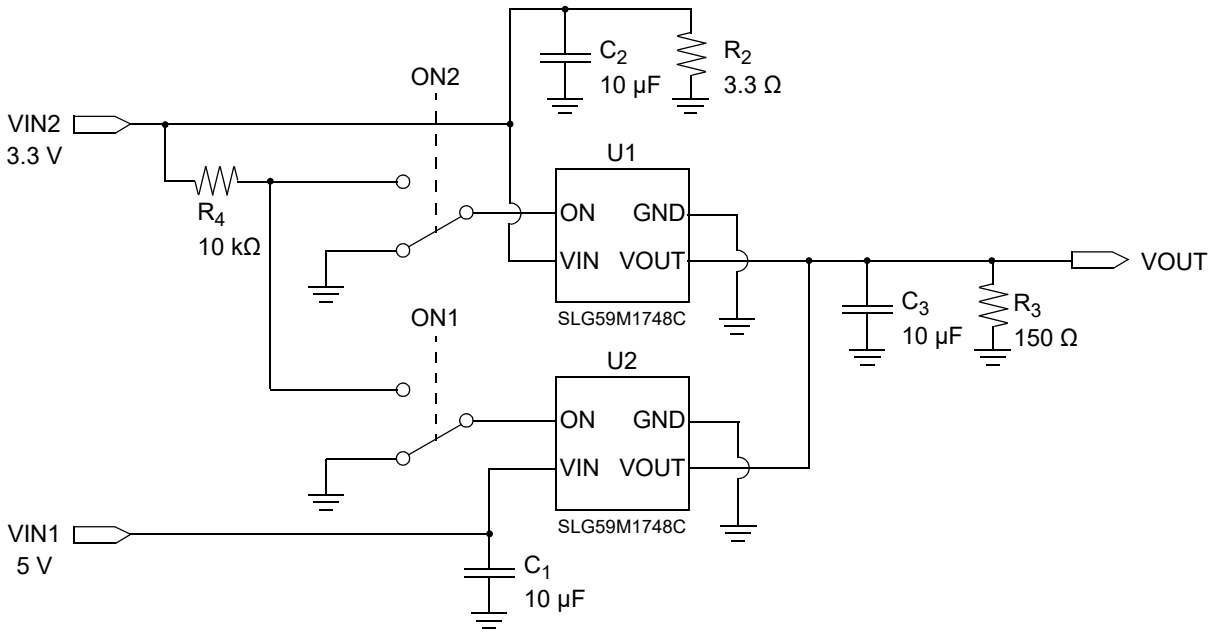


Figure 7. A typical application schematic where a pair of SLG59M1748Cs is used to multiplex two power rails to a common output

By toggling ON1 and ON2 High → Low → High, it is possible to switch between VIN1 and VIN2 power rails with minimal crossover transients.

In the case where VIN1 (the higher of the two power rails) is already turned ON and the output is to be switched to VIN2 (the lower power rail), it is necessary to toggle ON1 Low after ON2 is toggled High, otherwise, the circuit's VOUT will still be locked to VIN1. To minimize 5 V → 3.3 V → 5 V switchover transients, ON1 can be toggled Low or High while ON2 is always High. To reduce the voltage drop during a 5 V to 3.3 V switchover, it is recommended to use a larger load capacitance (C_3) or a larger load resistance (R_3). For more details of this application's operation with additional waveforms, please consult AN-1096.

Layout Guidelines:

1. Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 8, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59M1748C's VIN and VOUT pins;

3. The GND pin should be connected to system analog or power ground plane.

SLG59M1748C Evaluation Board:

A GFET3 Evaluation Board for SLG59M1748C is designed according to the statements above and is illustrated on Figure 8. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

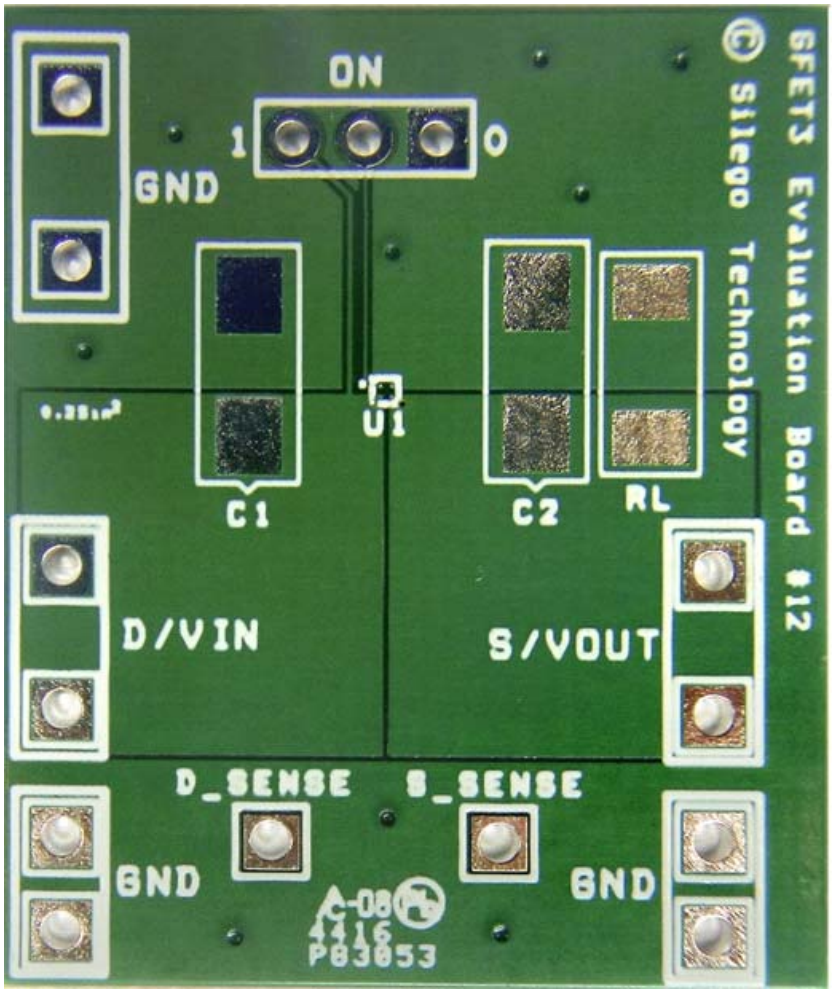


Figure 8. SLG59M1748C Evaluation Board

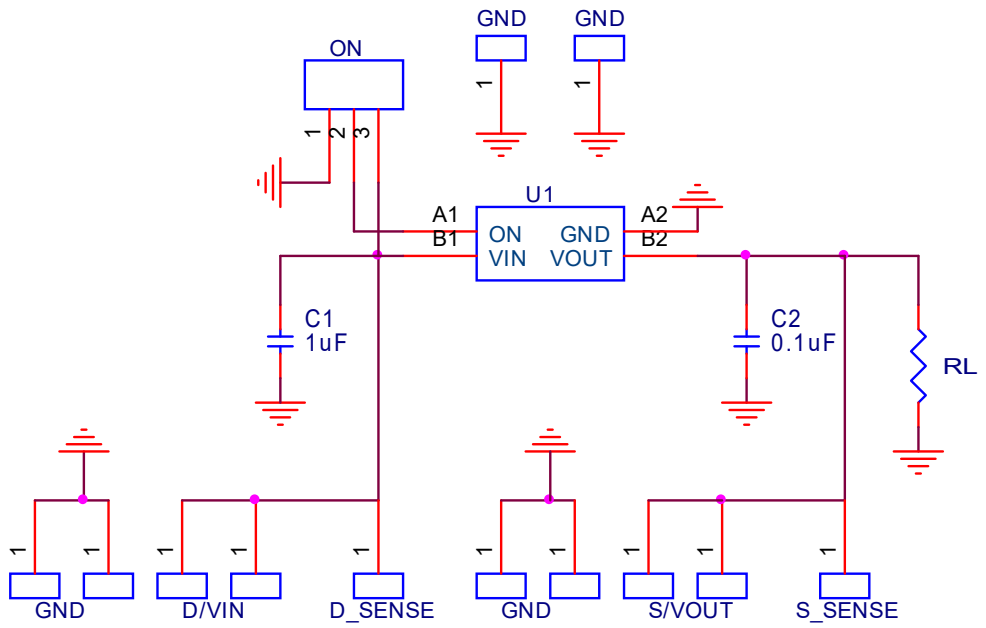


Figure 9. SLG59M1748C Evaluation Board Connection Circuit

Basic Test Setup and Connections

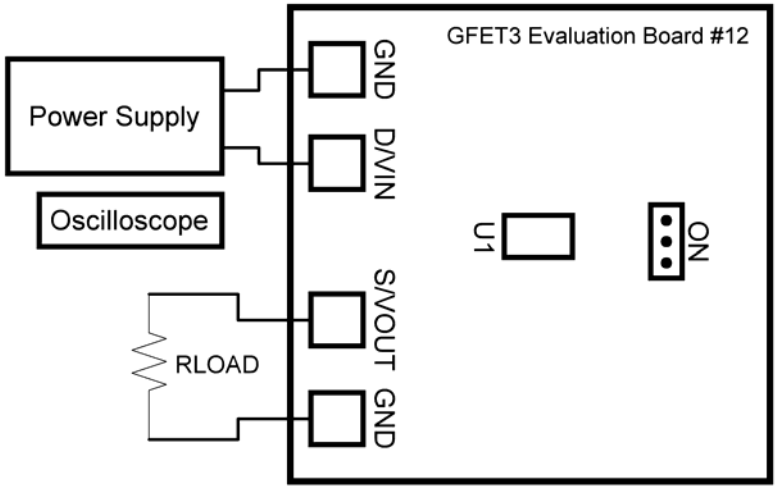


Figure 10. SLG59M1748C Evaluation Board Connection Circuit

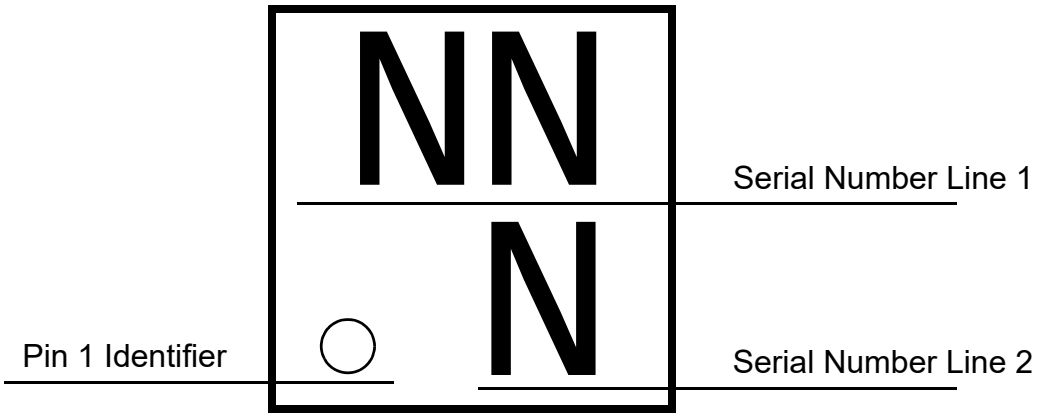
EVB Configuration

1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;

2. Turn on Power Supply and set desired V_{IN} from 1.6 V…5 V range;

3. Toggle the ON signal High or Low to observe SLG59M1748C operation.

Package Top Marking System Definition



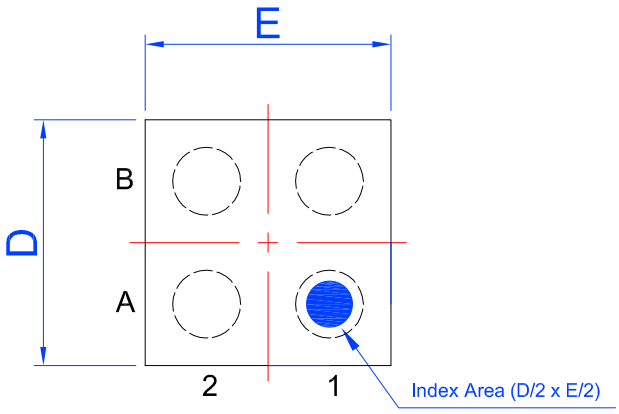
NN - Part Serial Number Field Line 1
where each “N” character can be A-Z and 0-9

N - Part Serial Number Field Line 2
where each “N” character can be A-Z and 0-9

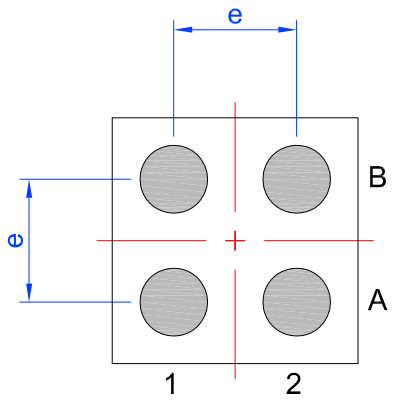
Package Drawing and Dimensions

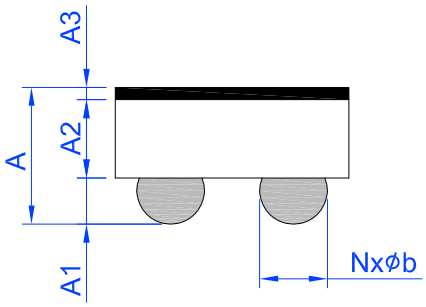
4 Pin WLCSP Green Package 0.8 x 0.8 mm

Laser Marking View



Bump View





SIDE View

TERMINALS ASSIGNMENTS		
B	VIN	VOUT
A	ON	GND
	1	2

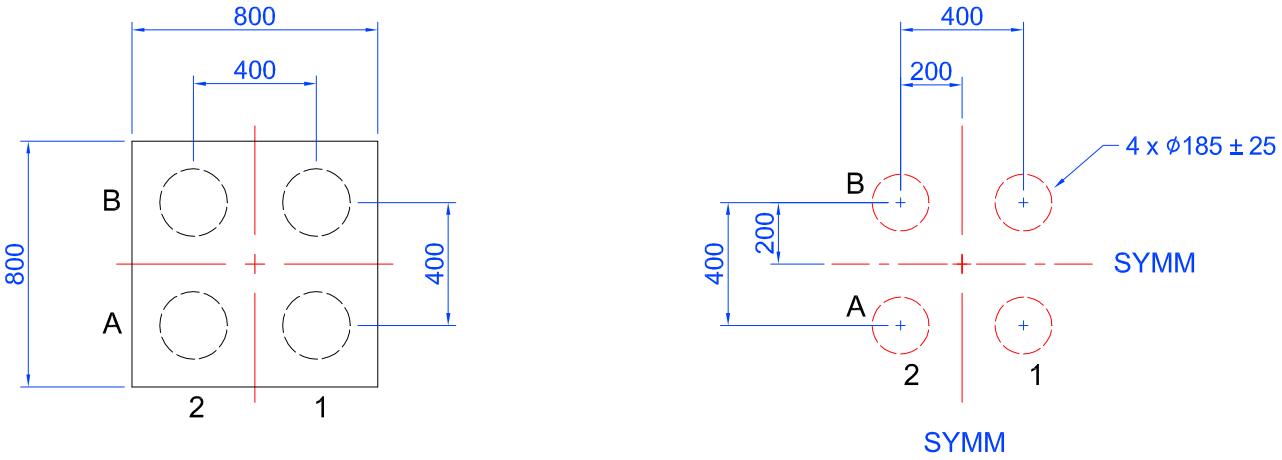
Unit: mm

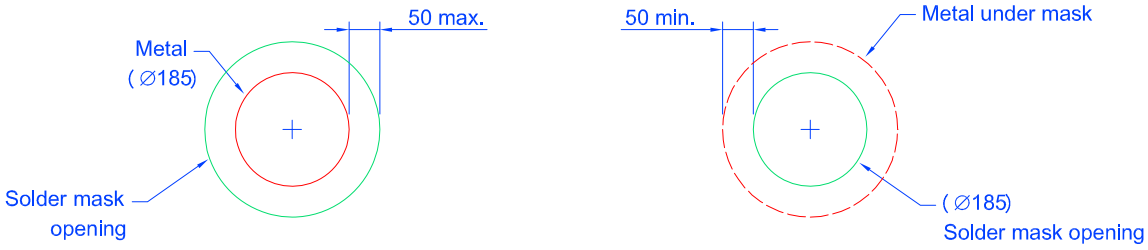
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.380	-	0.500	D	0.77	0.80	0.83
A1	0.125	0.150	0.175	E	0.77	0.80	0.83
A2	0.240	0.265	0.290	e	0.40 BSC		
A3	0.015	0.025	0.035	N	4 (Bump)		
b	0.195	0.220	0.245				

SLG59M1748C 4 Pin WLCSP PCB Landing Pattern

Exposed Bump
(Laser marking view)

Recommended
Land Pattern



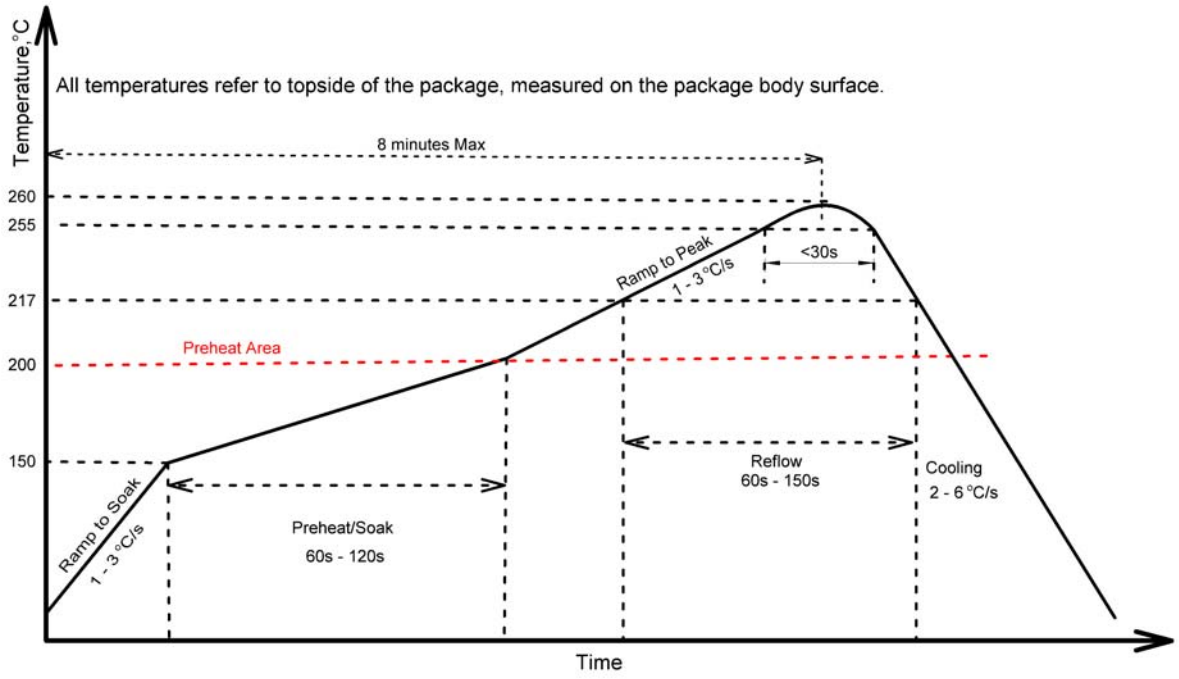


Solder mask detail (not to scale)

Unit: um

Recommended Reflow Soldering Profile

For successful reflow of the SLG59M1748C a recommended thermal profile is illustrated below:



Note: This reflow profile is for classification/preconditioning and are not meant to specify board assembly profile. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed parameters depicted on figure above.

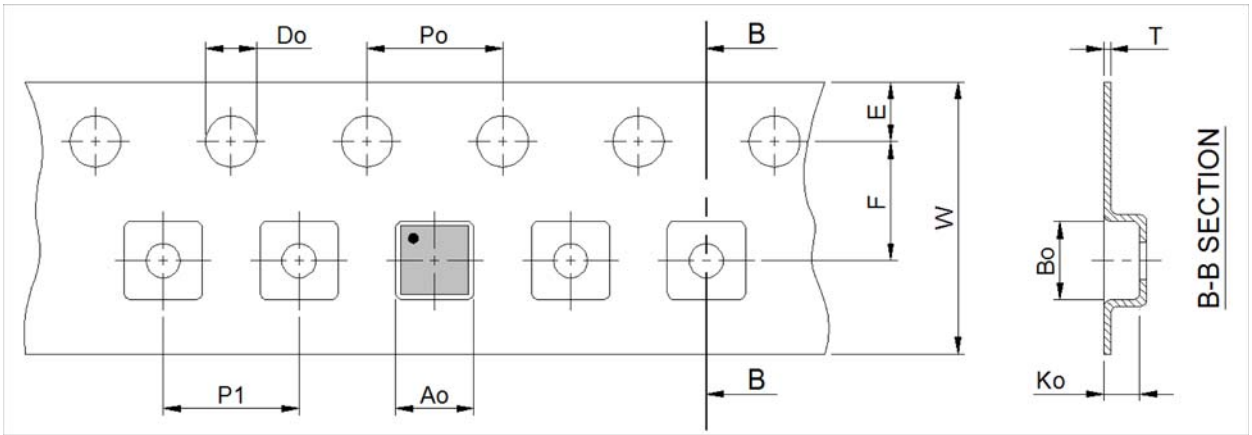
Please see more information on IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.352 mm^3 (nominal).

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
WLCSP 4L 0.8 x 0.8 mm 0.4P Green	4	0.8 x 0.8 x 0.44	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width	Tape Thickness
	A0	B0	K0	P0	P1	D0	E	F	W	T
WLCSP 4L 0.8 x 0.8 mm 0.4P Green	0.87	0.87	0.56	4	4	1.5	1.75	3.5	8	0.2



Note: 1.Orientation in carrier: Pin1 is at upper left corner (Quadrant 1). **Refer to EIA-481 specification**

Revision History

Date	Version	Change
12/10/2018	1.03	Updated style and formatting Added Layout Guidelines
7/24/2017	1.02	Updated Tape and Reel Specification
5/17/2017	1.01	Added Application Information
4/17/2017	1.00	Production Release