SLG5NT1611V

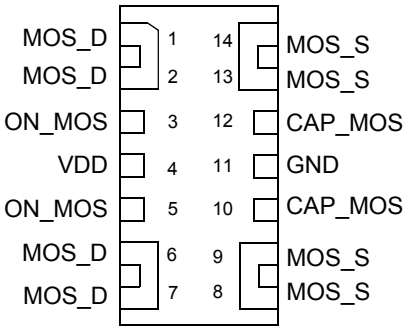
An Ultra-small 7.8 mΩ, 9 A, Single-channel Integrated Power Switch with Reverse-current Blocking

General Description

The SLG5NT1611V is a high-performance 7.8 mΩ NMOS power switch designed for all 0.85 V to 5.5V power rail applications up to 9 A. Incorporating reverse-current blocking, the SLG5NT1611V is uniquely suited for those power rail applications where output-to-input voltage backfeed conditions are to be avoided. Using a proprietary MOSFET design, the SLG5NT1611V achieves a stable 7.8 mΩ RDSON across its applied supply voltage range and over temperature. Using Silego's proprietary CuFET technology, the SLG5NT1611V package also exhibits low thermal resistance for high-current operation.

Fully specified over the -40 °C to 85 °C temperature range, the SLG5NT1611V is packaged in a space-efficient, low thermal resistance, RoHS-compliant 1.0 mm x 3.0 mm STDFN package.

Pin Configuration

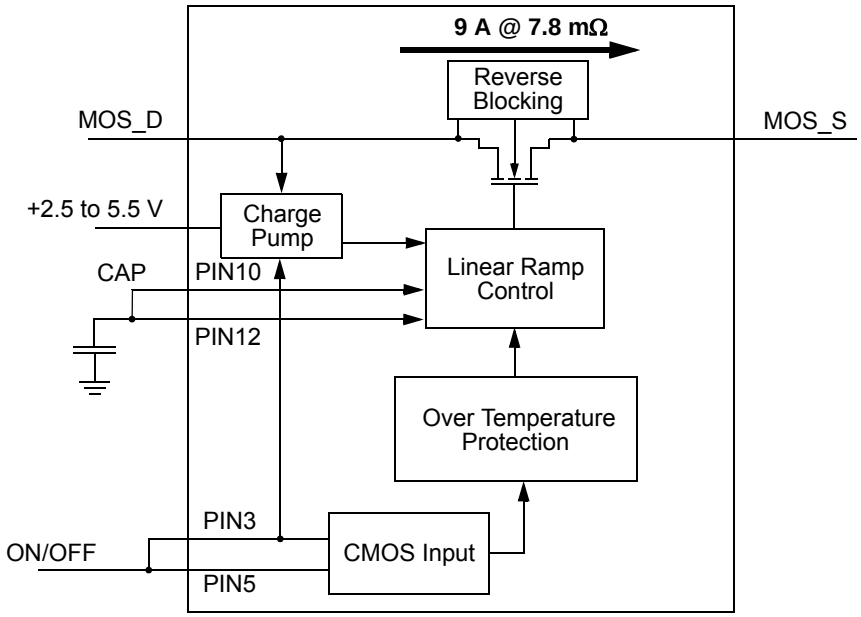


14-pin STDFN
(Top View)

Features

- High-performance MOSFET Switch Design
  - Low Typical RDSON: 7.8 mΩ
- Steady-state Operating Current: Up to 9 A
- FET Bulk-switch Reverse-current Blocking
- Supply Voltage: 2.5 V ≤ VDD ≤ 5.5 V
- Wide Supply/Input Voltage Range: 0.85 V ≤ VIN ≤ VDD
- Capacitor-programmable Start-up and Inrush Current Control
- Internal MOSFET Gate Drive
- Thermal Shutdown Protection
- Operating Temperature: -40 °C to 85 °C
- Low θJA, 14-pin 1.0 mm x 3.0 mm STDFN Packaging
  - Pb-Free / Halogen-Free / RoHS complian

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1, 2, 6, 7	MOS_D	MOSFET	Drain terminal connections of the n-channel MOSFET. Connect a low-ESR 10-µF (or larger) capacitor from the MOS_D pins (Pins 1, 2, 6, and 7) to ground. Capacitors used at MOS_D should be rated at 10 V or higher.
3,5	ON_MOS	Input	A low-to-high transition on these pins initiates the operation of the SLG5NT1611V's state machine. ON_MOS is an asserted HIGH, level-sensitive CMOS input with VIL < 0.3 V and VIH > 0.85 V. While there is an internal pull-down circuit to GND (~4MΩ), connect these pins directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow these pins to be open-circuited.
4	VDD	VDD	With an internal 1.5 V UVLO threshold, VDD supplies the power for the operation of the power switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1 µF (or larger) capacitor.
8, 9, 13, 14	MOS_S	MOSFET	Source terminal connections of the n-channel MOSFET. Connect a low-ESR 10-µF (up to CAP_{SOURCE}) capacitor from the MOS_S pins (Pins 8, 9, 13, and 14) to ground. Capacitors used at MOS_S should be rated at 10 V or higher.
10, 12	CAP_MOS	Input	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from the CAP_MOS pins (Pins 10 & 12) to GND sets the MOS_S slew rate and overall turn-on time of the SLG5NT1611V. For additional information, please consult the CAP_MOS typical performance characteristics on Page 5. Capacitors used at CAP_MOS should be rated at 10 V or higher.
11	GND	GND	Ground connection. Connect this pin to the system's analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG5NT1611V	STDFN 14L	Industrial, -40 °C to 85 °C
SLG5NT1611VTR	STDFN 14L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_D	Power Supply		--	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	1mm x 3mm 14L STDFN; Determined using 1 in^2, 1.2 oz. copper pads under VIN and VOUT on FR4 pcb material	--	71	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	1.2	W
IDS_{MAX}	Max Operating Current				9	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 10 continuous seconds out of every 100 seconds	--	--	12	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage		2.5	--	5.5	V
I_{DD}	Power Supply Current when OFF		--	0.1	1	µA
	Power Supply Current, ON_MOS_1 & ON_MOS_2 (Steady State)		--	50	100	µA
RDS_{ON}	ON Resistance	T_A 25°C MOSFET @100 mA	--	7.8	10.5	mΩ
		T_A 70°C MOSFET @100 mA	--	9.0	12.1	mΩ
		T_A 85°C MOSFET @100 mA		8.4	12.7	mΩ
MOSFET IDS	Current from Drain to Source for each MOSFET	Continuous	--	--	9	A
IDS_{LKG}	IDS Leakage (Reverse Blocking enabled)	V_S = 1.0 V to 5.0 V, V_{DD} = V_D = 0 V, ON_MOS = LOW, Full temp range	--	0.5	5.0	µA
V_D	Drain Voltage		0.85	5.0	V_{DD}	V
T_{ON_Delay}	ON pin Delay Time	50% ON to Ramp Begin, R_L = 20 Ω, no C_L	--	270	500	µs
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_S	Configurable [1]			ms
		Example: CAP (Pin 10 & 12) share a single 4nF capacitor, V_{DD} = V_D = 5 V, Source_Cap = 10 µF, R_L = 20 Ω	--	1.1	--	ms
$T_{SLEWRATE}$	Slew Rate	10% V_S to 90% V_S	Configurable [1]			V/ms
		Example: CAP (Pin 10 & 12) share a single 4nF capacitor, V_{DD} = V_D = 5 V, Source_Cap = 10 µF, R_L = 20 Ω	--	6.0	--	V/ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S Fall, V_{DD} = V_D = 5 V, R_L = 20 Ω, no C_L	--	1.7	3	µs
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V

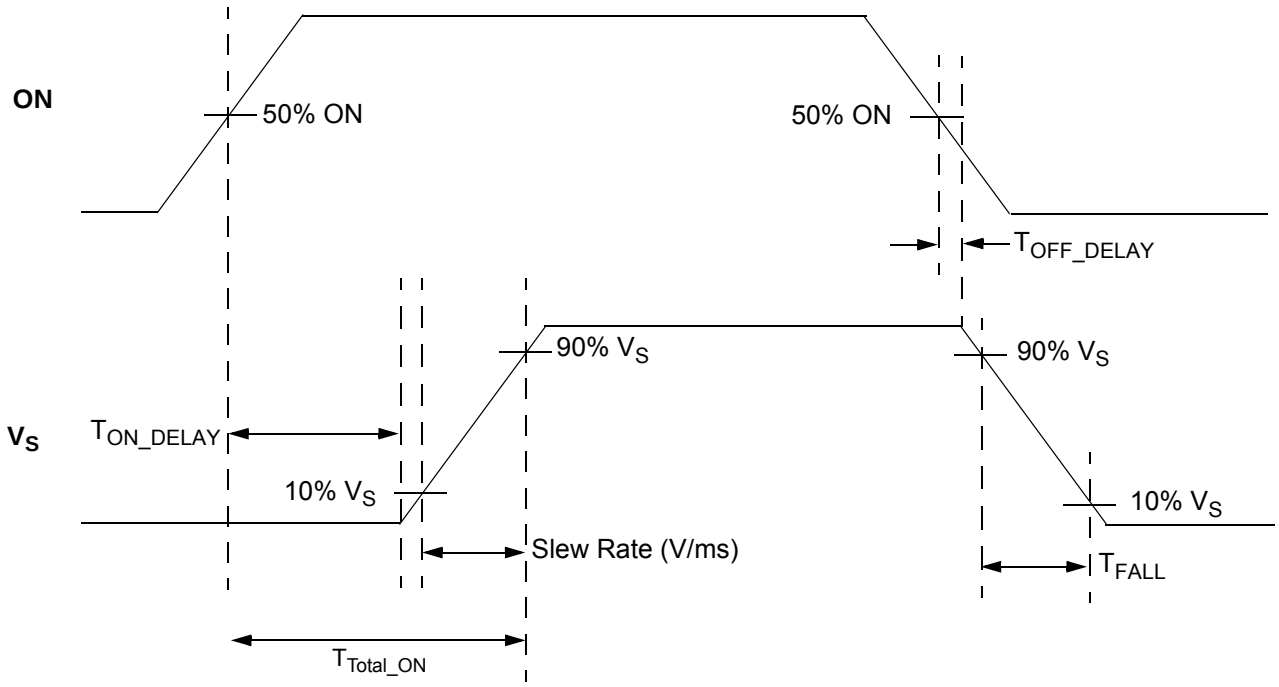
Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated)

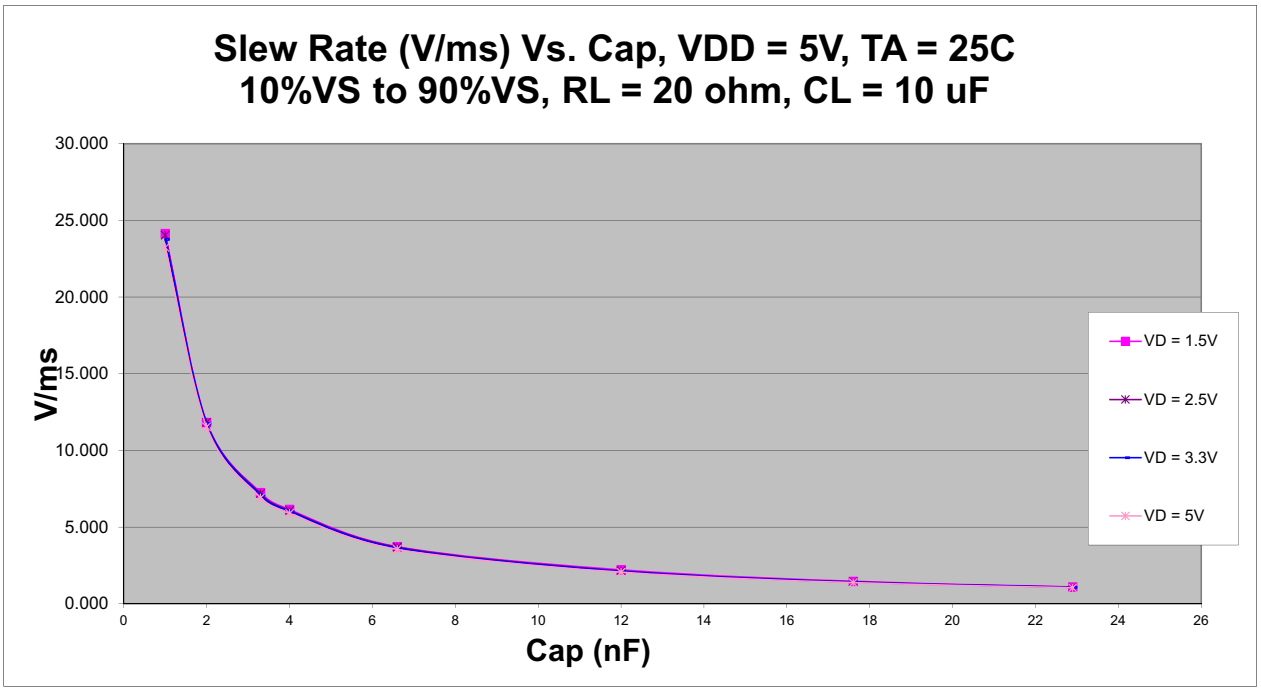
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
CAP_{SOURCE}	Source Cap	Source to GND	--	--	1000	µF
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	125	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	100	--	°C
$THERM_{TIME}$	Thermal shutoff time		--	--	1	ms

Notes:
1. Refer to table for configuration details.

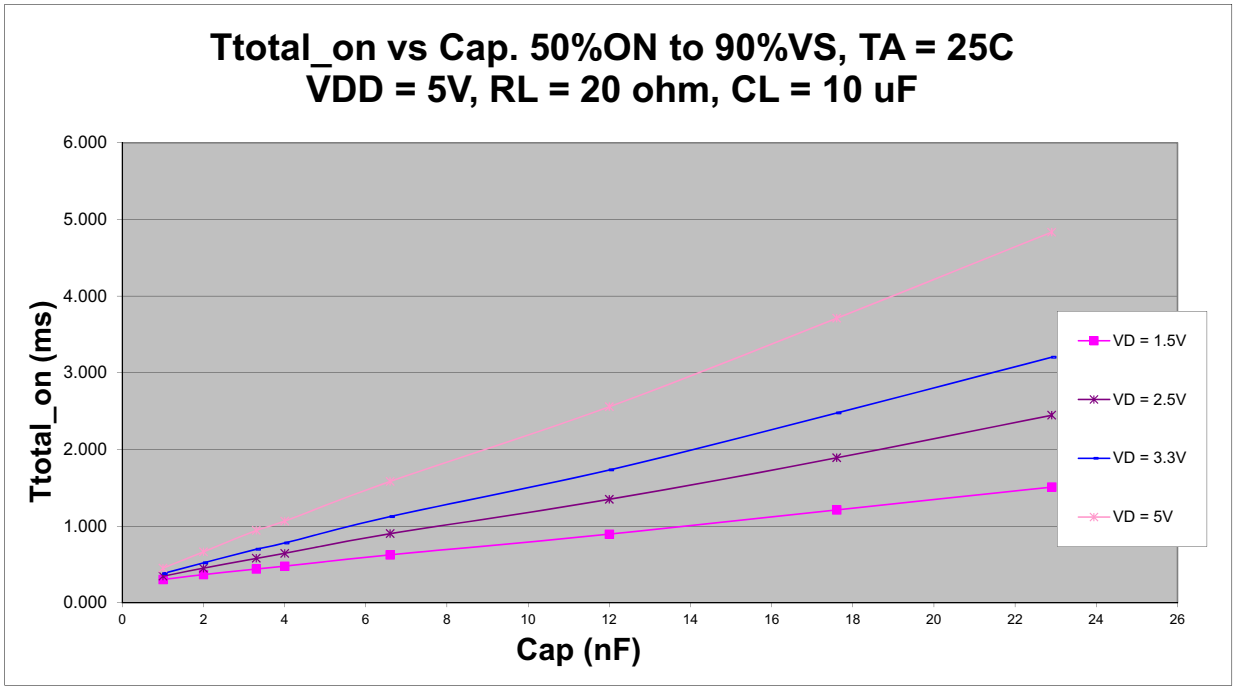
T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



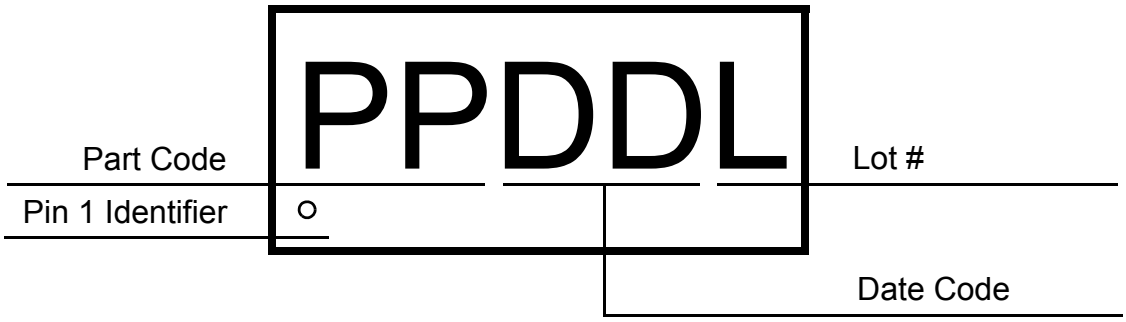
T_{SLEW} vs. CAP_MOS



T_{TOTAL_ON} vs. CAP_MOS

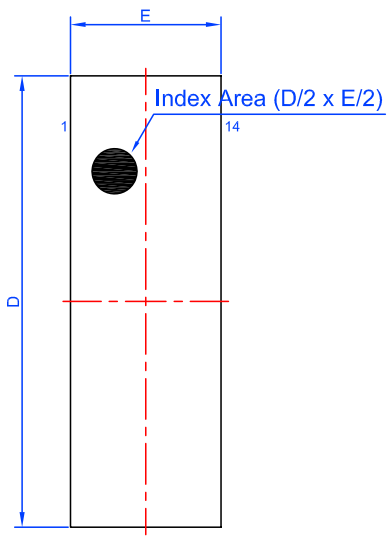


Package Top Marking System Definition

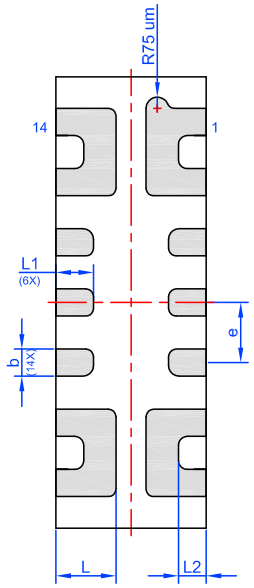


Package Drawing and Dimensions

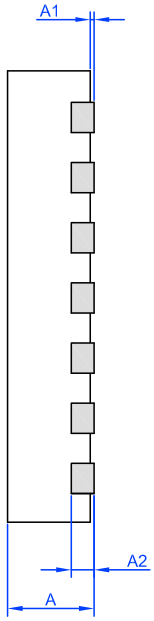
14 Lead STDFN Package 1 mm x 3 mm (Fused Lead)



Top View



BTM View

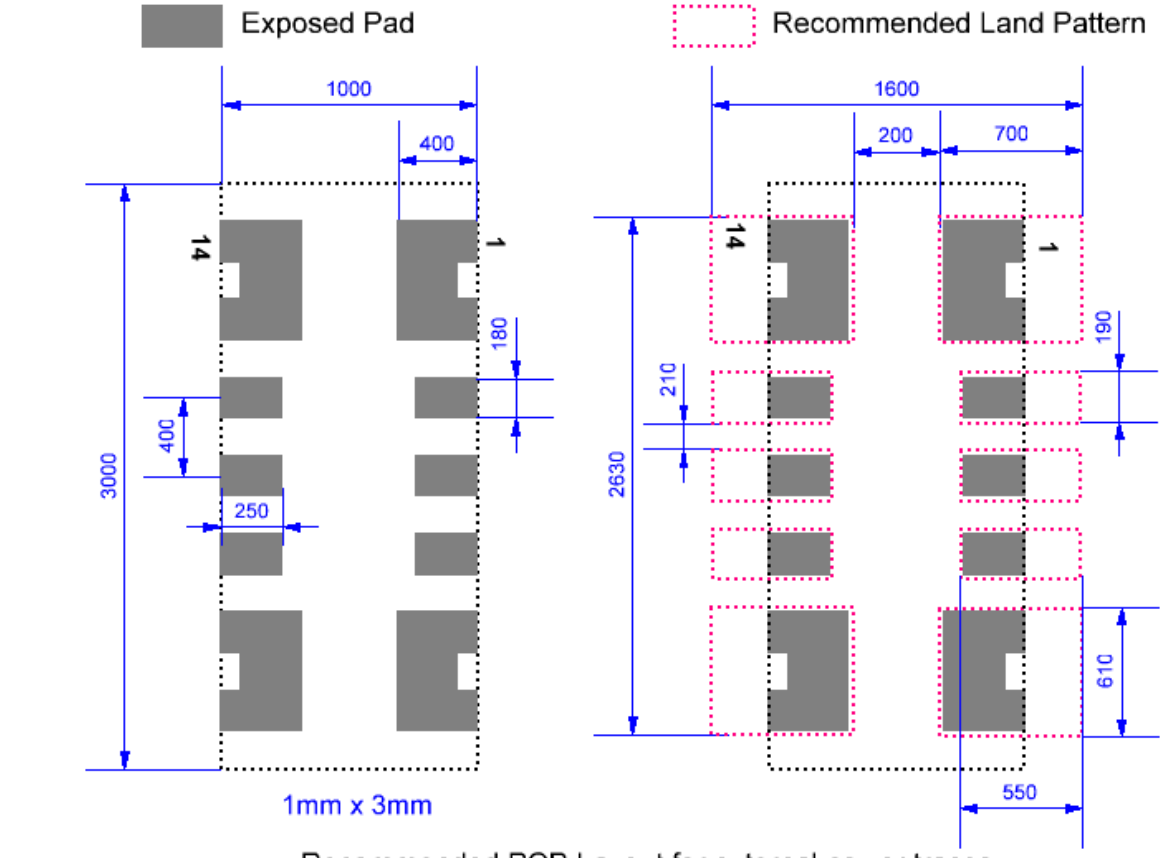


SIDE View

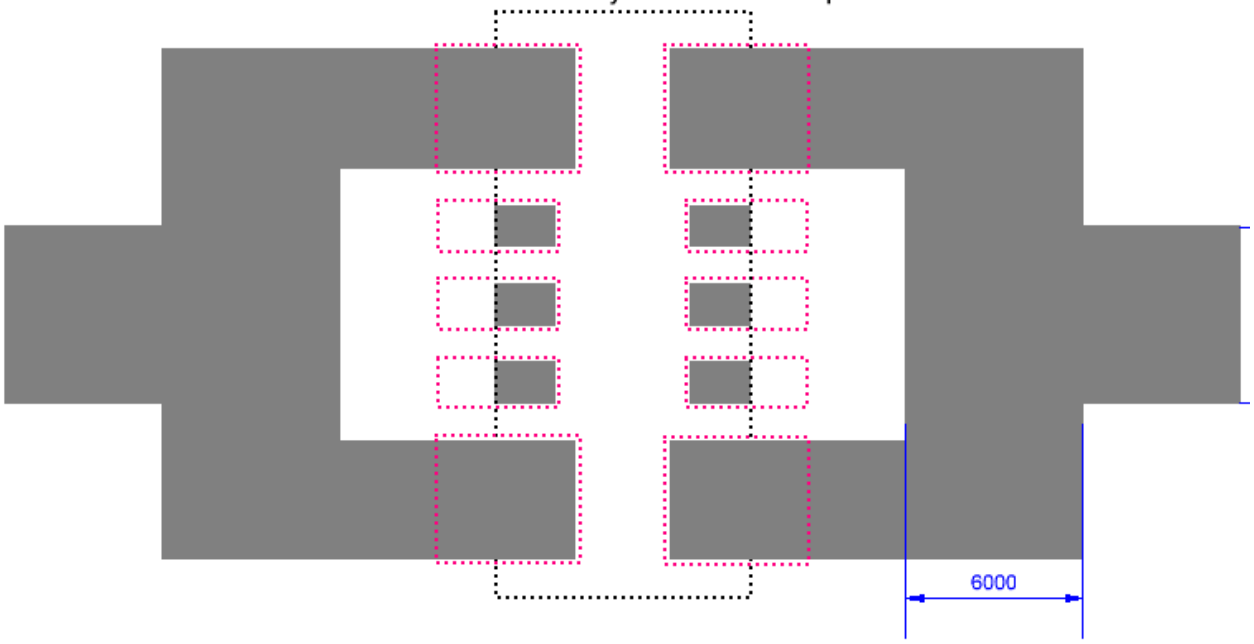
Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.20	0.25	0.30
e	0.40 BSC			L2	0.06	0.11	0.16

Recommended Land Pattern and PCB Layout



Recommended PCB Layout for external power traces



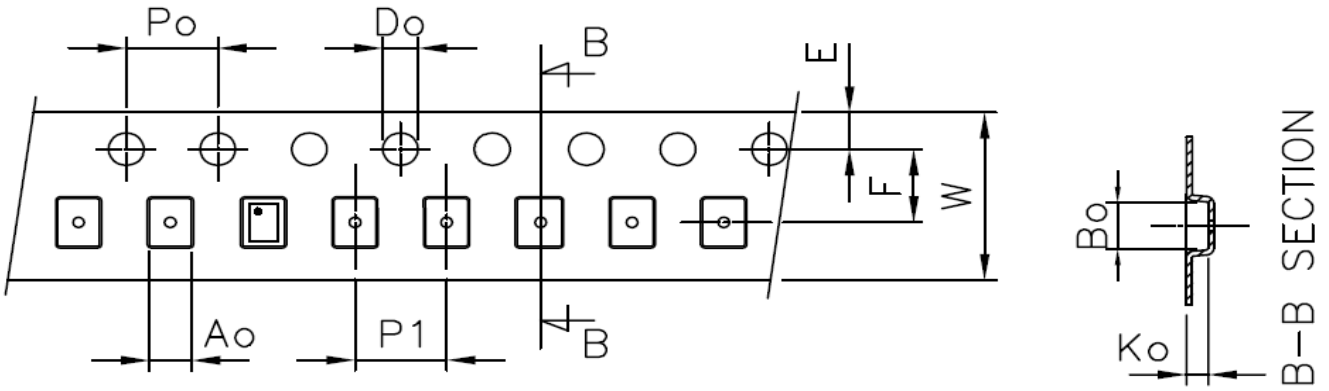
Note: All dimensions are in micrometers (μm)

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size	Units per Reel	Max Units per Box	Reel & Hub Size (mm)	Trailer A		Leader B		Pocket Tape (mm)	
						Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STDFN 14L 1x3mm 0.4P FC	14	1x3x0.55mm	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 14L 1x3mm 0.4P FC	1.15	3.15	0.7	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.65 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
1/20/2016	1.00	Updated IDD values Production release
1/14/2016	0.32	Updated Title, General Description, and Features Updated Pin Descriptions Updated text for clarity
12/10/2015	0.31	Updated Abs Max and Electrical Characteristics Tables
10/8/2015	0.30	Advanced Release