GreenFET™
Dual Power Source Gate Driver

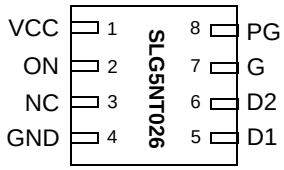
Features

- 12V Power supply
- Drain Voltage Range 1.0V to 20V
- Internal Gate Voltage Charge Pump
- Controlled Turn on Delay
- Controlled Turn on Slew Rate
- Pb-Free / RoHS Compliant
- Halogen-Free
- 2mm x 2mm TDFN-8 Package

Applications

- Power Rail Switches
- Hot Plugging Applications
- Soft Switching
- Personal computers and Servers
- Data Communications Equipment

Pin Configuration

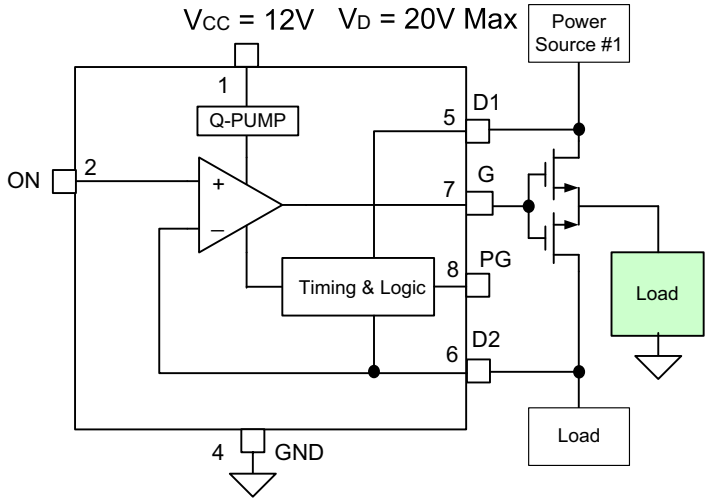


8-pin TDFN

Environmental

- Pb-Free / RoHS compliant
- Halogen Free

Block Diagram



SLG5NT026
For N-MOSFETS with 8V<V_{GS}< 16V

Pin Description

Pin #	Pin Name	Type	Pin Description
1	VCC	Power	Supply Voltage
2	ON	Input	CMOS Logic Level. High True
3	NC	--	No Connect.
4	GND	GND	Ground.
5	D1	Input	FET1 Drain Connection
6	D2	Input	FET2 Drain Connection
7	G	Output	FET Gate Drive
8	PG	Output	Output Open Drain - Power Good, indicates external FET fully on. Pull-up resistor greater than 300kΩ recommended.

Overview

The SLG5NT026 N-Channel FET Gate Driver is used for controlling a delayed turn on and ramping slew rate of the source voltage on N-Channel FET switches from a CMOS logic level input. Intended as a supporting control element for switched voltage rails in energy efficient, advanced power management systems, the SLG5NT026 also integrates circuits to discharge opened switched voltage rails. The gate driver is available in a variety of configurations supporting a range of turn-on slew rates from 0.80V/ms up to 4V/ms which, depending on load supplying source voltages in the range of 1.0V to 20V results in ramp times from 200µs to over 20ms(see Application Section). Delays until the ramp begins are source voltage independent and range from 250µs to 5ms. A power good condition is output to indicate that the ramp-up slew of the source voltage is finished. Additionally, an internal discharge circuit provides a controlled path to remove charge from open power rails. The SLG5NT026 gate drive is packaged in an 8 pin DFN package.

When used with external N-Channel FETs, the SLG5NT026 supports low transient, energy efficient switching of high current loads at source voltages ranging from 1.0V to 20V.

Ordering Information

Part Number	Type
SLG5NT026-xxxxxxV	TDFN-8
SLG5NT026-xxxxxxVTR	TDFN-8 - Tape and Reel (3k units)

Configuration Options

Code (xxxxxx)	Ramp Rate (V/ms)	Delay (ms)	Discharge (Ω)
200300	2.0	0.25	Open

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_D or V_S to GND	-0.3	40.0	V
Voltage at Logic Input pins	-0.3	6.5	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Operating temperature range	-55	125	°C
Junction temperature	--	150	°C
ESD Human Body Model	--	2000	V
ESD Machine Model	--	200	V

Electrical Characteristics (0°C to 70°C)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		11.5	12.0	12.5	V
T_{VCC_RAMP}	V_{CC} Ramp-up Rate	See Note 1	0.25	--	--	V/ms
I_q	Quiescent Current	V_G not ramping FET = ON	--	50	80	µA
		V_G not ramping FET = OFF	--	0.1	1	µA
V_D	FET Drain Voltage	SLG5NT026	1.0	--	21	V
V_{GS}	Gate-Source Voltage	SLG5NT026	8.0	11.5	16	V
C_G	FET Gate Capacitance		500	--	16000	pF
T_{DELAY}	Ramp Delay Range		--	0.25	0.325	ms
T_{SLEW}	FET Turn on Slew Rate	4.0V/ms config option	2.8	4.0	5.2	V/ms
		2.0V/ms config option	1.4	2.0	2.6	V/ms
$I_{DISCHARGE}$	Internal Discharge Resistor		--	Open	--	Ω
V_{IH}	HIGH-level input voltage	ON (200mV Hysteresis)	2.4	--	5.5	V
V_{IL}	LOW-level Input voltage	ON (200mV Hysteresis)	--	--	0.4	V
V_{OH}	HIGH-level output voltage	PG Open Drain	--	--	5.5	V
I_{OL_LOGIC}	Logic LOW level output	PG Sink Current (0.4V)	--	0.02	--	mA

Note 1: If T_{VCC_RAMP} > 5V/ms and ON is asserted, Gate charging will begin after 1ms.

Device Operation

In a typical application, de-asserting ON (low) turns off the external power N-FET. When ON is asserted (high), the device will not begin driving the gate of the external power FET unless the voltage at the drain of the device is at or above 0.8V (e.g. $V_D \geq 0.8$). Gate voltage is not applied to the gate of the external power N-FET after DLY_t then the gate source (Vgs) voltage is ramped up to 11.5V above the source voltage V_S at a slew rate determined by the internal slew rate control element internal to the SLG5NT026. Monotonic rise of Vs is maintained even as ID increases dramatically after the load device turn on threshold voltage is reached. After the source voltage has ramped up to its maximum steady state value, the Open Drain PG (Power Good) signal is asserted. PG may be used as the ON control of a second SLG5NT026 thereby providing power on sequence control of a number of switched power rails, or used in a 'wired and' with other PG signals to indicate all switched power rails are in a power good condition.

If the ON signal has been asserted prior to the application of VCC, the device will begin turning on the external power FET after VCC ramps up

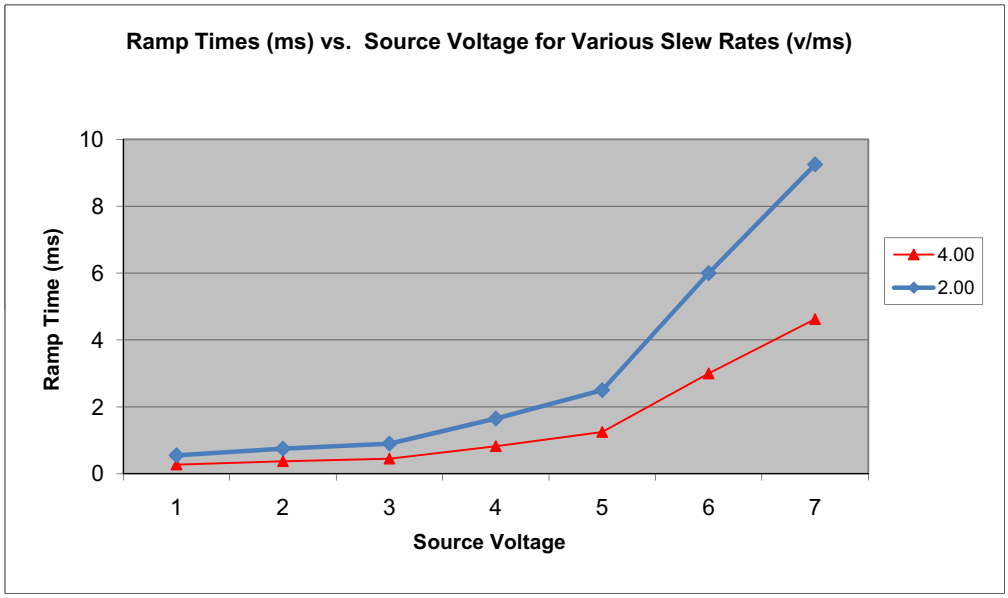
Delay Time and Slew Rates

The two components of controlling the application of FET source voltage to the load are a fixed time delay before beginning turn on of the FET (DLY_t below) and the Slew Time of the source voltage (Slew_t below). The Delay Time before gate voltage to the FET is applied and the corresponding delay is 250µs independent of FET drain voltage, source voltage or SLG5NT026 supply voltage.

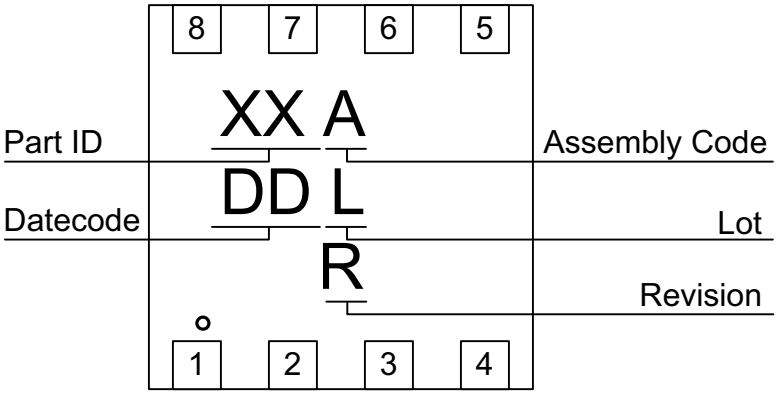
Having control over the Slew Rate of the FET's source voltage as the FET is turning on is important in controlling dv/dt caused transients. A power FET, for example, switching a 5V rail which has a total of 500µF of decoupling, fully on in 10µs will generate a 250A current surge which is very undesirable. If the FET turn on time can be stretched to 1ms, the current surge to charge the decoupling capacitors is reduced to 2.5A. The SLG5NT026 controls slew rate of a FET's source voltage as it is turned on. A range of slew rates are available as device order options. Obviously the time to fully slew the source voltage to fully on is a function of the drain supply voltage. The table and graph below shows source voltage ramp times for various slew rates supported by the SLG5NT026 for a range of specific source voltages.

Slew Rates (V/ms)	Ramp Times (ms) vs. Source Voltages (V)						
	1.1V	1.5V	1.8V	3.3V	5.0V	12V	18.5V
4.00	0.28	0.38	0.45	0.83	1.25	3.00	4.63
2.00	0.56	0.76	0.90	1.66	2.50	6.00	9.26

* The minimum time that ON can be de-asserted between switching cycles is 100µs.



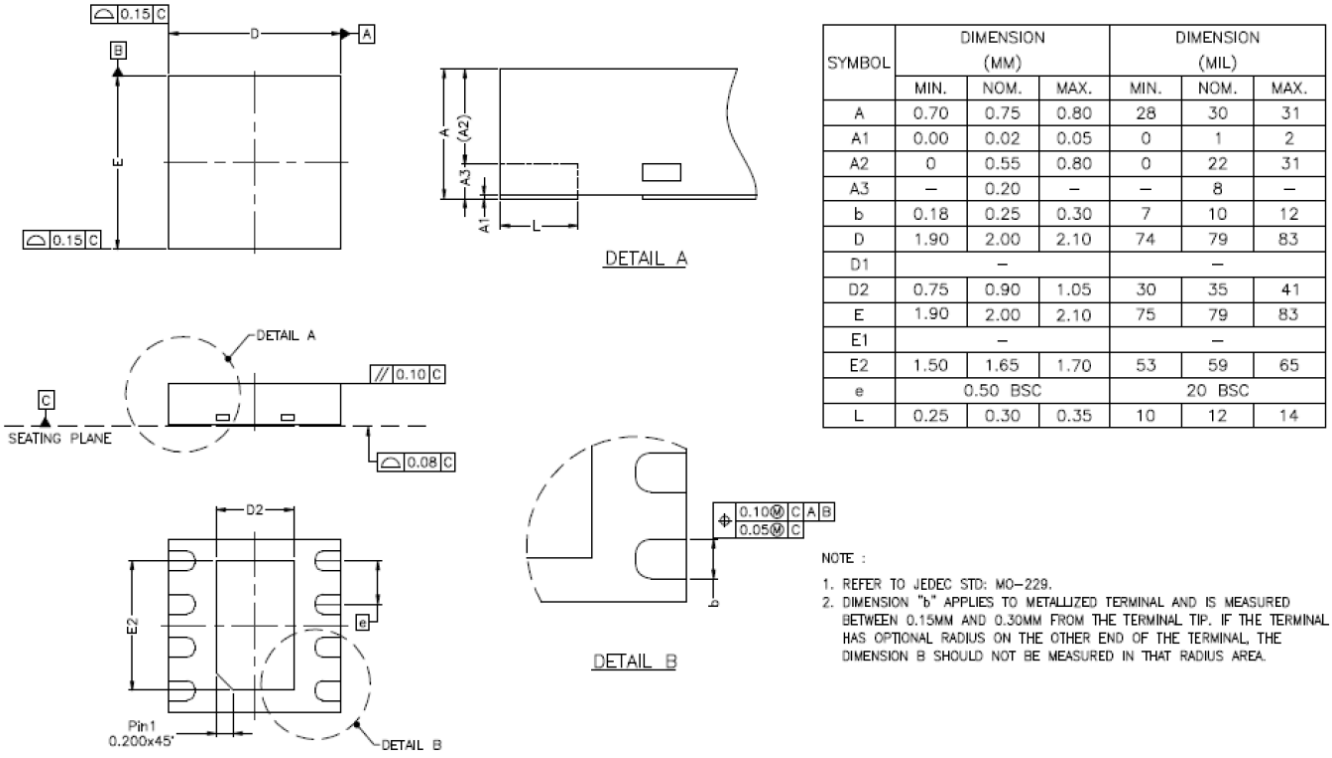
Package Top Marking System Definition



XX – Part ID Field: identifies the specific device configuration
A – Assembly Code Field: Assembly Location of the device.
DD – Date Code Field: Coded date of manufacture
L – Lot Code: Designates Lot #
R – Revision Code: Device Revision

Package Drawing and Dimensions

8 Lead TDFN Package



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	31
A1	0.00	0.02	0.05	0	1	2
A2	0	0.55	0.80	0	22	31
A3	–	0.20	–	–	8	–
b	0.18	0.25	0.30	7	10	12
D	1.90	2.00	2.10	74	79	83
D1		–			–	
D2	0.75	0.90	1.05	30	35	41
E	1.90	2.00	2.10	75	79	83
E1		–			–	
E2	1.50	1.65	1.70	53	59	65
e	0.50 BSC			20 BSC		
L	0.25	0.30	0.35	10	12	14

NOTE :

1. REFER TO JEDEC STD: MO–229.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
TDFN 8L Green	8	2 x 2 x 0.5	3,000	3,000	178 / 60	42	168	42	168	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index hole to Pocket center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8