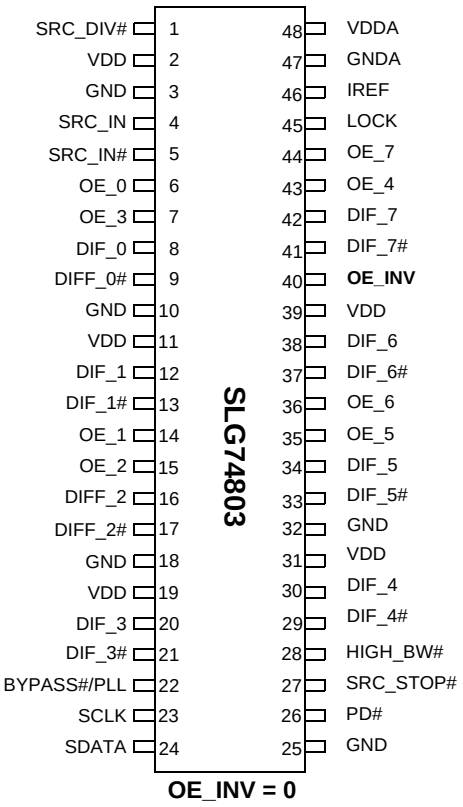
# SLG74803

## DB800 PCI Express Clock Buffer

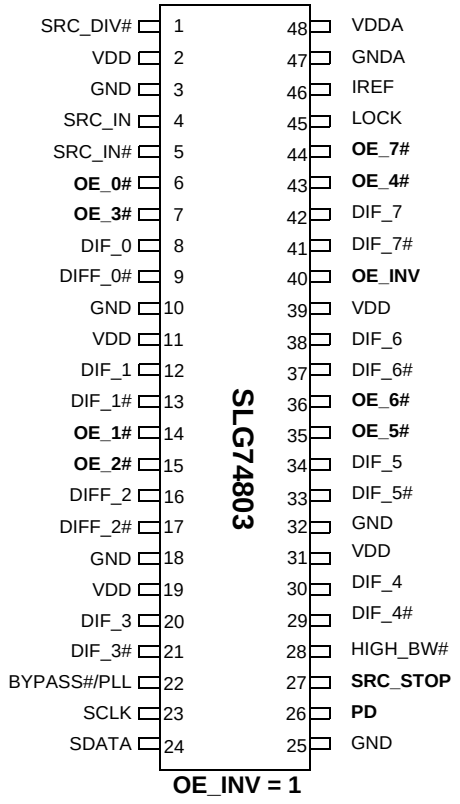
The SLG74803 is a member of Silego's PCI Express Clock Buffer Family.

**Recommended Application:**
PCI Express Gen1, Gen2, and Gen3 Reference Clock Buffer
**Output Features:**
• 8 - 0.7V current-mode differential output pairs
• Supports zero delay buffer mode and fanout mode
• Bandwidth programming available
**Key Specifications:**
• Outputs cycle-cycle jitter < 50ps
• Outputs skew: 50ps
• Phase jitter: PCIe Gen1 < 86ps peak to peak
• Phase jitter: PCIe Gen2 < 3.1ps rms
• Phase jitter: PCIe Gen3 < 1.0ps rms
**Features/Benefits:**
• Spread spectrum modulation tolerant, 0 to -0.5% down spread and +/- 0.25% center spread
• Supports undriven differential outputs in PD# and SRC_STOP# modes for power management.

### Pin Configuration




**OE_INV = 0**




**OE_INV = 1**

**48-pin SSOP & TSSOP**

## Pin Description for OE_INV = 0

| Pin # | Name | Type | Description |
|---|---|---|---|
| 1 | SRC_DIV# | IN | Active low Input for determining SRC output frequency SRC or SRC/2<br>0 = SRC/2, 1 = SRC |
| 2 | VDD | PWR | Power supply, nominal 3.3V |
| 3 | GND | PWR | Ground pin. |
| 4 | SRC_IN | IN | 0.7V Differential SRC TRUE input |
| 5 | SRC_IN# | IN | 0.7V Differential SRC COMPLEMENTARY input |
| 6 | OE_0 | IN | Active high input for enabling outputs.<br>0 = tri-state outputs, 1 = enable outputs |
| 7 | OE_3 | IN | Active high input for enabling outputs<br>0 = tri-state outputs, 1 = enable outputs |
| 8 | DIF_0 | OUT | 0.7V differential true clock outputs |
| 9 | DIF_0# | OUT | 0.7V differential complement clock outputs |
| 10 | GND | PWR | Ground pin |
| 11 | VDD | PWR | Power supply, nominal 3.3V |
| 12 | DIF_1 | OUT | 0.7V differential true clock outputs |
| 13 | DIF_1# | OUT | 0.7V differential complement clock outputs |
| 14 | OE_1 | IN | Active high input for enabling outputs.<br>0=tri-state outputs, 1=enable outputs |
| 15 | OE_2 | IN | Active high input for enabling outputs.<br>0=tri-state outputs, 1=enable outputs |
| 16 | DIF_2 | OUT | 0.7V differential true clock outputs |
| 17 | DIF_2# | OUT | 0.7V differential complement clock outputs |
| 18 | GND | PWR | Ground pin |
| 19 | VDD | PWR | Power supply, nominal 3.3V |
| 20 | DIF_3 | OUT | 0.7V differential true clock outputs |
| 21 | DIF_3# | OUT | 0.7V differential complement clock outputs |
| 22 | BYPASS#/PLL | IN | Input to select Bypass(fan-out) or PLL (ZDB) mode<br>0 = Bypass mode, 1 = PLL mode |
| 23 | SCLK | IN | Clock pin of SMBus circuitry 5V tolerant |
| 24 | SDATA | I/O | Data pin for SMBus circuitry 5V tolerant |
| 25 | GND | PWR | Ground pin |
| 26 | PD# | IN | Asynchronous active low input pin, with 120Kohm internal pull-up resistor, used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped |
| 27 | SRC_STOP | IN | Active low input to stop SRC outputs |
| 28 | HIGH_BW# | IN | 3.3V input for selecting PLL Band Width<br>0 = High, 1= Low |
| 29 | DIF_4# | OUT | 0.7V differential complement clock outputs |
| 30 | DIF_4 | OUT | 0.7V differential true clock outputs |
| 31 | VDD | PWR | Power supply, nominal 3.3V |

## Pin Description for OE_INV = 0 (continued)

| Pin # | Name | Type | Description |
|---|---|---|---|
| 32 | GND | PWR | Ground pin. |
| 33 | DIF_5# | OUT | 0.7V differential complement clock outputs |
| 34 | DIF_5 | OUT | 0.7V differential clock outputs |
| 35 | OE_5 | IN | Active high inputs for enabling outputs<br>0 = tri-state outputs, 1 = enable outputs |
| 36 | OE_6 | IN | Active high input for enabling outputs.<br>0 = tri-state outputs, 1 = enable outputs |
| 37 | DIF_6# | OUT | 0.7V differential complement clock outputs |
| 38 | DIF_6 | OUT | 0.7V differential true clock outputs |
| 39 | VDD | PWR | Power supply, nominal 3.3V |
| 40 | OE_INV | IN | This latched input slectes the polarity of the OE pins.<br>0 = OE pins active high, 1 = OE pins active low (OE#) |
| 41 | DIF_7# | OUT | 0.7V differential complement clock outputs |
| 42 | DIF_7 | OUT | 0.7V differential true clock outputs |
| 43 | OE_4 | IN | Active high input for enabling outputs.<br>0 = tri-state outputs, 1 = enable outputs |
| 44 | OE_7 | IN | Active high input for enabling outputs.<br>0 = tri-state outputs, 1 = enable outputs |
| 45 | LOCK | OUT | 3.3V output indicating PLL Lock Status. This pin goes high when lock is achieved |
| 46 | IREF | IN | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 47 | GNDA | PWR | Ground pin for the PLL core. |
| 48 | VDDA | PWR | 3.3V power for the PLL core. |

**Pin Description for OE_INV = 1**

| Pin # | Name | Type | Description |
|---|---|---|---|
| 1 | SRC_DIV# | IN | Active low Input for determining SRC output frequency SRC or SRC/2<br>0 = SRC/2, 1 = SRC |
| 2 | VDD | PWR | Power supply, nominal 3.3V |
| 3 | GND | PWR | Ground pin. |
| 4 | SRC_IN | IN | 0.7V Differential SRC TRUE input |
| 5 | SRC_IN# | IN | 0.7V Differential SRC COMPLEMENTARY input |
| 6 | OE_0# | IN | Active low input for enabling DIF pair 0<br>1 = tri-state outputs, 0 = enable outputs |
| 7 | OE_3# | IN | Active low input for enabling DIF pair 3<br>1 = tri-state outputs, 0 = enable outputs |
| 8 | DIF_0 | OUT | 0.7V differential true clock outputs |
| 9 | DIF_0# | OUT | 0.7V differential complement clock outputs |
| 10 | GND | PWR | Ground pin |
| 11 | VDD | PWR | Power supply, nominal 3.3V |
| 12 | DIF_1 | OUT | 0.7V differential true clock outputs |
| 13 | DIF_1# | OUT | 0.7V differential complement clock outputs |
| 14 | OE_1# | IN | Active low input for enabling DIF pair 1.<br>1=tri-state outputs, 0=enable outputs |
| 15 | OE_2# | IN | Active low input for enabling DIF pair 2.<br>1=tri-state outputs, 0=enable outputs |
| 16 | DIF_2 | OUT | 0.7V differential true clock outputs |
| 17 | DIF_2# | OUT | 0.7V differential complement clock outputs |
| 18 | GND | PWR | Ground pin |
| 19 | VDD | PWR | Power supply, nominal 3.3V |
| 20 | DIF_3 | OUT | 0.7V differential true clock outputs |
| 21 | DIF_3# | OUT | 0.7V differential complement clock outputs |
| 22 | BYPASS#/PLL | IN | Input to select Bypass(fan-out) or PLL (ZDB) mode<br>0 = Bypass mode, 1 = PLL mode |
| 23 | SCLK | IN | Clock pin of SMBus circuitry 5V tolerant |
| 24 | SDATA | I/O | Data pin for SMBus circuitry 5V tolerant |
| 25 | GND | PWR | Ground pin |
| 26 | PD | IN | Asynchronous active high input pin used to power down the device. The internal clocks are disabled and the VCO is stopped. |
| 27 | SRC_STOP | IN | Active high input to stop SRC outputs |
| 28 | HIGH_BW# | IN | 3.3V input for selecting PLL Bandwidth<br>0 = High, 1= Low |
| 29 | DIF_4# | OUT | 0.7V differential complement clock outputs |
| 30 | DIF_4 | OUT | 0.7V differential true clock outputs |
| 31 | VDD | PWR | Power supply, nominal 3.3V |
| 32 | GND | PWR | Ground pin. |
| 33 | DIF_5# | OUT | 0.7V differential complement clock outputs |
| 34 | DIF_5 | OUT | 0.7V differential clock outputs |
| 35 | OE_5# | IN | Active low input for enabling DIF pair 5.<br>1 = tri-state outputs, 0 = enable outputs |

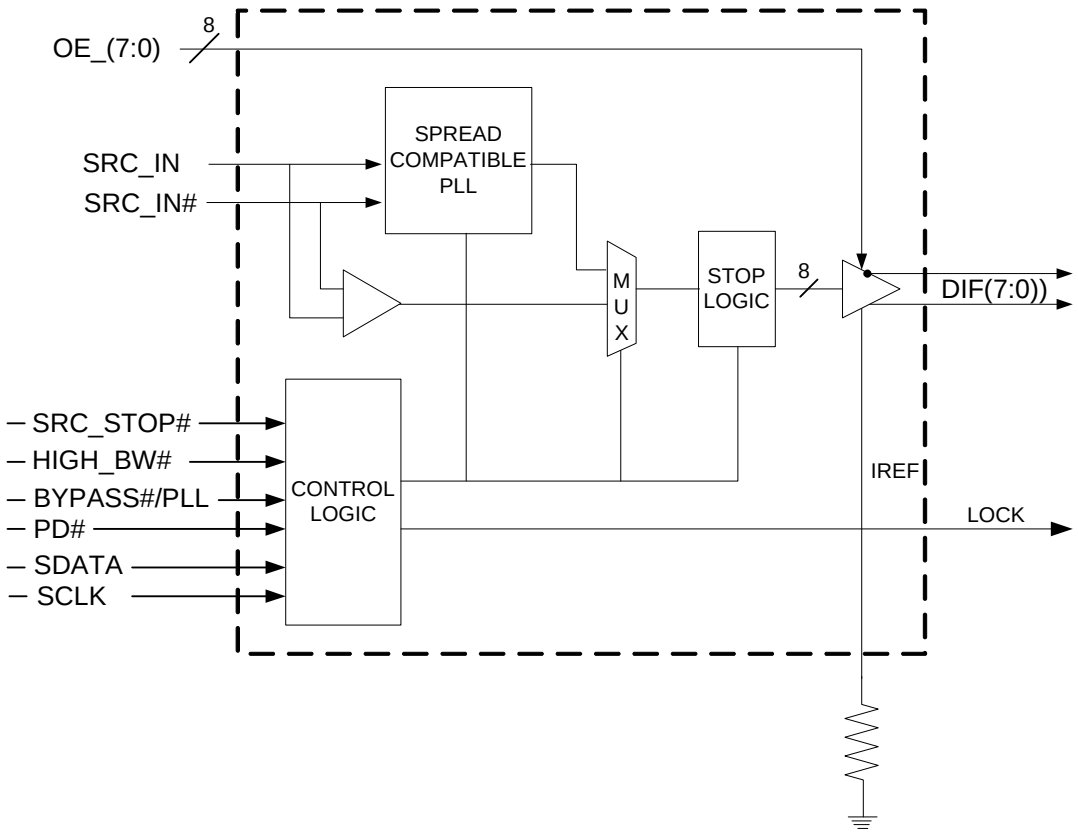
| Pin # | Name | Type | Description |
|---|---|---|---|
| 36 | OE_6# | IN | Active low input for enabling DIF pair 6.<br>1= tri-state outputs, 0= enable outputs |
| 37 | DIF_6# | OUT | 0.7V differential complement clock outputs |
| 38 | DIF_6 | OUT | 0.7V differential true clock outputs |
| 39 | VDD | PWR | Power supply, nominal 3.3V |
| 40 | OE_INV | IN | This latched input slectes the polarity of the OE pins.<br>0 = OE pins active high, 1 = OE pins active low (OE#) |
| 41 | DIF_7# | OUT | 0.7V differential complement clock outputs |
| 42 | DIF_7 | OUT | 0.7V differential true clock outputs |
| 43 | OE_4# | IN | Active low input for enabling DIF pair 4.<br>1= tri-state outputs, 0 = enable outputs |
| 44 | OE_7# | IN | Active low input for enabling DIF pair 7.<br>1= tri-state outputs, 0 = enable outputs |
| 45 | LOCK | OUT | 3.3V output indicating PLL Lock Status. This pin goes high when lock is achieved |
| 46 | IREF | IN | This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 47 | GNDA | PWR | Ground pin for the PLL core. |
| 48 | VDDA | PWR | 3.3V power for the PLL core. |

continued

## General Description

The SLG74803 follows the Intel DB800 Differential Buffer Specification v2.0. This buffer provides eight PCI-Express SRC clocks. The SLG74803 is driven by a differential input pair from a CK409/CK410 main clock generator. It provides outputs meeting tight cycle-to-cycle jitter (50ps) and output-to-output skew (50ps) requirements.

## Block Diagram




**Note:** Polarities shown for OE_INV = 0.

## Absolute Max

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| VDD_A | 3.3V Core Supply Voltage | | 4.6 | V |
| VDD_In | 3.3V Logic Supply Voltage | | 4.6 | V |
| $V_{IL}$ | Input Low Voltage | GND-0.5 | | V |
| $V_{IH}$ | Input High Voltage | | $V_{DD}$ +0.5V | V |
| $T_S$ | Storage Temperature | -65 | 150 | °C |
| Tambient | Ambient Operating Temp | 0 | 70 | °C |
| Tambient | Ambient Operating Temp (ordering option K) | 0 | 85 | °C |
| Tcase | Case Temperature | | 115 | °C |
| ESD protection | Input ESD protection human body model | 2000 | | V |

## Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A$ = 0 to (70°C or 85°C); Supply Voltage $V_{DD}$ = 3.3V +/-5%

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | 3.3 V +/-5% | 2 | | $V_{DD}$ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | 3.3V +/-5% | GND - 0.3 | | 0.8 | V | |
| Input High Current | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | -5 | | 5 | uA | |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0V; Inputs with no pull-up resistors | -5 | | | uA | |
| | $I_{IL2}$ | $V_{IN}$ = 0V; Inputs with pull-up resistors | -200 | | | uA | |
| Operating Supply Current | $I_{DD3,3OP}$ | Full Active, $C_L$ = Full load; | | | 200 | mA | |
| Powerdown Current | | All differential pairs driven | | | 70 | mA | |
| | $I_{DD3,3PD}$ | All differential pairs tri-stated | | | 4 | mA | |
| Input Frequency[3] | $F_i$ | $V_{DD}$ = 3.3V | 50 | | 110 | MHz | 3 |
| | $F_{iBYPASS}$ | Bypass Mode | 50 | | 400 | MHz | 1 |
| Pin Inductance[1] | $L_{pin}$ | | | | 7 | nH | 1 |
| Input Capacitance[1] | $C_{IN}$ | Logic Inputs | 1.5 | | 5 | pF | 1 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| PLL Bandwidth | BW | PLL Bandwidth when PLL_BW#=0 | 2 | 3 | | MHz | 1 |
| | | PLL Bandwidth when PLL_BW#=1 | 0.7 | 1 | 1.4 | MHz | 1 |
| CLK Stabilization[1,2] | $T_{STAB}$ | From $V_{DD}$ Power-Up and after input clock stabilization or deassertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| Modulation Frequency | | Triangular Modulation | 30 | | 33 | kHz | 1 |
| Tdrive_SRC_STOP# | | DIF output enable after SRC_Stop# de-assertion | | | 15 | ns | 1,3 |
| Tdrive_PD# | | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Tfall | | Fall time of PD# and SRC_STOP# | | | 5 | ns | 1 |
| Trise | | Rise time of PD# and SRC_STOP# | | | 5 | ns | 2 |

## Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

$T_A$ = 0 to (70°C or 85°C); $V_{DD}$ = 3.3V +/-5%, $C_L$ = 2pF, $R_S$ = 33.2Ω, $R_P$ = 49.9Ω, $I_{REF}$ = 475Ω

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| Current Source Output Impedance | $Z_O$[1] | $V_O = V_X$ | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal using oscilloscope math function. | 660 | | 850 | mV | 1,3 |
| Voltage Low | VLow | | -150 | | 150 | | 1,3 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | | 1 |
| Crossing Voltage (abs) | Vcross(abs) | | 250 | | 550 | mB | 1 |
| Crossing Voltage (var) | d-Vcross | Variation of crossing over all edges | | | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | | | 0 | ppm | 1,2 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.175V, VOH = 0.525V | 175 | | 700 | ps | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 0.525V VOL = 0.175V | 175 | | 700 | ps | 1 |
| Rise Time Variation | d-$t_r$ | | | | 125 | ps | 1 |
| Fall Time Variation | d-$t_f$ | | | | 125 | ps | 1 |
| Duty Cycle | $d_{t3}$ | Measurement from differential waveform | 45 | 50 | 55 | % | 1 |
| Skew | $t_{sk3}$ | $V_T$ = 50% | | | 50 | ps | 1 |
| Jitter, Cycle to Cycle | $t_{jcyc-cyc}$ | PLL Mode | | 40 | 50 | ps | 1,5 |
| | | BYPASS mode as additive jitter | | 15 | 50 | ps | 1,4,5 |
| Jitter, Phase | $t_{jphasebypass}$ | PCIe Gen 1 specs (pk to pk value) | | 30 | 86 | ps | 1,4 |
| | | PCIe Gen 2 specs (rms value) | | 2.6 | 3.1 | ps | 1,4 |
| | $t_{jphasePLL}$ | PCIe Gen 1 specs (pk to pk value) | | 40 | 86 | ps | 1,6 |
| | | PCIe Gen 2 specs (rms value) | | 2.8 | 3.1 | ps | 1,6 |
| | | PCIe Gen 3 specs (rms value) | | 0.7 | 1.0 | ps | 1,6,7 |

[1] Guaranteed by design and characterization, not 100% tested in production.
[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that the input clock complies with CK409/CK410/CK505 accuracy requirements.
[3] $I_{REF} = V_{DD}/(3xR_R)$. For $R_R$ = 475Ω (1%), $I_{REF}$ = 2.32mA. $I_{OH}$ = 6 x $I_{REF}$ and $V_{OH}$ = 0.7V @ $Z_O$ = 50Ω
[4] Applies to Bypass Mode Only
[5] Measured from differential waveform
[6] Device driven by HP81134A generator
[7] PCIe* Gen3 filter characteristics are subject to final ratification by PCISIG. Please check the PCI* SIG for the latest specification.

| SRC Reference Clock | | | |
|---|---|---|---|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, Route as non-coupled 50 ohm trace | 0.5 max | inch | 2, 3 |
| L2 length, Route as non-coupled 50 ohm trace | 0.2 max | inch | 2, 3 |
| L3 length, Route as non-coupled 50 ohm trace | 0.2 max | inch | 2, 3 |
| $R_S$ | 33 | ohm | 2, 3 |
| $R_t$ | 49.9 | ohm | 2, 3 |

| Down Device Differential Routing | Dimension or Value | Unit | Figure |
|---|---|---|---|
| L4 length, Route as coupled **microstrip** 100 ohm differential trace | 2 min to 16 max | inch | 2 |
| L4 length, Route as coupled **stripline** 100 ohm differential trace | 1.8 min to 14.4 max | inch | 2 |

| Differential Routing to PCI Express Connector | Dimension or Value | Unit | Figure |
|---|---|---|---|
| L4 length, Route as coupled **microstrip** 100 ohm | 0.25 to 14 max | inch | 3 |
| L4 length, Route as coupled **stripline** 100 ohm | 0.225 min to 12.6 max | inch | 3 |

Fig. 1

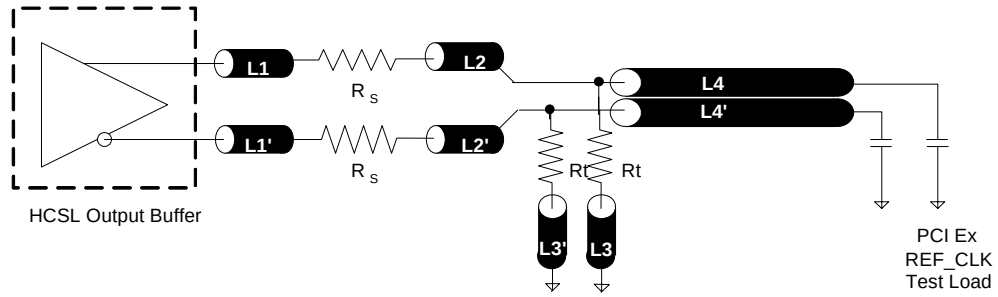



Fig. 2

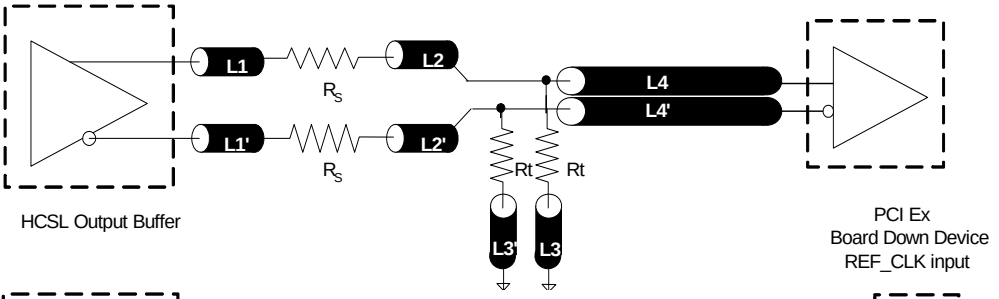
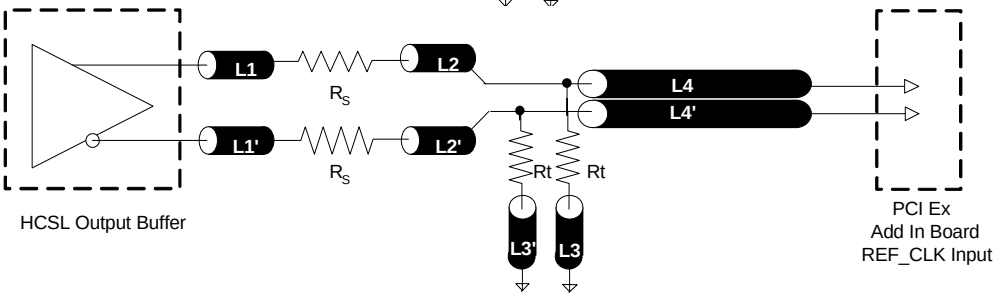



Fig. 3



## General SMBus serial interface information for the SLG74803

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address DC (H)
- Silego clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- Silego clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- Silego clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
(see Note 2)
- Silego clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address DC (H)
- Silego clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- Silego clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address DD (H)
- Silego clock will ***acknowledge***
- Silego clock will send the data byte count = X
- Silego clock sends ***Byte N + X -1***
- Silego clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).***
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | | **Silego(Slave/Receiv-er)** |
| T | Start Bit | | |
| Slave Address DC (H) | | | |
| WR | Write | | |
| | | | Ack |
| Beginning Byte = N | | | |
| | | | Ack |
| Data Byte Count = X | | | |
| | | | Ack |
| Beginning Byte N | | X Byte | |
| | | | Ack |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | Ack |
| P | Stop Bit | | |

| Index Block Read Operation | | | |
|---|---|---|---|
| **Controller (Host)** | | **Silego (Slave/Receiver)** | |
| T | Start Bit | | |
| Slave Address DC (H) | | | |
| WR | Write | | |
| | | | Ack |
| Beginning Byte = N | | | |
| | | | Ack |
| RT | Repeat Start | | |
| Slave Address DD (H) | | | Ack |
| RD | Read | | |
| | | | Ack |
| | | | |
| | | | Data Byte Count = X |
| Ack | | | |
| | | X Byte | Beginning Byte N |
| Ack | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not Ack | | |
| P | Stop Bit | | |

### SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (DC/DD)

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | - | PD_Mode | PD# drive mode | RW | driven | Hi-Z | 0 |
| **Bit 6** | - | STOP_Mode | SRC_Stop# drive mode | RW | driven | Hi-Z | 0 |
| **Bit 5** | - | PD_Polarity | X | RW | low | high | 0 |
| **Bit 4** | - | Reserved | Reserved | RW | Reserved | | X |
| **Bit 3** | - | Reserved | Reserved | RW | Reserved | | X |
| **Bit 2** | - | PLL_BW# | Select PLL BW | RW | High BW | Low BW | 1 |
| **Bit 1** | - | BYPASS# | BYPASS#/PLL | RW | fan-out | ZDB | 1 |
| **Bit 0** | - | SRC_DIV# | SRC Divide by 2 Select | RW | x/2 | 1x | 1 |

### SMBus Table:Output Control Register

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 42,41 | DIF_7 | Output Control | RW | Disable | Enable | 1 |
| **Bit 6** | 38,37 | DIF_6 | Output Control | RW | Disable | Enable | 1 |
| **Bit 5** | 34,33 | DIF_5 | Output Control | RW | Disable | Enable | 1 |
| **Bit 4** | 30,29 | DIF_4 | Output Control | RW | Disable | Enable | 1 |
| **Bit 3** | 20,21 | DIF_3 | Output Control | RW | Disable | Enable | 1 |
| **Bit 2** | 16,17 | DIF_2 | Output Control | RW | Disable | Enable | 1 |
| **Bit 1** | 12,13 | DIF_1 | Output Control | RW | Disable | Enable | 1 |
| **Bit 0** | 8,9 | DIF_0 | Output Control | RW | Disable | Enable | 1 |

### SMBus Table:Output Control Register

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | 42,41 | DIF_7 | Output Control | RW | Free-run | Stoppable | 0 |
| **Bit 6** | 38,37 | DIF_6 | Output Control | RW | Free-run | Stoppable | 0 |
| **Bit 5** | 34,33 | DIF_5 | Output Control | RW | Free-run | Stoppable | 0 |
| **Bit 4** | 30,29 | DIF_4 | Output Control | RW | Free-run | Stoppable | 0 |
| **Bit 3** | 20,21 | DIF_3 | Output Control | RW | Free-run | Stoppable | 0 |
| **Bit 2** | 16,17 | DIF_2 | Output Control | RW | Free-run | Stoppable | 0 |
| **Bit 1** | 12,13 | DIF_1 | Output Control | RW | Free-run | Stoppable | 0 |
| **Bit 0** | 8,9 | DIF_0 | Output Control | RW | Free-run | Stoppable | 0 |

### SMBBus Table: Output Control Register

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | | Reserved | | RW | Reserved | | X |
| **Bit 6** | | Reserved | | RW | Reserved | | X |
| **Bit 5** | | Reserved | | RW | Reserved | | X |
| **Bit 4** | | Reserved | | RW | Reserved | | X |
| **Bit 3** | | Reserved | | RW | Reserved | | X |
| **Bit 2** | | Reserved | | RW | Reserved | | X |
| **Bit 1** | | Reserved | | RW | Reserved | | X |
| **Bit 0** | | Reserved | | RW | Reserved | | X |

### SMBBus Table: Vendor & Revision ID Register

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | - | RID3 | REVISION ID | R | - | - | 0 |
| **Bit 6** | - | RID2 | | R | - | - | 0 |
| **Bit 5** | - | RID1 | | R | - | - | 0 |
| **Bit 4** | - | RID0 | | R | - | - | 0 |
| **Bit 3** | - | VID3 | VENDOR ID | R | - | - | 0 |
| **Bit 2** | - | VID2 | | R | - | - | 1 |
| **Bit 1** | - | VID1 | | R | - | - | 1 |
| **Bit 0** | - | VID0 | | R | - | - | 0 |

### SMBus Table: DEVICE ID

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | - | Device ID 7 (MSB) | | RW | Reserved | | 1 |
| **Bit 6** | - | Device ID 6 | | RW | Reserved | | 0 |
| **Bit 5** | - | Device ID 5 | | RW | Reserved | | 0 |
| **Bit 4** | - | Device ID 4 | | RW | Reserved | | 0 |
| **Bit 3** | - | Device ID 3 | | RW | Reserved | | 0 |
| **Bit 2** | - | Device ID 2 | | RW | Reserved | | 0 |
| **Bit 1** | - | Device ID 1 | | RW | Reserved | | 1 |
| **Bit 0** | - | Device ID 0 | | RW | Reserved | | 1 |

**SMBus Table: Byte Count Register**

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| **Bit 7** | - | BC7 | Writing to this register configures how many bytes will be read back. | RW | - | - | 0 |
| **Bit 6** | - | BC6 | | RW | - | - | 0 |
| **Bit 5** | - | BC5 | | RW | - | - | 0 |
| **Bit 4** | - | BC4 | | RW | - | - | 0 |
| **Bit 3** | - | BC3 | | RW | - | - | 0 |
| **Bit 2** | - | BC2 | | RW | - | - | 1 |
| **Bit 1** | - | BC1 | | RW | - | - | 1 |
| **Bit 0** | - | BC0 | | RW | - | - | 1 |

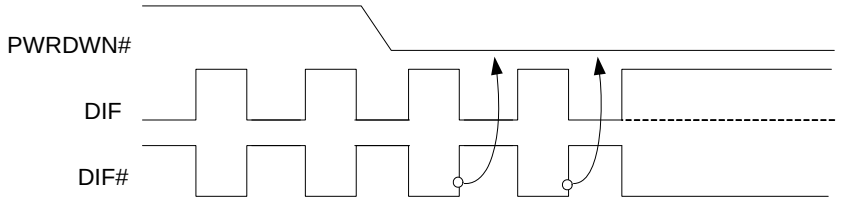
Note: Polarities in timing diagrams are shown OE_INV = 0. They are similar to OE_INV = 1.

**PD#, Power Down**

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

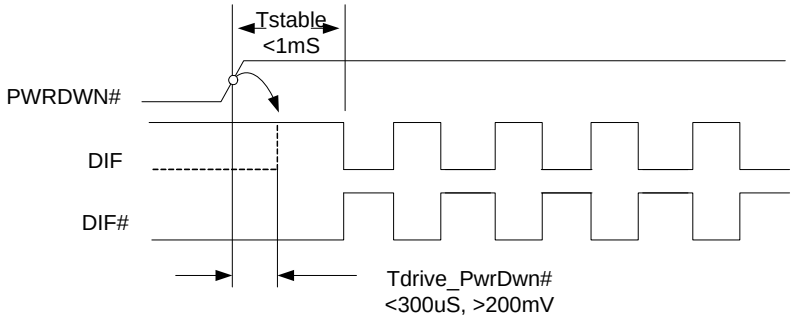
**PD# Assertion**

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to '0', all clock outputs will be held with DIF driven High with 2 x $I_{REF}$ and DIF# tri-stated. If the PD# drive mode bit is set to '1', both DIF and DIF# are tri-stated.




**PD# De-assertion**

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to '1', all the DIF outputs must driven to a voltage of >200 mV within 300 ms of PD# de-assertion.




## SRC_STOP#

The SRC_STOP# signal is an active-low asynchronous input that cleanly stops and starts the DIF outputs. A valid clock must be present on SRC_IN for this input to work properly. The SRC_STOP# signal is de-bounced and must remain stable for two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

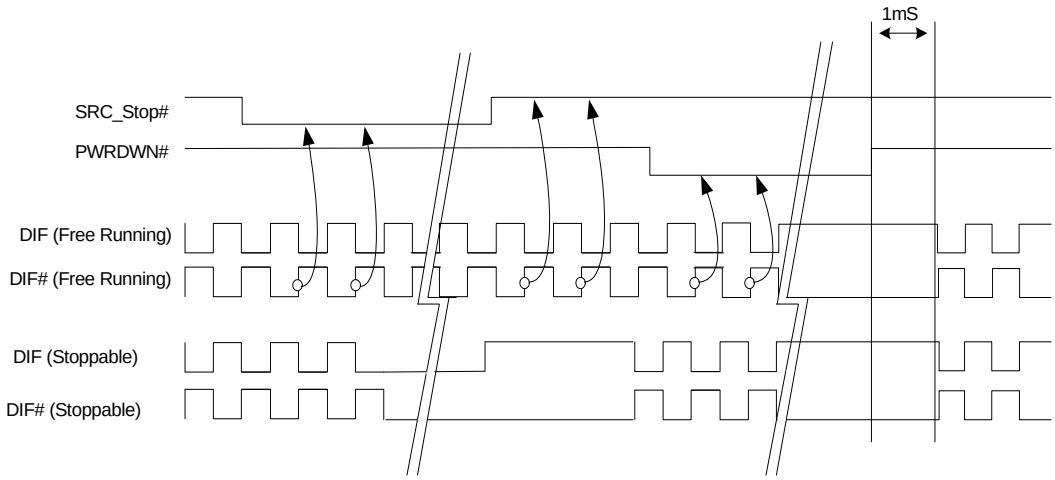
## SRC_STOP# - Assertion

Asserting SRC_STOP# causes all DIF outputs to stop after their next transition (if the control register settings allow the output to stop). When the SRC_STOP# drive bit is '0', the final state of all stopped DIF outputs is DIF = High and DIF# = Low. There is no change in output drive current. DIF is driven with 6x$I_{REF}$. DIF# is not driven, but pulled low by the termination. When the SRC_STOP# drive bit is '1', the final state of all DIF output pins is Low. Both DIF and DIF# are not driven.

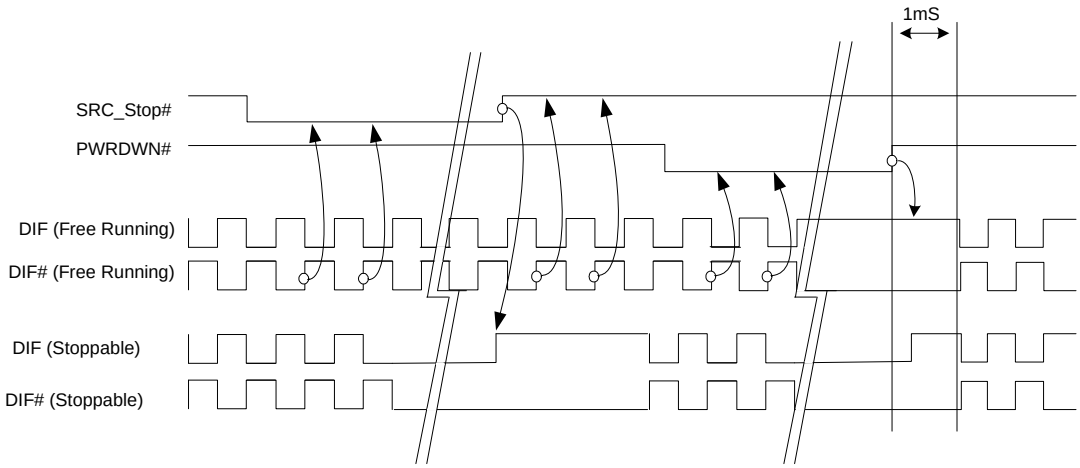
## SRC_STOP# - De-assertion (transition from '0' to '1')

All stopped differential outputs resume normal operation in a glitch-free manner. The de-assertion latency to active outputs is 2-6 DIF clock periods, with all DIF outputs resuming simultaneously. If the SRC_STOP# drive control bit is '1' (tri-state), all stopped DIF outputs must be driven High (>200 mV) within 10 ns of de-assertion.

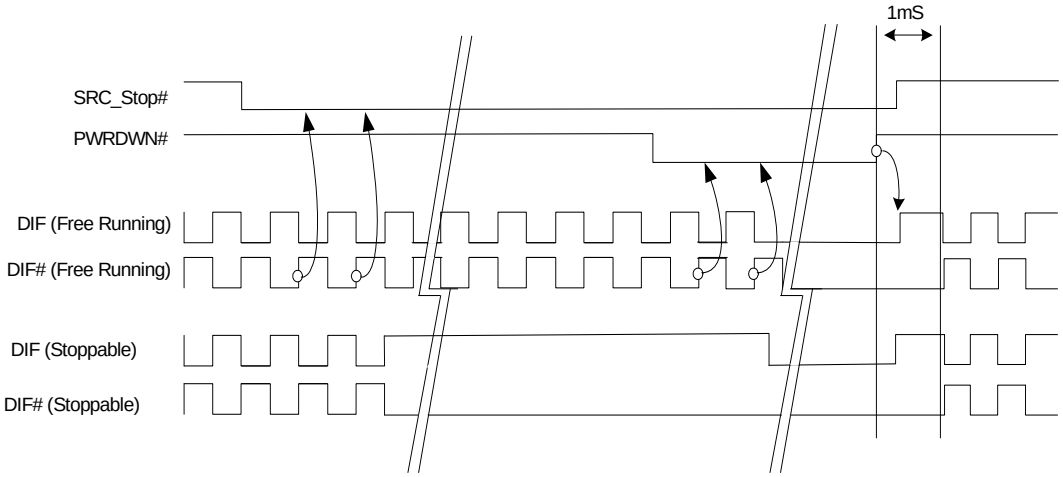
### SRC_STOP_1 (SRC_Stop = Driven, PD = Driven)



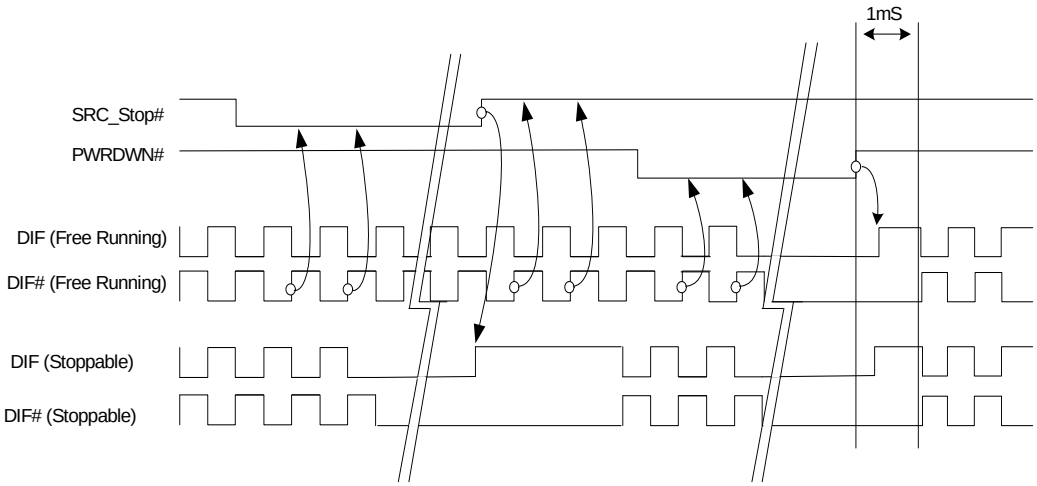

### SRC_STOP_2 (SRC_Stop = Tristate, PD = Driven)



## SRC_STOP_3 (SRC_Stop = Driven, PD = Tristate)




## SRC_STOP_4 (SRC_Stop = Tristate, PD = Tristate)

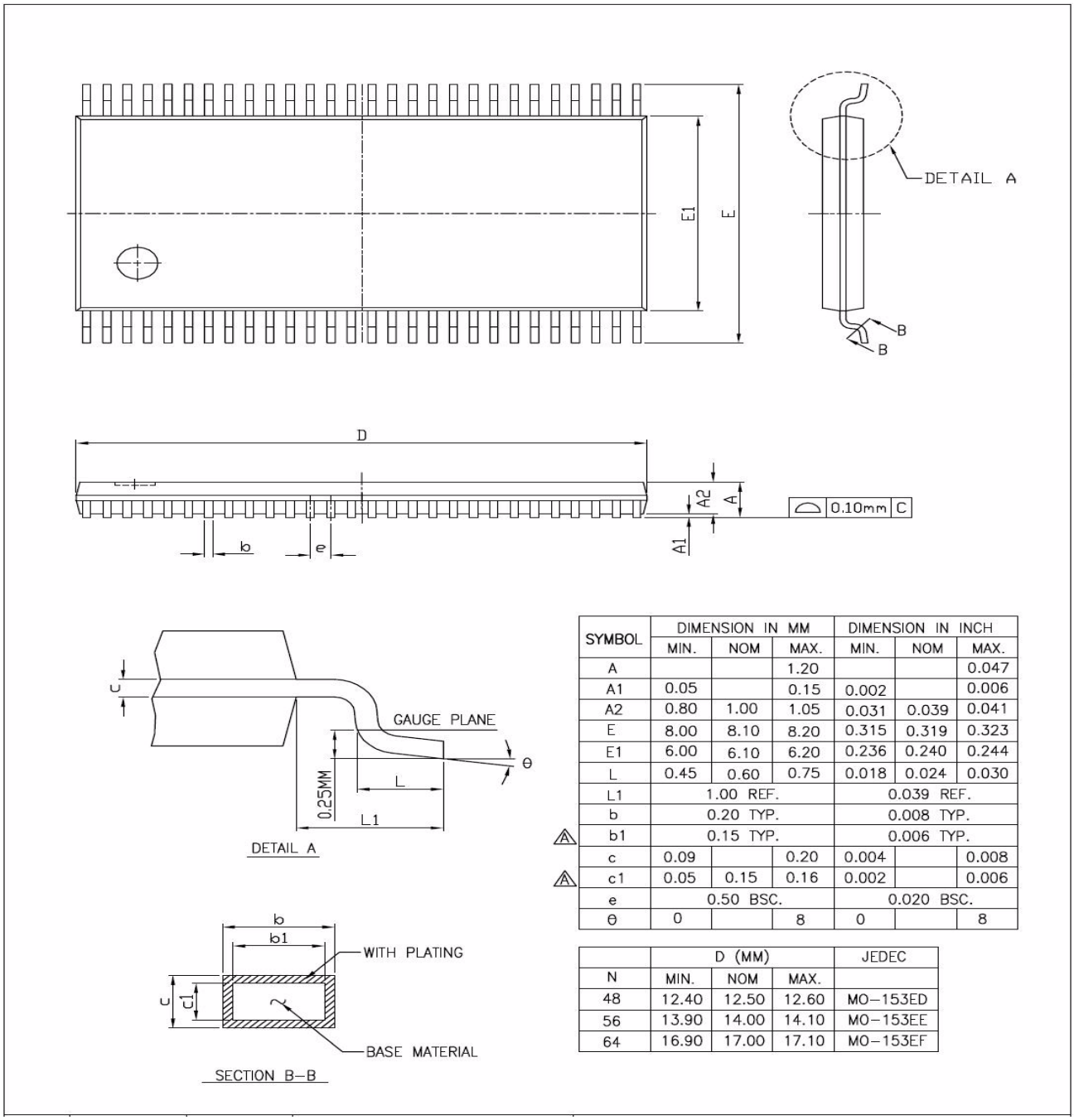



### Silego Ordering Information

| Part Number | Package Type | Temperature Range |
|---|---|---|
| SLG74803T | 48 Lead Green Package TSSOP | Commerical, 0°C to 70°C |
| SLG74803TTR | 48 Lead Green Package TSSOP - Tape and Reel | Commerical, 0°C to 70°C |
| SLG74803KT | 48 Lead Green Package TSSOP | Industrial, 0°C to 85°C |
| SLG74803KTTR | 48 Lead Green Package TSSOP - Tape and Reel | Industrial 0°C to 85°C |

## Package Drawings and Dimensions

**48L TSSOP (6.10 mm body, 0.50 mm pitch) see other dimensions in the table below.**
**(56-pin drawing is shown for reference)**




| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM | MAX. | MIN. | NOM | MAX. |
| A | | | 1.20 | | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 0.80 | 1.00 | 1.05 | 0.031 | 0.039 | 0.041 |
| E | 8.00 | 8.10 | 8.20 | 0.315 | 0.319 | 0.323 |
| E1 | 6.00 | 6.10 | 6.20 | 0.236 | 0.240 | 0.244 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF. | | | 0.039 REF. | | |
| b | 0.20 TYP. | | | 0.008 TYP. | | |
| ⚠ b1 | 0.15 TYP. | | | 0.006 TYP. | | |
| c | 0.09 | | 0.20 | 0.004 | | 0.008 |
| ⚠ c1 | 0.05 | 0.15 | 0.16 | 0.002 | | 0.006 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| θ | 0 | | 8 | 0 | | 8 |

| | D (MM) | | | JEDEC |
|---|---|---|---|---|
| N | MIN. | NOM | MAX. | |
| 48 | 12.40 | 12.50 | 12.60 | MO–153ED |
| 56 | 13.90 | 14.00 | 14.10 | MO–153EE |
| 64 | 16.90 | 17.00 | 17.10 | MO–153EF |