Digital Green-Mode Synchronous Rectifier Controller

1 Description

The iW673 is a high performance synchronous rectifier controller with an integrated MOSFET driver for flyback converters operating at discontinuous conduction mode. Combined with the MOSFET, the iW673 can emulate the diode rectifier at the secondary side of the flyback to reduce conduction loss. The iW673 determines the timing of the driver by sensing the voltage across the $R_{DS(ON)}$ to achieve lossless sensing. The iW673 uses proprietary digital adaptive turn-off control technology to minimize the turn-off deadtime of the synchronous rectifier so that the parallel Schottky diode required by conventional synchronous rectifiers can be eliminated. The integrated driver has strong driving capability for high efficiency. The operating power consumption of the controller excluding the driver is less than 4mW at no load to achieve the ultra-low no-load power consumption at 5V output. The iW673 integrates a pulse linear regulator to maintain the operation of the synchronous rectifier at low system output voltage when the system is operating in constant current (CC) mode.

2 Features

- Digital adaptive turn-off control minimizes dead-time and eliminates the parallel Schottky diode
- Integrated pulse linear regulator (PLR) enables SR operation at down to 2.4V system output when system is in constant current (CC) mode with iW673-00, iW673-01, or iW673-20
- Wide V_{IN} pin operating voltage up to 25V (16V for iW673-00)
- Optimized 5V MOSFET gate driver Intelligent low power management achieves ultra-low no-load operating current
- Lossless MOSFET V_{DS} sensing for SR timing control
- 6-pin SOT23 package

3 Applications

- Compact AC/DC adapters/chargers for media tablets and smart phones

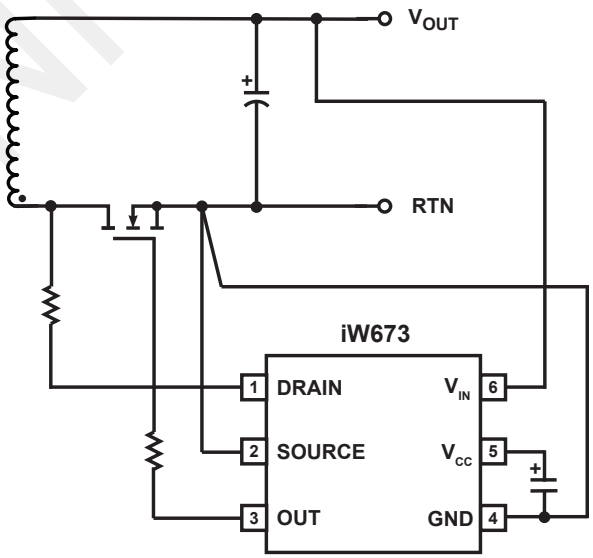


Figure 3.1 : iW673 Typical Application Circuit

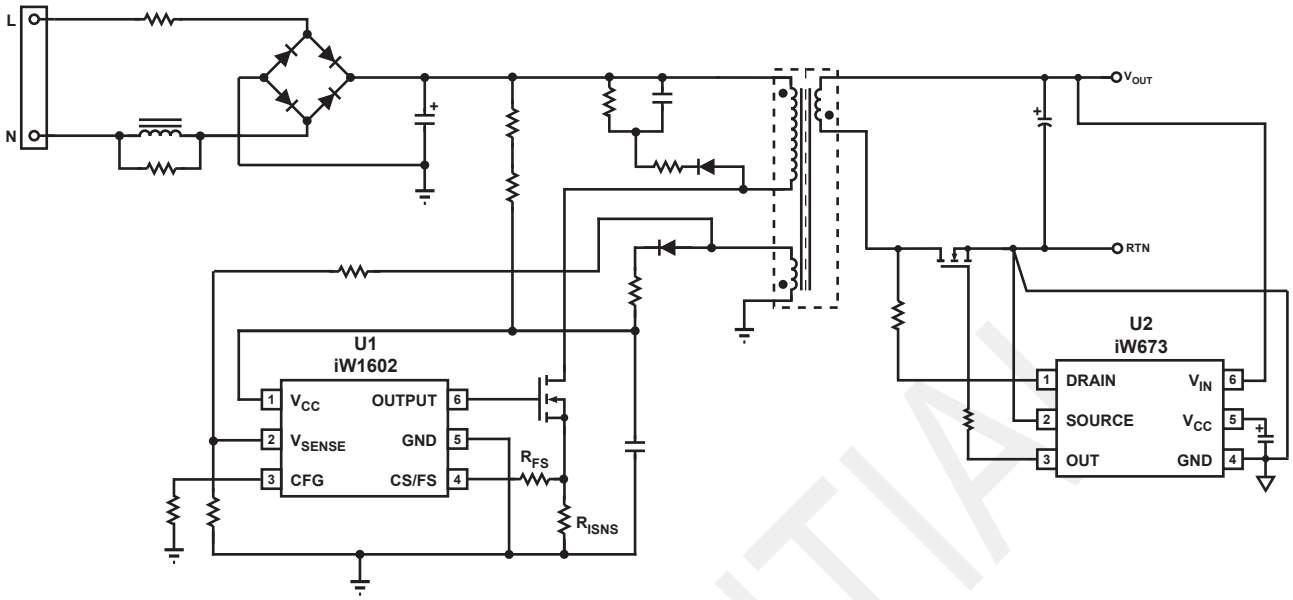


Figure 3.2 : iW673 Typical Application Circuit Using iW1602 as the Primary-Side Controller (Achieving <75mW No-Load Power Consumption in 5V, 2.5A Adapter Designs with Fast Dynamic Load Response, and Supporting Constant Current Operation down to 2.4V System Output)

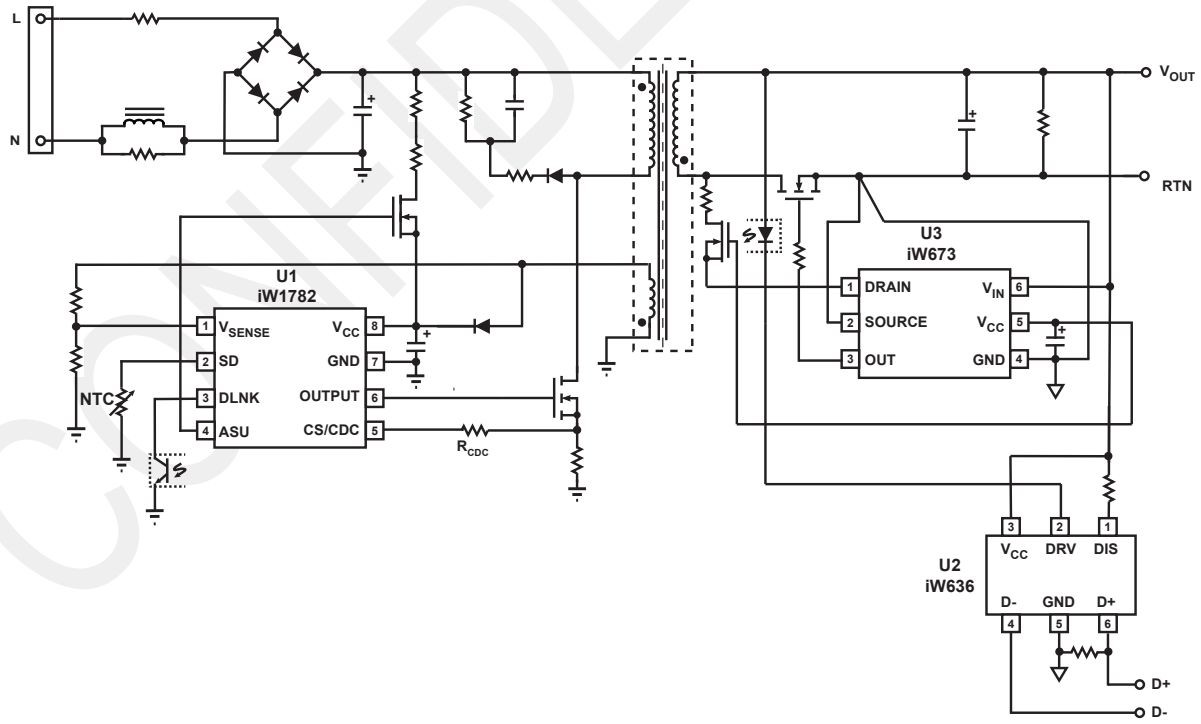


Figure 3.3 : iW673 Typical Application Circuit for Multi-Level Output Voltage and Current (Using iW1782 as Primary-Side Controller and iW636 as Secondary-Side Controller for Qualcomm® Quick Charge™ 3.0) (Achieving <20mW No-Load Power Consumption)

Note: The DFET clamping circuit at the DRAIN pin of iW673 is not needed if the maximum voltage on the drain of the SR MOSFET is lower 60V.

4 Pinout Description

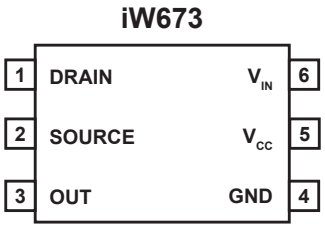


Figure 4.1 : 6-Pin SOT23 Package

Pin No.	Pin Name	Type	Pin Description
1	DRAIN	Analog Input	Synchronous rectifier MOSFET drain voltage sensing and the Pulse Linear Regulator (PLR) input.
2	SOURCE	Analog input	Synchrnous rectifier MOSFET source voltage sensing input.
3	OUT	Output	Synchronous rectifier MOSFET driver.
4	GND	Ground	Ground.
5	V_{CC}	Power Input	Output of internal LDO and PLR. It provides bias voltage for the internal logic circuit and the MOSFET driver. Connect this pin to a capacitor.
6	V_{IN}	Analog Input	Input of internal LDO and system output voltage sensing circuit. Connect to adapter/charger output for bias voltage. The internal LDO clamps the V_{CC} voltage at 5V when V_{IN} > 5V. The V_{IN} is also the input for the PLR enable comparator and the SR enable comparator.

5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.

Parameter	Symbol	Value	Units
V_{IN} DC supply voltage range (pin 6, I_{CC} = 15mA max)	V_{IN}	-0.3 to 33	V
Continuous DC supply current at V_{IN} pin (V_{IN} = 30V)	I_{VO}	15	mA
Continuous DC supply current at V_{CC} pin (V_{CC} = 5.5V)	I_{VCC}	15	mA
Gate peak output current	I_G	±3	A
DRAIN pin voltage (Note 1)	V_D	-1.5 to 60	V
DRAIN pin peak current	I_{DRAIN}	-40 to 300	mA
SOURCE pin voltage	V_{SOURCE}	- 0.6 to 1	V
V_{CC} pin voltage	V_{CC}	-0.6 to 6	V
Junction temperature	T_J	-40 to 150	°C
Storage temperature		–65 to 150	°C
Thermal resistance junction-to-ambient	θ_{JA}	190	°C/W
ESD rating per JEDEC JESD22-A114		2,000	V

Notes:

Note 1: The DRAIN pin voltage should not be below -0.6V for more than 500 ns.

6 Electrical Characteristics

V_{CC} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Low Dropout Regulator (LDO) and Pulse Linear Regulator (PLR) Blocks							
Switching between LDO and PLR							
PLR disable rising threshold at V_{IN} pin		$V_{LR\_DISABLE}$		4.49	4.7	4.92	V
PLR disable hysteresis at V_{IN} pin (iW673-0X and iW673-20)		V_{LR_HYS}		0.13	0.16	0.22	V
PLR enable falling threshold at V_{IN} pin (iW673-0X and iW673-20)		V_{LR_ENABLE}		4.31	4.55	4.81	V
LDO							
Recommended DC input voltage range (Note 1)	For iW673-00	$V_{IN\_DC\_MAX}$				16	V
	For all others					25	V
DC regulation voltage		V_{CC_LDO}	V_{IN} = 6V, I_{LDO} = 5mA	4.7	5	5.35	V
Pulse Linear Regulator (PLR)							
Regulated output voltage at V_{CC}		V_{PLROUT}		4.2	5	5.5	V
Synchronous Rectifier Block							
Bias Voltage Supply							
DC supply operating voltage (Note 1)		V_{CC}				5.5	V
Bias current		I_{CC_BIAS}	OUT pin floating, 50kHz		640	1300	µA
Bias current, no load		I_{CC_NL}	OUT pin floating, 1kHz		430	750	µA
UVLO for SR Driver Block, at V_{CC} Pin							
V_{CC} POR threshold, SR		$V_{CC\_SR\_POR}$	Voltage applied on V_{CC} and V_{IN} floating	3.13	3.3	3.47	V
UVLO hysteresis, SR		$V_{CC\_\_SR\_HYS}$	Voltage applied on V_{CC} and V_{IN} floating	0.15	0.24	0.33	V
V_{CC} UVLO threshold, SR		$V_{CC\_\_SR\_UVLO}$	Voltage applied on V_{CC} and V_{IN} floating	2.9	3.1	3.22	V
Gate Driver							
Gate pull-up resistor		R_{UP}		2.5	4	6.5	Ω
Gate pull-down resistor		R_{DOWN}		1	2	4.1	Ω
Gate output high voltage (Note 2)		V_{G_H}		V_{CC}-0.3	V_{CC}-0.2	5.5	V
Gate output low voltage (Note 2)		V_{G_L}		0	0.15	0.25	V
Gate rising time (Note 2)		t_{G_RISE}	1V to 4V, 3.3nF		44		ns
Gate falling time (Note 2)		t_{G_FALL}	1V to 4V, 3.3nF		31		ns

6 Electrical Characteristics (continued)

V_{CC} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
SR function enable threshold, at V_{IN} pin		V_{SR_ENABLE}		2	2.2	2.4	V
SR function enable hysteresis, at V_{IN} pin		$V_{SR\_ENABLE\_HYS}$		0.075	0.18	0.3	V
Turn-on threshold		V_{ON_TH}		-153	-120	-95	mV
Turn-off threshold, initial		$V_{OFF\_TH\_INIT}$		-5	0	5	mV
Minimun off delay comparator threshold		$V_{MIN\_OFF\_TH}$		0.28	0.6	1	V
Minimum On/Off Time							
Minimum on time	For iW673-01	t_{ON_MIN}		0.875	1.0	1.125	µs
	For all others			0.7	0.8	0.9	
Minimum off time (Note 3)		t_{OFF_MIN}		2.2	2.5	2.8	µs

Notes:

Note 1: The parameters are recommended maximum operation range of the pin.

Note 2: These parameters are not 100% tested. They are guaranteed by design and/or characterization.

Note 3: The minimum off time increases if the actual on time is the same as the minimum on time. See Section 9.3 for more information.

7 Typical Performance Characteristics

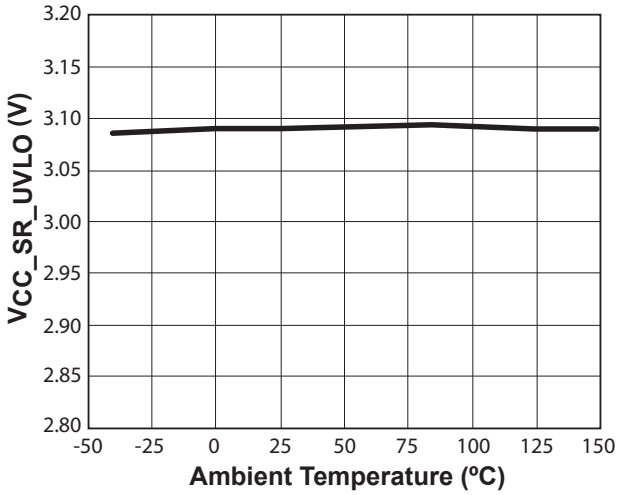


Figure 7.1 : V_{CC} UVLO Voltage vs.Temperature

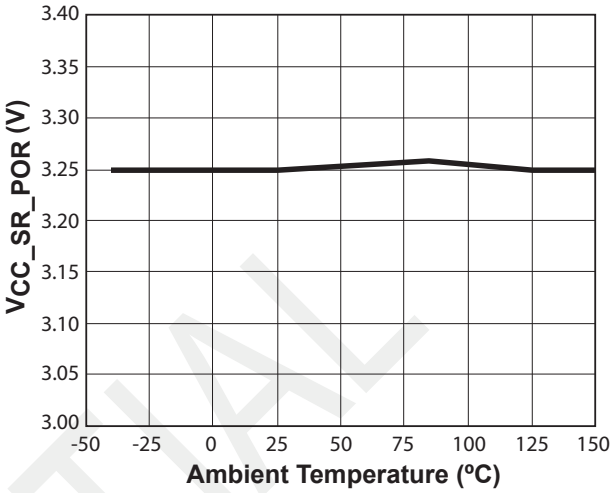


Figure 7.2 : V_{CC} POR Voltage vs.Temperature

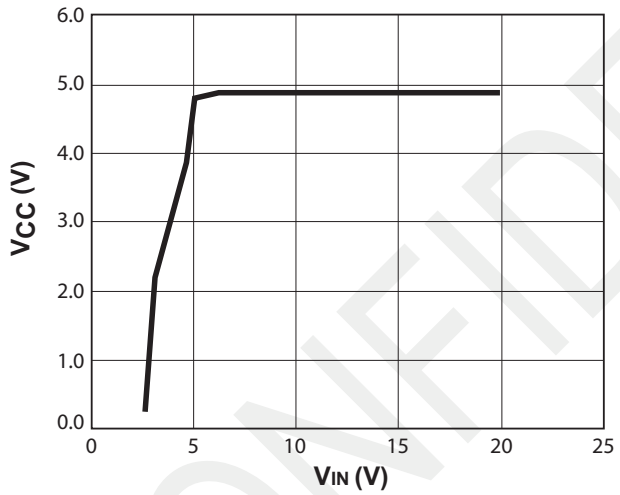


Figure 7.3 : LDO Regulation

8 Functional Block Diagram

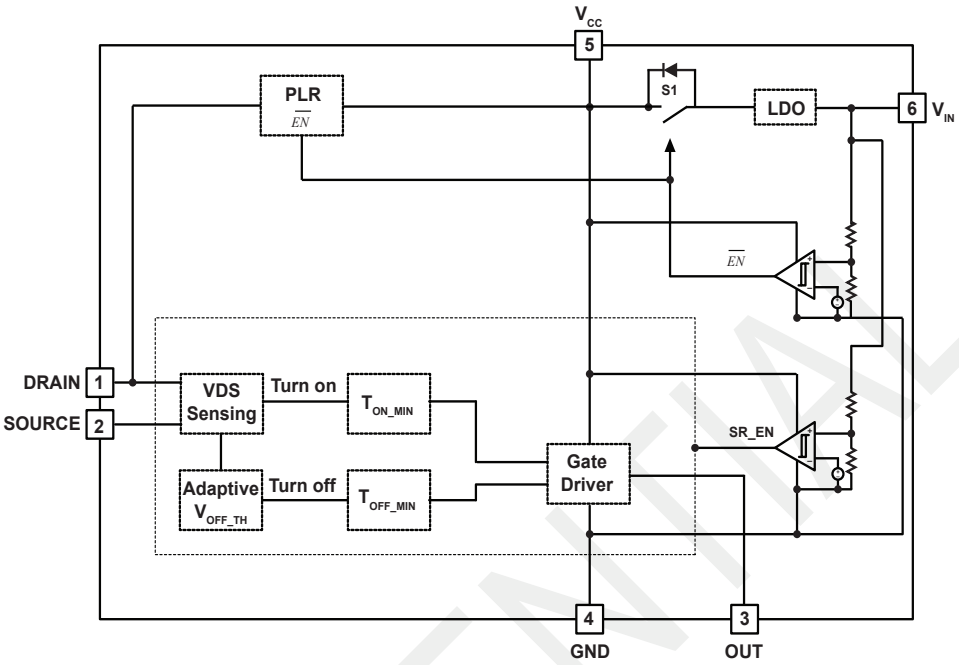


Figure 8.1 : iW673 Functional Block Diagram

9 Theory of Operation

The iW673 is a synchronous rectifier controller that uses a new, proprietary digital adaptive turn-off control technology to minimize the turn-off deadtime. This results in a lower diode conduction loss at the deadtime so that no parallel Schottky diode is required.

Figure 8.1 shows the block diagram of iW673. It measures the voltage across the synchronous MOSFET to achieve lossless current sensing for the driver timing control. The digital SR logic control block generates the gate driver control signal based on the drain-to-source voltage of the synchronous MOSFET. The gate driver control signal is fed into the integrated MOSFET driver to drive the synchronous MOSFET.

The iW673 includes two independent branches of V_{CC} regulators to support wide system output operation range. The internal LDO of the iW673 is connected to the system output to provide a stable 5V output to the V_{CC} when system output is 5V or above. It supports up to 25V (up to 16V for iW673-00) input to cover a wide range of system output voltage levels. When the system output voltage is low, the PLR circuit utilizes the DRAIN voltage of the synchronous MOSFET to maintain sufficient V_{CC} voltage for iW673 operation and MOSFET driving. Refer to Section 9.2 for details and product options.

The iW673 enters light load mode when the switching frequency of the flyback is low. The operating current is reduced to 430µA (typical) to reduce the light load and no load loss of the whole system.

9.1 Pin Detail

Pin 1 – DRAIN

Synchronous MOSFET drain voltage sensing and Pulse Linear Regulator (PLR) input. Connect this pin as close to the drain of the MOSFET as possible to avoid noise picked up from the traces.

At start-up, the PLR circuit is enabled to bring up the V_{CC} of iW673 as fast as possible. The peak current to this pin at start-up can be as high as 300mA. The average current at normal operation is less than 10mA. Note that the voltage rating of the pin is 60V. In 9V or 12V system output applications, the synchronous MOSFET's drain voltage may be above the DRAIN pin's maximum voltage rating. In this case, DFET is needed to clamp the DRAIN pin voltage. Refer to Section 9.4 for details.

A 50Ω resistor is recommended between MOSFET and the pin to limit the negative current within -40mA, and to protect the DRAIN pin in case of the synchronous MOSFET failure.

Pin 2 – Source

Synchronous MOSFET source voltage sensing. Connect this pin as close to the source of the MOSFET as possible to avoid noise picked up from the traces.

Pin 3 – OUT

Gate drive for the external synchronous MOSFET switch.

Pin 4 – GND

Ground.

Pin 5 – V_{CC}

Output of Pulse Linear Regulator and the internal linear regulator. It provides bias voltage for the controller. A capacitor (typical 4.7µF) must be connected between the V_{CC} pin and GND. When an electrolytic capacitor is used, a decoupling capacitor of 0.1uF or so should be connected between the V_{CC} pin and GND.

Pin 6 – V_{IN}

Internal linear regulator (LDO) input. Connect this pin to the flyback output. The internal linear regulator output is internally connected to V_{CC} through a MOSFET (S1 in Figure 8.1).

This pin is also the input of PLR-enabling comparator. This comparator enables and disables the PLR circuit based on the V_{IN} pin voltage. Refer to Section 9.2 for more details.

This pin is also the input of synchronous rectification function comparator. The synchronous rectification function is disabled if the V_{IN} pin voltage is lower than 2.2V (typical).

9.2 Powering the Controller

Internal circuits of the controller require bias voltage between 3V and 5.5V from the capacitor at the V_{CC} pin. Depending on the flyback output voltage level and the connection, the V_{CC} is powered by either the internal linear regulator (LDO) or the internal pulse linear regulator (PLR).

9.2.1 The iW673-0X and iW673-20 for CC Mode Operation at Very Low Output Voltage

The iW673-0X and iW673-20 are designed for AC/DC adapter systems which require Constant Current (CC) operation at very low output voltage, such as systems with 3V or 2.5V CC shutdown voltage.

When the flyback operates at constant current mode, the flyback output voltage may drop to 3V or below. In order to provide sufficient bias voltage for the continuous operation of the synchronous rectifier controller at constant current mode, the pulse linear regulator provides bias current to the controller from the drain of the synchronous MOSFET. The IC monitors the flyback output voltage at the V_{IN} pin. When flyback output voltage is lower than 4.55V (typical), the PLR block is enabled. Pulse current from the drain of the synchronous MOSFET charges and maintains the V_{CC} voltage level at 5V. In order to prevent reverse current from V_{CC} to V_{IN} pin, the MOSFET S1 between the LDO output and the V_{CC} pin is at the OFF state when the PLR is at the ON state.

At normal operation when the flyback output is higher than 4.7V (typical), the PLR is at the OFF state and the switch MOSFET S1 is at the ON state. The flyback output provides the operating current through the LDO into the V_{CC} pin. The LDO regulates the V_{CC} voltage at 5V. When the flyback output is close to 5V, the LDO cannot maintain V_{CC} regulation and it operates at pass through mode. In this mode the drop-out voltage from the V_{IN} pin to V_{CC} pin is smaller than 0.4V when the V_{IN} pin current is 5mA.

At start-up, both PLR and the internal linear regulator are enabled. Although the switch S1 is turned off, the LDO is still able to charge the capacitor at V_{CC} through the body diode of S1. Since the PLR has stronger current capability and higher input voltage level, it may charge up the V_{CC} voltage higher than the flyback output voltage during the startup. Once the flyback output voltage reaches 4.7V (typical), the PLR is at the OFF state. The switch S1 is at the ON state and the internal LDO provides the operating current to V_{CC}.

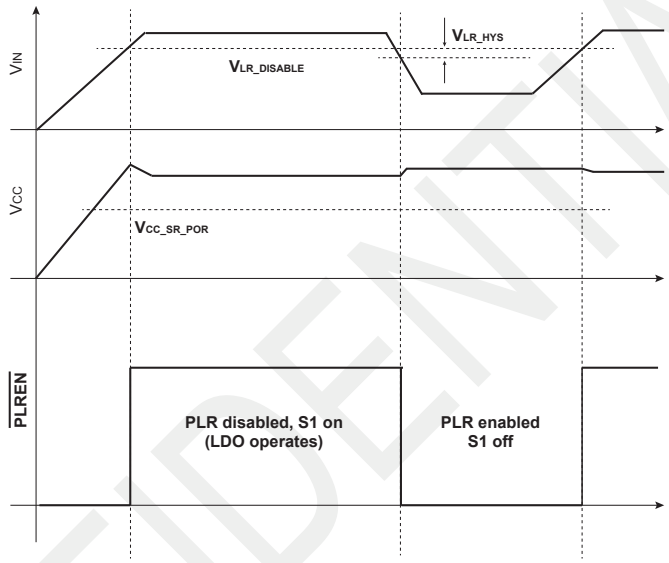


Figure 9.1 : Switching between the Two Power Sources in iW673-00, iW673-01, or iW673-20

9.2.2 The iW673-10 to Support Light-Load Operation at Low V_{OUT}

The PLR circuit requires enough duty cycle (primary on-time over switching period) of the flyback converter in order to provide enough charging current into the V_{CC} to maintain the voltage level. In typical designs the PLR circuit can hold V_{CC} above 4V when the duty cycle is at least 5%. When the system operates at CC mode, there is enough system loading to maintain high duty cycle so that PLR circuit can maintain the V_{CC} level. However, in some applications, the system may operate at 3.6V no load in which condition the duty cycle of the flyback is much less than 5%. Thus the PLR circuit is not able to maintain the V_{CC} voltage. On the other hand, since the system output is lower than 4.55V (typical), the iW673-0X or iW673-20 turns off the internal switch S1 in the LDO block, thus the voltage dropping between the V_{IN} pin and the V_{CC} pin is at least a diode voltage drop with a typical value of 0.8V. With 3.6V system output at no load, the V_{CC} voltage drops below the ULVO of the IC, therefore the iW673-0X or iW673-20 cannot operate under such condition.

The PLR circuit in iW673-10 is enabled at start-up before the system output reaches 4.7V (typical). As a result, the PLR circuit can bring up the V_{CC} for SR operation when the system output is still low during start-up or under the system output short circuit fault condition.

Once the system successfully starts up with its output voltage reaching 4.7V, the PLR circuit is disabled and remains disabled until the UVLO of the iW673-10. The V_{CC} of iW673-10 is powered only by the LDO which utilizes the voltage from the system output. The internal switch S1 remains on after PLR circuit is disabled to minimize the voltage drop on the LDO circuit. Since the system output in this application remains above 3.6V, the V_{CC} is held above 3V to maintain operation and to drive the synchronous MOSFET. Since the PLR circuit is disabled after start-up, the system using iW673-10 cannot support CC operation at a very low voltage. It is recommended that the system CC shutdown voltage

is equal to or above 4V when iW673-10 is used. And the turn-on threshold of the synchronous MOSFET used in the system should be below 3V to guarantee that it can be turned on under low system output. The switching between PLR and LDO for iW673-10 is shown in Figure 9.2.

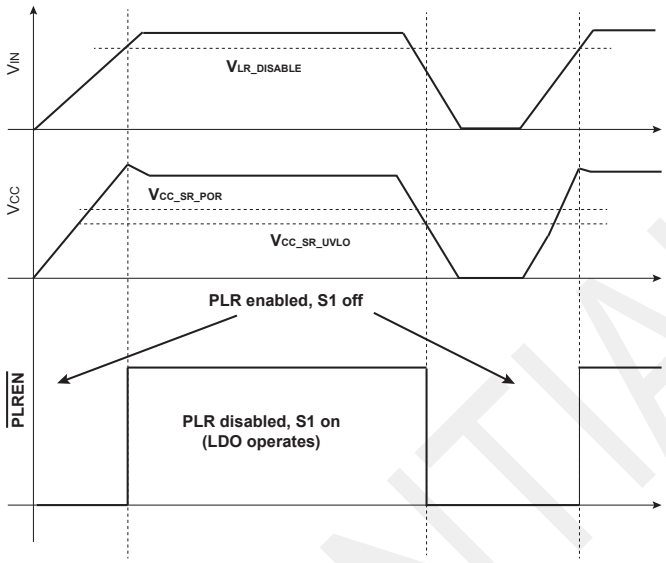


Figure 9.2 : Switching between the Two Power Sources in iW673-10

9.3 V_{DS} Sensing and Synchronous Rectifier Driving Scheme

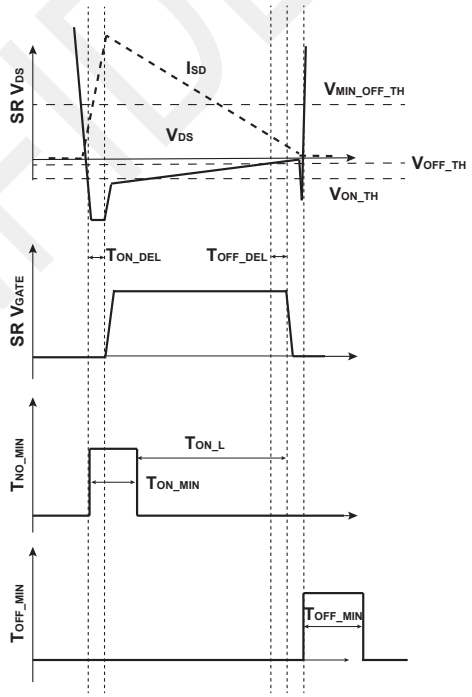


Figure 9.3 : SR Control Block Sequencing Diagram

The synchronous rectifier (SR) control block monitors the synchronous MOSFET's drain-to-source voltage (V_{DS}) to determine the driver timing. When the V_{DS} is below the V_{ON_TH} (-120mV), control block turns on the synchronous

MOSFET with its built-in driver. The driver has a minimum on-time (T_{ON_MIN}) to avoid the noise from turning off the driver immediately.

For applications with high output current or output power, a larger package such as TO-220 is usually chosen for the synchronous MOSFET for thermal consideration. Such packages introduce larger parasitic inductances into the circuit. As a result the V_{DS} voltage ringing during the SR turn-on may need longer time to settle. The iW673-01 is designed to support such applications with a longer minimum on-time.

As the current I_{SD} decreases, V_{DS} increases and gets close to 0 mV. The SR driver is turned off when the V_{DS} reaches V_{OFF_TH}. The iW673 builds in Dialog's proprietary adaptive turn-off technology to minimize the turn-off deadtime.

After the SR driver turns off, the V_{DS} rises. When the V_{DS} reaches $V_{MIN\_OFF\_TH}$, the SR control block initiates a 2.5µs timer during which the SR remains off to avoid the ringing from turning on the synchronous MOSFET. The drain-to-source voltage of the synchronous MOSFET has a ringing after the secondary current reaches zero, which is caused by the magnetizing inductance of the transformer and the parasitic capacitances of the MOSFETs and the transformer. Depending on the damping factor, this ringing may reach the turn-on threshold of iW673 in its first ringing cycle. The 2.5µs T_{OFF_MIN} is designed to prevent it from turning on the synchronous MOSFET. In typical 10W to 25W designs, the ringing frequency is between 500kHz and 1MHz. Thus the 2.5µs T_{OFF_MIN} is long enough to cover the first ringing cycle. However, in designs with lower ringing frequency, the first ringing cycle may be longer than 2µs, and the ringing may cause a false turn-on of synchronous MOSFET. In this case, it is recommended to use a resistor in parallel with the transformer winding to damp the ringing so that the ringing does not reach the turn-on threshold of iW673 in the first ringing period.

If the T_{ON_L} in Figure 9.3 is smaller than 100ns, the following T_{OFF_MIN} is extended to 5µs.

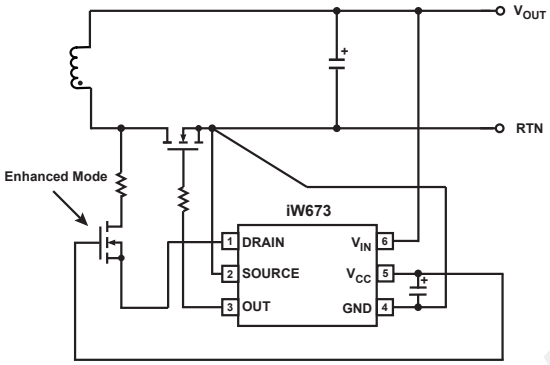
During the start-up, the system output voltage may be too low to reset the transformer so that the system may operate at the Continuous Current Mode (CCM). To avoid the SR operation at CCM, a comparator at V_{IN} pin monitors the system output. When V_{IN} voltage is lower than 2.2V (typical), the whole SR control block is disabled.

9.4 High Voltage Support for DRAIN Pin

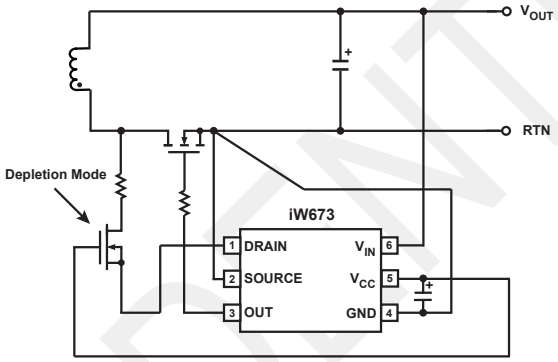
The recommended maximum DC operation voltage of the V_{IN} pin is 16V. Therefore, the iW673 can support a wide range of system output voltages, such as 5V, 9V, 12V, or above. However, the maximum voltage ratings of the DRAIN pin is limited to 60V, which provides enough margins for a typical 5V output design but may not be sufficient for higher output designs. During a system design stage, it is recommended to evaluate the voltage stress on the drain of the SR MOSFET. If the maximum drain-to-source voltage on the SR MOSFET is close to or higher than 60V, an external voltage clamping circuit is required to protect the DRAIN pin.

Figure 9.4 shows recommended voltage clamping circuits for different applications in which the voltage stress on the drain of the SR MOSFET exceeds 60V. If the PLR function is not used, the DRAIN pin can be protected with a NMOS, as shown in Figure 9.4(a). By connecting the gate of the NMOS to V_{CC} of iW673, the DRAIN pin voltage (connected to the source of the NMOS) is clamped below $V_{CC} – V_{TH}$, where the V_{TH} is the turn-on threshold of the NMOS. The V_{TH} of the NMOS is recommended to be smaller than 3V (maximum 2.5V preferred) to allow proper operation of the iW673.

If the PLR function is used, in order for the PLR circuit to operate properly, the maximum DRAIN voltage should be higher than the V_{CC} voltage. The enhanced mode NMOS cannot be used as the clamping circuit. Instead, a depletion NMOS is recommended as the clamping circuit for such applications, as shown in Figure 9.4(b). By connecting the gate of the depletion mode NMOS to V_{CC} of iW673, the DRAIN pin voltage (connected to the source of the depletion mode NMOS) is clamped below $V_{CC} – V_{TH}$, where the V_{TH} is the turn-on threshold of the depletion mode NMOS and has a negative value. The V_{TH} of the depletion mode NMOS is recommended to be lower than -5V to allow enough current driving capability of the pulse linear regulator.



(a) Voltage Clamping Circuit for DRAIN Only, PLR Not Used



(b) Voltage Clamping Circuit for DRAIN Pin with PLR Function Support

Figure 9.4 : Clamping Circuit for DRAIN Pin of the iW673

9.5 Layout Considerations

The layout of the system printed circuit board is very important for high performance of the controller IC in terms of accurate signal sensing and lower driving related loss.

The switching on and off of the active device in the switch mode power supply causes fast current and voltage change in the circuit. Such fast current change induces voltage transient on the parasitic impedance of the power devices, interconnect or circuit traces. This voltage transient may be picked up by the signal sensing circuit of the controller and may compromise its performance. Therefore it is important to reduce this voltage transient by minimizing the parasitic impedance with proper layout. The critical components must be placed as close to each other as possible and be connected with wide and short traces.

Figure 9.5 shows the critical components and their connections on the secondary side of a flyback converter with a synchronous rectifier. The synchronous MOSFET and the output capacitor must be close to each other. And the PCB trace between them must be wide and short. The GND pin of the iW673 must be connected to the source of the MOSFET with single point connection. If vias are used in the layout for the ground connection, it is recommended to use at least two vias in parallel to reduce their impedance.

To reduce the ringing at the turn-on and turn-off transient of the synchronous MOSFET, the gate driving current loop must be as small as possible.

The V_{CC} capacitor (C_{VCC}) must be as close to the pin 4 and 5 of the IC as possible. The traces connecting the capacitor to the IC pins should be as short as possible.

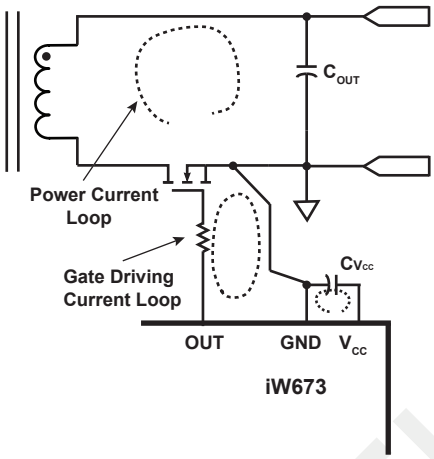


Figure 9.5 : Power Loops at the Secondary Side of the Flyback

Figure 9.6 shows the connection for V_{DS} voltage sensing. It is very important that the source of synchronous MOSFET is directly connected to the SOURCE pin of the iW673. The DRAIN pin must be connected as close to the drain of synchronous MOSFET as possible. The voltage sensing loops must be minimized to reduce the coupling of noise.

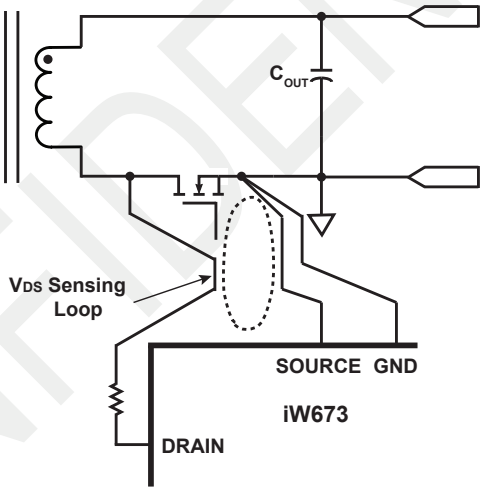


Figure 9.6 : Voltage Sensing Loops at the Secondary Side of the Flyback

Figure 9.7 shows an example of an improper layout connection. In this layout the SOURCE of the iW673 is not connected to the source of the MOSFET. Instead, it is connected closer to the system output connector at point B. The trace between point A and B carries the output current. Such current causes voltage drop on the trace and introduces an offset on the V_{DS} sensing circuit. This offset changes with the load current and affects the turn-off timing of the iW673. To avoid this issue, the SOURCE of the iW673 must be connected directly to point A.

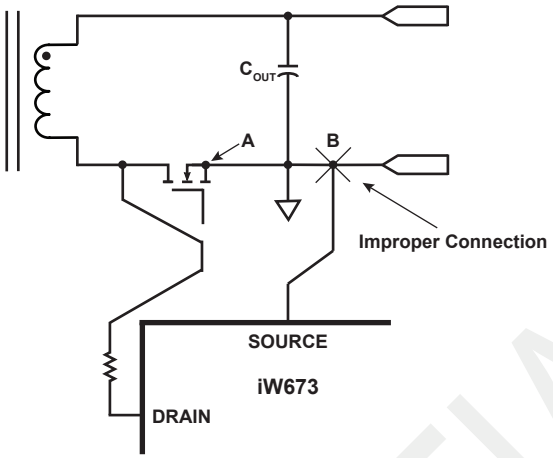


Figure 9.7 : Example of Improper Ground Connection

Figure 9.8 shows the connection for V_{IN} LDO input loop. It is also the V_{IN} voltage sensing loop. It is very important that the loop is minimized for proper voltage sensing and low input noise for proper LDO output regulation. The V_{IN} pin of iW673 should be connected to the output capacitor using a single point connection. If the loop has to be large due to the PCB constraints, such as when single layer PCB is used, an RC filter is recommended at the V_{IN} pin of iW673 to minimize the impact of the noise.

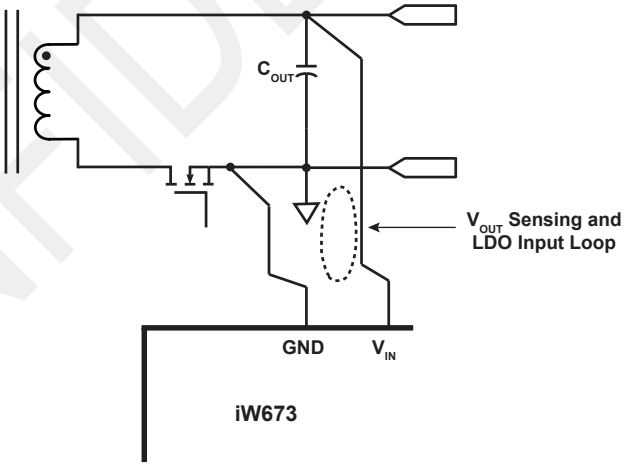
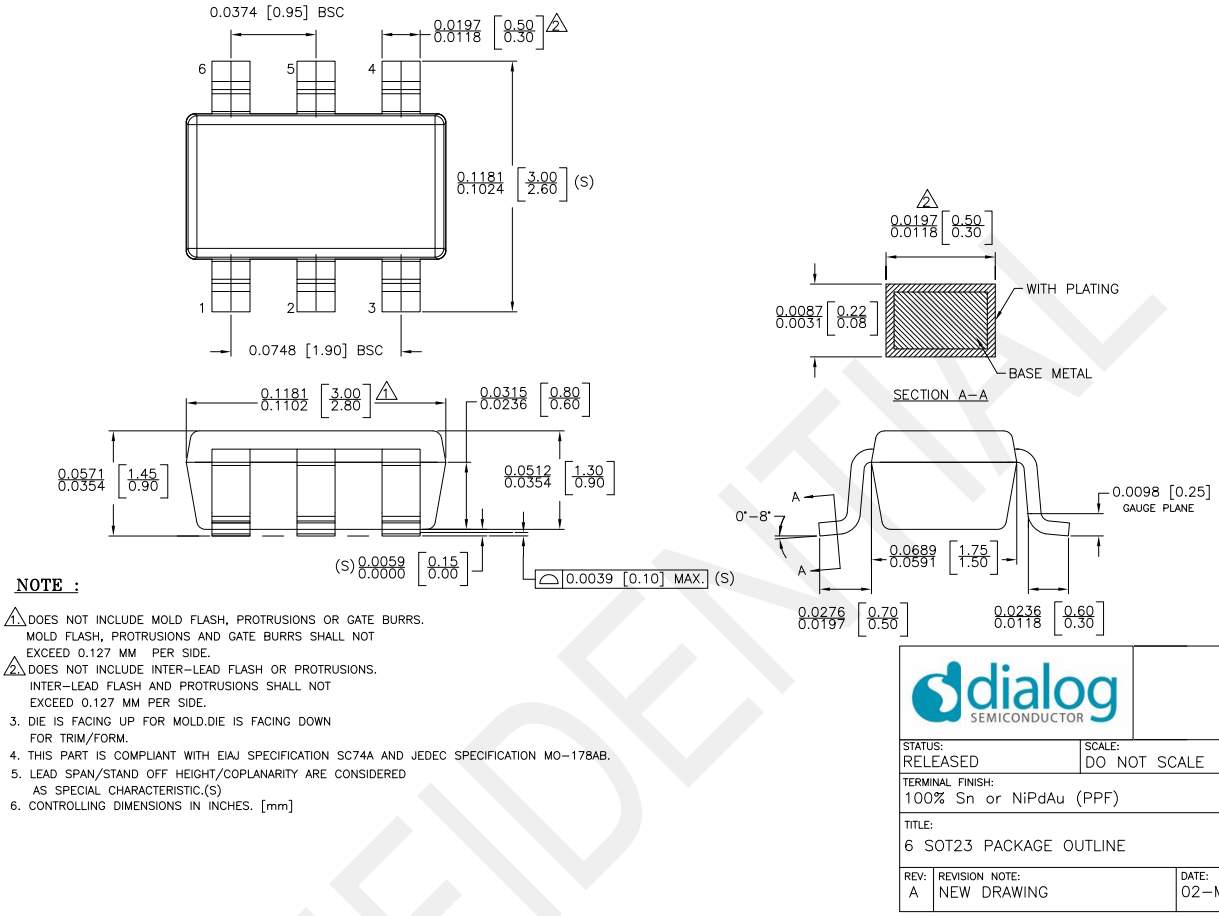


Figure 9.8 : V_{IN} LDO Input Loop and V_{IN} Sensing Loop

10 Physical Dimensions



NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.127 MM PER SIDE.
2. DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.127 MM PER SIDE.
3. DIE IS FACING UP FOR MOLD.DIE IS FACING DOWN FOR TRIM/FORM.
4. THIS PART IS COMPLIANT WITH EIAJ SPECIFICATION SC74A AND JEDEC SPECIFICATION MO–178AB.
5. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
6. CONTROLLING DIMENSIONS IN INCHES. [mm]

STATUS: RELEASED	SCALE: DO NOT SCALE
TERMINAL FINISH: 100% Sn or NiPdAu (PPF)	
TITLE: 6 SOT23 PACKAGE OUTLINE	
REV: A	REVISION NOTE: NEW DRAWING — DATE: 02–MAR–2015

11 Ordering Information

Part no.	Options	Package	Description
iW673-00	V_{OUT} < 16V. I_{OUT} < 4A. Not recommended for new designs	SOT23	Tape & Reel[1]
iW673-01	V_{OUT} < 25V. I_{OUT} > 4A or when SR MOSFET with large package inductance (TO-220 or similar) is used.	SOT23	Tape & Reel[1]
iW673-10	V_{OUT} < 25V. I_{OUT} < 4A. PLR circuit is disabled until UVLO once V_{OUT} reaches PLR disable threshold ($V_{LR\_DISABLE}$).	SOT23	Tape & Reel[1]
iW673-20	V_{OUT} < 25V. I_{OUT} < 4A.	SOT23	Tape & Reel[1]

Note 1: Tape and reel packing quantity is 3,000/reel. Minimum packing quantity is 3,000.

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